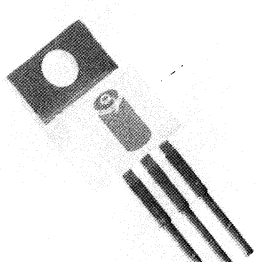

System Extension Data Book

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GENERAL INFORMATION

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PART NUMBER	DESCRIPTION	DATA BOOK
DS0621	TMEX™ Professional Software Developer's Kit	Automatic Identification
DS0630x	TMEX™ Performance Modules	Automatic Identification
DS1000	5–Tap Silicon Delay Line	System Extension
DS1000–IND	Industrial Temperature Range 5–Tap Silicon Delay Line	System Extension
DS1003	4–Tap Silicon Delay Line for RISC Applications	System Extension
DS1004	5–Tap High–Speed Silicon Delay Line	System Extension
DS1005	5–Tap Silicon Delay Line	System Extension
DS1007	7–in–1 Silicon Delay Line	System Extension
DS1010	10–Tap Silicon Delay Line	System Extension
DS1012	2–in–1 Sub–Miniature Silicon Delay Line with Logic	System Extension
DS1013	3–in–1 Silicon Delay Line	System Extension
DS1020	Programmable 8–Bit Silicon Delay Line	System Extension
DS1021	Programmable 8-Bit Silicon Delay Line	System Extension
DS1033	3–in–1 Low–Voltage Silicon Delay Line	System Extension
DS1035	3–in–1 High–Speed Silicon Delay Line	System Extension
DS1040	Programmable One–Shot Pulse Generator	System Extension
DS1044	4–in–1 High–Speed Silicon Delay Line	System Extension
DS1045	4–Bit Dual Programmable Delay Line	System Extension
DS1200	Serial RAM Chip	Timekeeping and NV RAM
DS1201	Electronic Tag	Timekeeping and NV RAM
DS1202, DS1202S	Serial Timekeeping Chip	Timekeeping and NV RAM
DS1204V	Electronic Key	Automatic Identification
DS1205S	MultiKey Chip	Automatic Identification
DS1205V	MultiKey	Automatic Identification
DS1206	Phantom Serial Interface Chip	System Extension
DS1207	TimeKey	Automatic Identification
DS1210	Nonvolatile Controller Chip	System Extension
DS1211	Nonvolatile Controller x 8 Chip	System Extension
DS1212	Nonvolatile Controller x 16 Chip	System Extension
DS1213B	SmartSocket 16K/64K	Timekeeping and NV RAM
DS1213C	SmartSocket 256K	Timekeeping and NV RAM
DS1213D	SmartSocket 256K/1M	Timekeeping and NV RAM
DS1215	Phantom Time Chip	Timekeeping and NV RAM
DS1216B	SmartWatch/RAM 16K/64K	Timekeeping and NV RAM
DS1216C	SmartWatch/RAM 64K/256K	Timekeeping and NV RAM
DS1216D	SmartWatch/RAM 256K/1M	Timekeeping and NV RAM
DS1216E	SmartWatch/ROM 64K/256K	Timekeeping and NV RAM
DS1216F	SmartWatch/ROM 64K/256K/1M	Timekeeping and NV RAM
DS1217A	Nonvolatile Read/Write Cartridge	Timekeeping and NV RAM
DS1217M	Nonvolatile Read/Write Cartridge	Timekeeping and NV RAM
DS1218	Nonvolatile Controller	System Extension
DS1220AB/AD	16K Nonvolatile SRAM	Timekeeping and NV RAM
DS1220Y	16K Nonvolatile SRAM	Timekeeping and NV RAM
DS1221	Nonvolatile Controller x 4 Chip	System Extension
DS1222	BankSwitch Chip	System Extension
DS1225AB/AD	64K Nonvolatile SRAM	Timekeeping and NV RAM
DS1225Y	64K Nonvolatile SRAM	Timekeeping and NV RAM

PART NUMBER	DESCRIPTION	DATA BOOK
DS1228	+5V Powered Dual RS–232 Transmitter/Receiver	System Extension
DS1229	+5V Powered Triple RS–232 Transmitter/Receiver	System Extension
DS1230Y/AB	256K Nonvolatile SRAM	Timekeeping and NV RAM
DS1231/S	Power Monitor Chip	System Extension
DS1232	MicroMonitor Chip	System Extension
DS1232LP/LPS	Low Power MicroMonitor Chip	System Extension
DS1233	5V EconoReset	System Extension
DS1233A	3.3V EconoReset	System Extension
DS1233D	5V EconoReset	System Extension
DS1233M	EconoReset	System Extension
DS1234	Conditional Nonvolatile Controller Chip	System Extension
DS1236	MicroManager Chip	System Extension
DS1236A	MicroManager Chip	System Extension
DS1237	DRAM Nonvolatizer Chip	System Extension
DS1238	MicroManager	System Extension
DS1238A	MicroManager	System Extension
DS1239	MicroManager Chip	System Extension
DS1243Y	64K NV SRAM with Phantom Clock	Timekeeping and NV RAM
DS1244Y	256K NV SRAM with Phantom Clock	Timekeeping and NV RAM
DS1245Y/AB	1024K Nonvolatile SRAM	Timekeeping and NV RAM
DS1248Y	1024K NV SRAM with Phantom Clock	Timekeeping and NV RAM
DS1249Y	2048K Nonvolatile SRAM	Supplement 5/95
DS1250	KeyRing	Timekeeping and NV RAM
DS1259	Battery Manager Chip	Timekeeping and NV RAM
DS1260	Smart Battery	Timekeeping and NV RAM
DS1267	Dual Digital Potentiometer Chip	System Extension
DS1275	Line–Powered RS–232 Transceiver Chip	System Extension
DS1280	3–Wire to Bytewide Converter Chip	Timekeeping and NV RAM
DS1283	Watchdog Timekeeper Chip	Timekeeping and NV RAM
DS1284	Watchdog Timekeeper Chip	Timekeeping and NV RAM
DS1285/DS1285Q	Real Time Clock	Timekeeping and NV RAM
DS1286	Watchdog Timekeeper	Timekeeping and NV RAM
DS1287	Real Time Clock	Timekeeping and NV RAM
DS1287A	Real Time Clock	Timekeeping and NV RAM
DS12885, DS12885Q, and DS12885T	Real Time Clock	Timekeeping and NV RAM
DS12887	Real Time Clock	Timekeeping and NV RAM
DS12887A	Real Time Clock	Timekeeping and NV RAM
DS129x	Eliminator	System Extension
DS1302	Trickle Charge Timekeeping Chip	Timekeeping and NV RAM
DS1307	64 X 8 Serial Real Time Clock	Supplement 5/95
DS1330YLPM/ABLPM	256K Nonvolatile SRAM with Power Monitors	Timekeeping and NV RAM
DS1336	Afterburner Chip	System Extension
DS1345YLPM/ABLPM	1024K Nonvolatile SRAM with Power Monitors	Timekeeping and NV RAM
DS1350YLPM/ABLPM	4096K Nonvolatile SRAM with Power Monitors	Timekeeping and NV RAM
DS1380	RAMport	Timekeeping and NV RAM
DS1381	NV RAMport	Timekeeping and NV RAM
DS1385/DS1387	RAMified Real Time Clock 4K x 8	Timekeeping and NV RAM

PART NUMBER	DESCRIPTION	DATA BOOK
DS1386	RAMified Watchdog Timekeeper	Timekeeping and NV RAM
DS1395/DS1397	RAMified Real Time Clock	Timekeeping and NV RAM
DS1401	Front Panel Button Holder	Automatic Identification
DS1402	Button Cable	Automatic Identification
DS1410D	Parallel Port Button Holder	Automatic Identification
DS1410K	Parallel Holder Developer's Kit	Automatic Identification
DS1412	Serial Port Button Holder	Automatic Identification
DS1412K	Serial Holder Developer's Kit	Automatic Identification
DS1414	Network Button Holder	Automatic Identification
DS1414K	Authorization Button Developer's Kit	Automatic Identification
DS1420	Serial ID Button	Automatic Identification
DS1422	1Kbit Add–Only UniqueWare™ Button	Automatic Identification
DS1425	Multi Button™	Automatic Identification
DS1427	Time Button™	Automatic Identification
DS14285/DS14287	Real Time Clock with NVRAM Control	Supplement 5/95
DS1485/DS1488	RAMified Real Time Clock 8K x 8	Timekeeping and NV RAM
DS1486	RAMified Watchdog Timekeeper	Timekeeping and NV RAM
DS1495/DS1497	RAMified Real Time Clock	Timekeeping and NV RAM
DS1585/DS1587	Serialized Real Time Clocks	Timekeeping and NV RAM
DS1589/DS1593	Serialized Real Time Clocks	Timekeeping and NV RAM
DS1602	Elapsed Time Counter	Timekeeping and NV RAM
DS1603	Elapsed Time Counter Module	Timekeeping and NV RAM
DS1609	Dual Port RAM	Timekeeping and NV RAM
DS1610	Partitioned NV Controller	System Extension
DS1612	Lithium Battery Monitor	Timekeeping and NV RAM
DS1613C	Partitioned SmartSocket 256K	Timekeeping and NV RAM
DS1613D	Partitioned SmartSocket 1M	Timekeeping and NV RAM
DS1620	Digital Thermometer and Thermostat	System Extension
DS1621	Digital Thermometer and Thermostat	System Extension
DS1623	Digital Thermometer and Thermostat	System Extension
DS1624	Digital Thermometer and Memory	System Extension
DS1625	Digital Thermometer and Thermostat	System Extension
DS1630Y/AB, DS1630YLPM/ABLPM	Partitionable 256K NV SRAM	Timekeeping and NV RAM
DS1632	PC Power Fail and Reset Controller	System Extension
DS1633	High–Speed Battery Recharger	System Extension
DS1633x	High–Speed Battery Charger	System Extension
DS1640/DS1640C	Personal Computer Power FET	System Extension
DS1642	Nonvolatile Timekeeping RAM	Timekeeping and NV RAM
DS1643/DS1643LPM	Nonvolatile Timekeeping RAM	Timekeeping and NV RAM
DS1644/DS1644LPM	Nonvolatile Timekeeping RAM	Timekeeping and NV RAM
DS1645Y/AB, DS1645YLPM/ABLPM	Partitionable 1024K NV SRAM	Timekeeping and NV RAM
DS1646/DS1646LPM	Nonvolatile Timekeeping RAM	Timekeeping and NV RAM
DS1647	Nonvolatile Timekeeping RAM	Timekeeping and NV RAM
DS1650Y/AB, DS1650YLPM/ABLPM	Partitionable 4096K NV SRAM	Timekeeping and NV RAM
DS1651/DS1652	3–Code Lock/Key Match Memory System	System Extension
DS1652B	Code Memory Key	System Extension
DS1653/DS1652	4–Code Lock/Key Match Memory System	System Extension

PART NUMBER	DESCRIPTION	DATA BOOK
DS1658Y/AB	Partitionable 128K x 16 NV SRAM	Timekeeping and NV RAM
DS1666, DS1666S	Audio Digital Resistor	System Extension
DS1667	Digital Resistor with OP AMP	System Extension
DS1668, DS1669, DS1669S	Dallastat™ Electronic Digital Rheostat	System Extension
DS1685/DS1687	3 Volt/5 Volt Real Time Clock	Supplement 5/95
DS1688/DS1691	3 Volt/5 Volt Serialized Real Time Clock with NVRAM Control	Supplement 5/95
DS1689/DS1693	5 Volt/3 Volt Serialized Real Time Clock with NV RAM Control	Supplement 5/95
DS1705/DS1706	3.3 and 5.0 Volt MicroMonitor	System Extension
DS1707/DS1708	3.3 and 5.0 Volt MicroMonitor	System Extension
DS1710	Partitioned NV Controller	System Extension
DS17285/DS17287	3 Volt/5 Volt Real Time Clock	Supplement 5/95
DS1730Y/YLPM	3 Volt Partitionable 256K NV SRAM	Timekeeping and NV RAM
DS1745Y/YLPM	3 Volt Partitionable 1024K NV SRAM	Timekeeping and NV RAM
DS17485/DS17487	3 Volt/5 Volt Real Time Clock	Supplement 5/95
DS1750Y/YLPM	3 Volt Partitionable 4096K NV SRAM	Timekeeping and NV RAM
DS1758Y	3V Partitionable 128K x 16 NV SRAM	Timekeeping and NV RAM
DS1800	Dual Inverting Log/Gain Attenuator	System Extension
DS1801	Dual Audio Taper Potentiometer	System Extension
DS1802	Dual Audio Taper Potentiometer with Pushbutton Control	System Extension
DS1803	Addressable Dual Digital Potentiometer	System Extension
DS1804	NV Trimmer Potentiometer	System Extension
DS1806	Digital Sextet Potentiometer	System Extension
DS1807	Addressable Dual Audio Taper Potentiometer	System Extension
DS1810	5V EconoReset	System Extension
DS1811	5V EconoReset	System Extension
DS1813	5V EconoReset with Pushbutton	System Extension
DS1815	5V EconoReset	System Extension
DS1816	3.3V EconoReset	System Extension
DS1818	3V EconoReset with Pushbutton	System Extension
DS1820	1–Wire™ Digital Thermometer	System Extension
DS1821	Programmable Digital Thermostat	System Extension
DS1832	3.3 Volt MicroMonitor Chip	System Extension
DS1833	5V EconoReset	System Extension
DS1834/A/D	Dual EconoReset with Pushbutton	System Extension
DS1836A/B/C/D	3.3V/5.5V MicroManager	System Extension
DS1866	Log Trimmer Potentiometer	System Extension
DS1867	Dual Digital Potentiometer with EEPROM	System Extension
DS1868	Dual Digital Potentiometer Chip	System Extension
DS1869	3V Dallastat™ Electronic Digital Rheostat	System Extension
DS1920	Touch Thermometer™	Automatic Identification
DS1971	256–Bit EEPROM Touch Memory™	Automatic Identification
DS1981U/DS1982U	UniqueWare™ Touch Memory	Automatic Identification
DS1982	1Kbit Add–Only Touch Memory™	Automatic Identification
DS1985	16Kbit Add–Only Touch Memory™	Automatic Identification
DS1986	64Kbit Add–Only Touch Memory™	Automatic Identification
DS1990A	Touch Serial Number™	Automatic Identification
DS1991	Touch MultiKey™	Automatic Identification

PART NUMBER	DESCRIPTION	DATA BOOK
DS1992/DS1993	1Kbit/4Kbit Touch Memory™	Automatic Identification
DS1994	4Kbit Plus Time Touch Memory™	Automatic Identification
DS1995	16Kbit Touch Memory™	Automatic Identification
DS1996	64Kbit Touch Memory™	Automatic Identification
DS2009	512 x 9 FIFO Chip	Timekeeping and NV RAM
DS2010	1024 x 9 FIFO Chip	Timekeeping and NV RAM
DS2011	2048 x 9 FIFO Chip	Timekeeping and NV RAM
DS2012	4096 x 9 FIFO Chip	Timekeeping and NV RAM
DS2013	8192 x 9 FIFO Chip	Timekeeping and NV RAM
DS2016	2K x 8 3V Operation Static RAM	Timekeeping and NV RAM
DS2064	8K x 8 3V Operation Static RAM	Timekeeping and NV RAM
DS2105	SCSI Terminator	System Extension
DS21S07A	SCSI Terminator	System Extension
DS21S07C	SCSI Terminator	System Extension
DS2108	Differential SCSI Switchable Terminator	System Extension
DS2109	Plug and Play SCSI Terminator	System Extension
DS211	4 Driver/5Receiver RS–232 Serial Port	PC Data Book
DS2110	Plug and Play SCSI Terminator with EEPROM	System Extension
DS2112	BTL Terminator	System Extension
DS2130Q	Voice Messaging Processor	Telecommunications
DS2132A/Q	Digital Answering Machine Processor	Telecommunications
DS2141A	T1 Controller	Telecommunications
DS21Q41B	Quad T1 Framer	Telecommunications
DS2143/DS2143Q	E1 Controller	Telecommunications
DS21Q43A	Quad E1 Framer	Telecommunications
DS2151Q	T1 Single–Chip Transceiver	Telecommunications
DS2153Q	E1 Single–Chip Transceiver	Telecommunications
DS2164Q	G.726 ADPCM Processor	Telecommunications
DS2165/DS2165Q	16/24/32Kbps ADPCM Processor	Telecommunications
DS2172	Bit Error Rate Tester (BERT)	Telecommunications
DS2175	T1/CEPT Elastic Store	Telecommunications
DS2176	T1 Receive Buffer	Telecommunications
DS2180A	T1 Transceiver	Telecommunications
DS2181A	CEPT Primary Rate Transceiver	Telecommunications
DS2182A	T1 Line Monitor	Telecommunications
DS2186	Transmit Line Interface	Telecommunications
DS2187	Receive Line Interface	Telecommunications
DS2188	T1/CEPT Jitter Attenuator	Telecommunications
DS22B57	32K x 8 Static RAM	Timekeeping and NV RAM
DS222	Dual RS–232 Transmitter/Receiver with Shutdown	Supplement 5/95
DS2223/DS2224	EconoRAM	Automatic Identification
DS2227	Flexible NV SRAM Stik	Timekeeping and NV RAM
DS2229	Word–Wide 8 Meg SRAM Stik	Timekeeping and NV RAM
DS2250(T)	Soft Microcontroller	Soft Microcontroller
DS2251(T)	128K Soft Microcontroller	Soft Microcontroller
DS2252(T)	Secure Microcontroller	Soft Microcontroller
DS2282	T1 FDL Controller/Monitor Stik	Telecommunications
DS229	RS–232 Transmitter/Receiver	System Extension
DS2290	T1 Isolation Stik	Telecommunications

PART NUMBER	DESCRIPTION	DATA BOOK
DS2291	T1 Long Loop Stik	Telecommunications
DS232A	Dual RS–232 Transmitter/Receiver	System Extension
DS233A	Dual RS–232 Transmitter/Receiver	System Extension
DS2401	Silicon Serial Number	Automatic Identification
DS2404	EconoRAM Time Chip	Timekeeping and NV RAM
DS2404S–C01	Dual Port Memory Plus Time	Automatic Identification
DS2405	Addressable Switch	Automatic Identification
DS2407	Dual Addressable Switch Plus 1K–Bit Memory	Automatic Identification
DS2430A	256–Bit 1–Wire™ EEPROM	Automatic Identification
DS2434	Battery Identification Chip	System Extension
DS2435	Battery Identification Chip with Time/Temperature Histogram	System Extension
DS2501–UNW/DS2502–UNW	UniqueWare™ Add–Only Touch Memory	Automatic Identification
DS2502	1Kbit Add–Only Memory	Automatic Identification
DS2505	16Kbit Add–Only Memory	Automatic Identification
DS2506	64Kbit Add–Only Memory	Automatic Identification
DS5000(T)	Soft Microcontroller	Soft Microcontroller
DS5000FP	Soft Microcontroller Chip	Soft Microcontroller
DS5000TK	Evaluation Kit	Soft Microcontroller
DS5001FP	128K Soft Micro Chip	Soft Microcontroller
DS5002FP	Secure Micro	Soft Microcontroller
DS80C310	High–Speed Micro	High–Speed Microcontroller
DS80C320	High–Speed Micro	High–Speed Microcontroller
DS80C323	Low–Power Micro	High–Speed Microcontroller
DS83C520	ROM High–Speed Micro	High–Speed Microcontroller
DS87C520	EPROM High–Speed Micro	High–Speed Microcontroller
DS87C530	EPROM Micro with Real Time Clock	High–Speed Microcontroller
DS9000	Bytewide Cable Harness	Timekeeping and NV RAM
DS9002	Cartridge Housing	Timekeeping and NV RAM
DS9003	Cartridge Proto Board	Timekeeping and NV RAM
DS908xx	CyberKey/Card Receptacles	Timekeeping and NV RAM
DS9091K	1–Wire™ MicroLAN™ Evaluation Kit	Automatic Identification
DS9092	Touch Memory Probe	Automatic Identification
DS9092K	Touch Memory Starter Kit	Automatic Identification
DS9092R	Touch Port	Automatic Identification
DS9093x	Touch Memory Mount Products	Automatic Identification
DS9094	MicroCan Clip	Automatic Identification
DS9096P	Touch Memory Adhesive Pads	Automatic Identification
DS9097/DS9097E	Touch COM Port Adapter	Automatic Identification
DS9098	MicroCan Retainer	Automatic Identification
DS9100	Touch and Hold Probe Stampings	Automatic Identification
DS9101	Multi–Purpose Clip	Automatic Identification
DS9103K	Touch Memory Access Control Demo Kit	Automatic Identification

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS1000	14–Pin DIP	0 to 70	DS1000–xxx	xxx = 020 to 500 ns
	8–Pin DIP	0 to 70	DS1000M–xxx	xxx = 020 to 500 ns
	16–Pin SOIC	0 to 70	DS1000S–xxx	xxx = 020 to 500 ns
	8–Pin SOIC	0 to 70	DS1000Z–xxx	xxx = 020 to 500 ns
DS1000–IND	8–Pin DIP	–40 to +85	DS1000M–xxx Ind	xxx = 020 to 500 ns
	8–Pin SOIC	–40 to +85	DS1000Z–xxx Ind	xxx = 020 to 500 ns
	14–Pin DIP	–40 to +85	DS1000–xxx Ind	xxx = 020 to 500 ns
DS1003	8-Pin DIP	0 to 70	DS1003M–16	
	8–Pin DIP	0 to 70	DS1003M–20	
	8–Pin DIP	0 to 70	DS1003M–25	
	8–Pin DIP	0 to 70	DS1003M–33	
	8–Pin DIP	0 to 70	DS1003M–40	
	14–Pin DIP	0 to 70	DS1003–16	
	14–Pin DIP	0 to 70	DS1003–20	
	14–Pin DIP	0 to 70	DS1003–25	
	14–Pin DIP	0 to 70	DS1003–33	
	14–Pin DIP	0 to 70	DS1003–40	
DS1004	8–Pin DIP	0 to 70	DS1004M–002	13 ns total delay
	8–Pin DIP	0 to 70	DS1004M–003	17 ns total delay
	8–Pin DIP	0 to 70	DS1004M–004	21 ns total delay
	8–Pin DIP	0 to 70	DS1004M–005	25 ns total delay
	8–Pin SOIC	0 to 70	DS1004Z–002	13 ns total delay
	8–Pin SOIC	0 to 70	DS1004Z–003	17 ns total delay
	8–Pin SOIC	0 to 70	DS1004Z–004	21 ns total delay
	8–Pin SOIC	0 to 70	DS1004Z–005	25 ns total delay
DS1005	14–Pin DIP	0 to 70	DS1005–xxx	xxx = 060 to 250 ns
	8–Pin DIP	0 to 70	DS1005M–xxx	xxx = 060 to 250 ns
	16–Pin SOIC	0 to 70	DS1005S–xxx	xxx = 060 to 250 ns
DS1007	16–Pin DIP	0 to 70	DS1007–xxx	xxx = 001 to 014
	16–Pin SOIC	0 to 70	DS1007S–xxx	xxx = 001 to 014
DS1010	14–Pin DIP	0 to 70	DS1010–xxx	xxx = 050 to 500 ns
	16–Pin SOIC	0 to 70	DS1010S–xxx	xxx = 050 to 500 ns
DS1012	8–Pin DIP	0 to 70	DS1012M–xxx	
	8–Pin SOIC	0 to 70	DS1012Z–xxx	
DS1013	14–Pin DIP	0 to 70	DS1013–xxx	xxx = 010 to 200 ns
	8–Pin DIP	0 to 70	DS1013M–xxx	xxx = 010 to 200 ns
	16–Pin SOIC	0 to 70	DS1013S–xxx	xxx = 010 to 200 ns
DS1020	16–Pin DIP	0 to 70	DS1020–15	0.15 ns Steps
	16–Pin DIP	0 to 70	DS1020–25	0.25 ns Steps
	16–Pin DIP	0 to 70	DS1020–50	0.50 ns Steps
	16–Pin DIP	0 to 70	DS1020–100	1.00 ns Steps
	16–Pin DIP	0 to 70	DS1020–200	2.00 ns Steps
	16–Pin SOIC	0 to 70	DS1020S–15	0.15 ns Steps
	16–Pin SOIC	0 to 70	DS1020S–25	0.25 ns Steps
	16–Pin SOIC	0 to 70	DS1020S–50	0.50 ns Steps
	16–Pin SOIC	0 to 70	DS1020S–100	1.00 ns Steps
	16–Pin SOIC	0 to 70	DS1020S–200	2.00 ns Steps
DS1021	16–Pin SOIC	0 to 70	DS1021S–25	0.25 ns Steps
	16–Pin SOIC	0 to 70	DS1021S–50	0.50 ns Steps
DS1033	8–Pin DIP	0 to 70	DS1033M–xxx	xxx = 008 to 030 ns
	8–Pin SOIC	0 to 70	DS1033Z–xxx	xxx = 008 to 030 ns
	20–Pin TSSOP	0 to 70	DS1033E–xxx	xxx = 008 to 030 ns
DS1035	8–Pin DIP	0 to 70	DS1035M–xxx	xxx = 006 to 030 ns
	8–Pin SOIC	0 to 70	DS1035Z–xxx	xxx = 006 to 030 ns
	20–Pin TSSOP	0 to 70	DS1035E–xxx	xxx = 006 to 030 ns
DS1040	8–Pin DIP	0 to 70	DS1040M–75	75 ns max pulse width
	8–Pin DIP	0 to 70	DS1040M–100	100 ns max pulse width
	8–Pin DIP	0 to 70	DS1040M–150	150 ns max pulse width
	8–Pin DIP	0 to 70	DS1040M–200	200 ns max pulse width

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	8–Pin DIP	0 to 70	DS1040M–250	250 ns max pulse width
	8–Pin DIP	0 to 70	DS1040M–500	500 ns max pulse width
	8–Pin DIP	0 to 70	DS1040M–B50	50 ns max pulse width
	8–Pin DIP	0 to 70	DS1040M–D60	60 ns max pulse width
	8–Pin DIP	0 to 70	DS1040M–A15	15 ns max pulse width
	8–Pin DIP	0 to 70	DS1040M–A20	20 ns max pulse width
	8–Pin DIP	0 to 70	DS1040M–A32	32.5 ns max pulse width
	8–Pin DIP	0 to 70	DS1040M–B40	40 ns max pulse width
	8–Pin DIP	0 to 70	DS1040M–D70	70 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–75	75 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–100	100 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–150	150 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–200	200 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–250	250 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–500	500 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–B50	50 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–D60	60 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–A15	15 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–A20	20 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–A32	32.5 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–B40	40 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–D70	70 ns max pulse width
DS1044	14–Pin DIP	0 to 70	DS1044–xxx	xxx = 005 to 025 ns
	14–Pin SOIC	0 to 70	DS1044R–xxx	xxx = 005 to 025 ns
DS1045	16–Pin DIP	0 to 70	DS1045–2	2 ns Steps
	16–Pin DIP	0 to 70	DS1045–3	3 ns Steps
	16–Pin DIP	0 to 70	DS1045–4	4 ns Steps
	16–Pin DIP	0 to 70	DS1045–5	5 ns Steps
	16–Pin SOIC	0 to 70	DS1045S–2	2 ns Steps
	16–Pin SOIC	0 to 70	DS1045S–3	3 ns Steps
	16–Pin SOIC	0 to 70	DS1045S–4	4 ns Steps
	16–Pin SOIC	0 to 70	DS1045S–5	5 ns Steps
DS1210	8–Pin DIP	0 to 70	DS1210	
	16–Pin SOIC	0 to 70	DS1210S	
	8–Pin DIP	–40 to +85	DS1210N	
	16–Pin SOIC	–40 to +85	DS1210SN	
DS1211	20–Pin DIP	0 to 70	DS1211	
	20–Pin SOIC	0 to 70	DS1211S	
	20–Pin DIP	–40 to +85	DS1211N	
	20–Pin SOIC	–40 to +85	DS1211SN	
DS1212	28–Pin DIP	0 to 70	DS1212	
	28–Pin PLCC	0 to 70	DS1212Q	
	28–Pin DIP	–40 to +85	DS1212N	
	28–Pin PLCC	–40 to +85	DS1212QN	
DS1218	8–Pin DIP	0 to 70	DS1218	
	8–Pin SOIC	0 to 70	DS1218S	
DS1221	16–Pin DIP	0 to 70	DS1221	
	16–Pin SOIC	0 to 70	DS1221S	
	16–Pin DIP	–40 to +85	DS1221N	
	16–Pin SOIC	–40 to +85	DS1221SN	
DS1228	16–Pin DIP	0 to 70	DS1228	
	16–Pin SOIC	0 to 70	DS1228S	
DS1229	20–Pin DIP	0 to 70	DS1229	
	20–Pin SOIC	0 to 70	DS1229S	
DS1231	8–Pin DIP	0 to 70	DS1231–20	20
	8–Pin DIP	0 to 70	DS1231–35	35
	8–Pin DIP	0 to 70	DS1231–50	50
	8–Pin DIP	–40 to +85	DS1231N–20	20
	8–Pin DIP	–40 to +85	DS1231N–35	35

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	8–Pin DIP	–40 to +85	DS1231N–50	50
	8–Pin GULLWING	0 to 70	DS1231G–20	20
	8–Pin GULLWING	0 to 70	DS1231G–35	35
	8–Pin GULLWING	0 to 70	DS1231G–50	50
	8–Pin GULLWING	–40 to +85	DS1231GN–20	20
	8–Pin GULLWING	–40 to +85	DS1231GN–35	35
	8–Pin GULLWING	–40 to +85	DS1231GN–50	50
	16–Pin SOIC	0 to 70	DS1231S–20	20
	16–Pin SOIC	0 to 70	DS1231S–35	35
	16–Pin SOIC	0 to 70	DS1231S–50	50
	16–Pin SOIC	–40 to +85	DS1231SN–20	20
	16–Pin SOIC	–40 to +85	DS1231SN–35	35
	16–Pin SOIC	–40 to +85	DS1231SN–50	50
DS1232	8–Pin DIP	0 to 70	DS1232	
	8–Pin GULLWING	0 to 70	DS1232G	
	16–Pin SOIC	0 to 70	DS1232S	
	8–Pin DIP	–40 to +85	DS1232N	
	8–Pin GULLWING	–40 to +85	DS1232GN	
	16–Pin SOIC	–40 to +85	DS1232SN	
DS1232LP	8–Pin DIP	0 to 70	DS1232LP	
	8–Pin SOIC	0 to 70	DS1232LPS–2	
	16–Pin SOIC	0 to 70	DS1232LPS	
	8–Pin DIP	–40 to +85	DS1232LPN	
	8–Pin SOIC	–40 to +85	DS1232LPSN–2	
	16–Pin SOIC	–40 to +85	DS1232LPSN	
DS1233 5V	TO–92	–40 to +85	DS1233–5	5% MONITOR
	TO–92	–40 to +85	DS1233–10	10% MONITOR
	TO–92	–40 to +85	DS1233–15	15% MONITOR
	SOT–223	–40 to +85	DS1233Z–5	5% MONITOR
	SOT–223	–40 to +85	DS1233Z–10	10% MONITOR
	SOT–223	–40 to +85	DS1233Z–15	15% MONITOR
DS1233A 3.3V	TO–92	–40 to +85	DS1233A–10	10% MONITOR
	TO–92	–40 to +85	DS1233A–15	15% MONITOR
	SOT–223	–40 to +85	DS1233AZ–10	10% MONITOR
	SOT–223	–40 to +85	DS1233AZ–15	15% MONITOR
DS1233D 5V	TO–92	–40 to +85	DS1233D–5	5% MONITOR
	TO–92	–40 to +85	DS1233D–10	10% MONITOR
	TO–92	–40 to +85	DS1233D–15	15% MONITOR
	SOT–223	–40 to +85	DS1233DZ–5	5% MONITOR
	SOT–223	–40 to +85	DS1233DZ–10	10% MONITOR
	SOT–223	–40 to +85	DS1233DZ–15	15% MONITOR
DS1233M	TO–92	–40 to +85	DS1233M–55	5V–5% MONITOR
	TO–92	–40 to +85	DS1233M–5	5V–10% MONITOR
	TO–92	–40 to +85	DS1233M–3	3.3V–15% MONITOR
	8–Pin SOIC	–40 to +85	DS1233MS–55	5V–5% MONITOR
	8–Pin SOIC	–40 to +85	DS1233MS–5	5V–10% MONITOR
	8–Pin SOIC	–40 to +85	DS1233MS–3	3.3V–15% MONITOR
DS1234	14–Pin DIP	0 to 70	DS1234	
	16–Pin SOIC	0 to 70	DS1234S	
DS1236	16–Pin DIP	0 to 70	DS1236	10% MONITOR
	16–Pin DIP	0 to 70	DS1236–5	5% MONITOR
	16–Pin DIP	–40 to +85	DS1236N	10% MONITOR
	16–Pin DIP	–40 to +85	DS1236N–5	5% MONITOR
	16–Pin SOIC	0 to 70	DS1236S	10% MONITOR
	16–Pin SOIC	0 to 70	DS1236S–5	5% MONITOR
	16–Pin SOIC	–40 to +85	DS1236SN	10% MONITOR
	16–Pin SOIC	–40 to +85	DS1236SN–5	5% MONITOR

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS1236A	16–Pin DIP	0 to 70	DS1236A	10% MONITOR
	16–Pin DIP	0 to 70	DS1236A–5	5% MONITOR
	16–Pin DIP	–40 to +85	DS1236AN	10% MONITOR
	16–Pin DIP	–40 to +85	DS1236AN–5	5% MONITOR
	16–Pin SOIC	0 to 70	DS1236AS	10% MONITOR
	16–Pin SOIC	0 to 70	DS1236AS–5	5% MONITOR
	16–Pin SOIC	–40 to +85	DS1236ASN	10% MONITOR
	16–Pin SOIC	–40 to +85	DS1236ASN–5	5% MONITOR
DS1237	16–Pin DIP	0 to 70	DS1237–x	x = 1 to 8
	16–Pin SOIC	0 to 70	DS1237S–x	x = 1 to 8
DS1238	16–Pin DIP	0 to 70	DS1238	10% MONITOR
	16–Pin DIP	0 to 70	DS1238–5	5% MONITOR
	16–Pin DIP	–40 to +85	DS1238N	10% MONITOR
	16–Pin SOIC	0 to 70	DS1238S	10% MONITOR
	16–Pin SOIC	0 to 70	DS1238S–5	5% MONITOR
DS1238A	16–Pin DIP	0 to 70	DS1238A	10% MONITOR
	16–Pin DIP	0 to 70	DS1238A–5	5% MONITOR
	16–Pin SOIC	0 to 70	DS1238AS	10% MONITOR
	16–Pin SOIC	0 to 70	DS1238AS–5	5% MONITOR
DS1239	16–Pin DIP	0 to 70	DS1239	10% MONITOR
	16–Pin DIP	0 to 70	DS1239–5	5% MONITOR
	16–Pin DIP	–40 to +85	DS1239N	10% MONITOR
	16–Pin DIP	–40 to +85	DS1239N–5	5% MONITOR
	16–Pin SOIC	0 to 70	DS1239S	10% MONITOR
	16–Pin SOIC	0 to 70	DS1239S–5	5% MONITOR
	16–Pin SOIC	–40 to +85	DS1239SN	10% MONITOR
DS1267	14–Pin DIP	0 to 70	DS1267–10	10K ohms
	14–Pin DIP	0 to 70	DS1267–50	50K ohms
	14–Pin DIP	0 to 70	DS1267–100	100K ohms
	14–Pin DIP	–40 to +85	DS1267N–10	10K ohms
	14–Pin DIP	–40 to +85	DS1267N–50	50K ohms
	14–Pin DIP	–40 to +85	DS1267N–100	100K ohms
	14–Pin SOIC	0 to 70	DS1267S–10	10K ohms
	14–Pin SOIC	0 to 70	DS1267S–50	50K ohms
	14–Pin SOIC	0 to 70	DS1267S–100	100K ohms
	14–Pin SOIC	–40 to +85	DS1267SN–10	10K ohms
	14–Pin SOIC	–40 to +85	DS1267SN–50	50K ohms
	14–Pin SOIC	–40 to +85	DS1267SN–100	100K ohms
	20–Pin TSSOP	0 to 70	DS1267E–10	10K ohms
	20–Pin TSSOP	0 to 70	DS1267E–50	50K ohms
	20–Pin TSSOP	0 to 70	DS1267E–100	100K ohms
DS1275	8–Pin DIP	0 to 70	DS1275	
	8–Pin SOIC	0 to 70	DS1275S	
DS129X	16–Pin Encap. DIP	0 to 70	DS1290	
	16–Pin DIP	0 to 70	DS1291	
	24–Pin Encap. DIP	0 to 70	DS1292	
	24–Pin DIP	0 to 70	DS1293	
	16–Pin DIP	–40 to +85	DS1291N	
	24–Pin DIP	–40 to +85	DS1293N	
DS1336	16–Pin DIP	0 to 70	DS1336	
	16–Pin SOIC	0 to 70	DS1336S	
	16–Pin DIP	–40 to +85	DS1336N	
	16–Pin SOIC	–40 to +85	DS1336SN	
DS1610	16–Pin DIP	0 to 70	DS1610	
	16–Pin SOIC	0 to 70	DS1610S	
	16–Pin DIP	–40 to +85	DS1610N	
	16–Pin SOIC	–40 to +85	DS1610SN	
DS1620	8–Pin DIP	–55 to +125	DS1620	
	8–Pin SOIC	–55 to +125	DS1620S	

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS1621	8–Pin DIP	–55 to +125	DS1621	
	8–Pin SOIC	–55 to +125	DS1621S	
DS1623	8–Pin DIP	–55 to +125	DS1623	
	8–Pin SOIC	–55 to +125	DS1623S	
DS1624	8–Pin DIP	–55 to +125	DS1624	
	8–Pin SOIC	–55 to +125	DS1624S	
DS1625	8–Pin DIP	–55 to +125	DS1625	
	8–Pin SOIC	–55 to +125	DS1625S	
DS1632	16–Pin DIP	0 to 70	DS1632	
	16–Pin SOIC	0 to 70	DS1632S	
	16–Pin DIP	–40 to +85	DS1632N	
	16–Pin SOIC	–40 to +85	DS1632SN	
DS1633	3–Pin TO–220	–40 to +85	DS1633XX	See data sheet for complete specifications.
DS1640	16–Pin DIP	0 to 70	DS1640	
	16–Pin SOIC	0 to 70	DS1640S	
	16–Pin DIP	–40 to +85	DS1640N	
	16–Pin SOIC	–40 to +85	DS1640SN	
	16–Pin DIP	0 to 70	DS1640C	Consumer Grade
	16–Pin SOIC	0 to 70	DS1640SC	Consumer Grade
DS1651	8–Pin DIP	–25 to +85	DS1651	
	8–Pin SOIC	–25 to +85	DS1651S	
DS1652	8–Pin DIP	–25 to +85	DS1652	
	8–Pin SOIC	–25 to +85	DS1652S	
DS1653	16–Pin DIP	–25 to +85	DS1653	
	16–Pin SOIC	–25 to +85	DS1653S	
DS1666	14–Pin DIP	0 to 70	DS1666–10	10K ohms
	14–Pin DIP	0 to 70	DS1666–50	50K ohms
	14–Pin DIP	0 to 70	DS1666–100	100K ohms
	14–Pin DIP	–40 to +85	DS1666N–10	10K ohms
	14–Pin DIP	–40 to +85	DS1666N–50	50K ohms
	14–Pin DIP	–40 to +85	DS1666N–100	100K ohms
	16–Pin SOIC	0 to 70	DS1666S–10	10K ohms
	16–Pin SOIC	0 to 70	DS1666S–50	50K ohms
	16–Pin SOIC	0 to 70	DS1666S–100	100K ohms
	16–Pin SOIC	–40 to +85	DS1666SN–10	10K ohms
	16–Pin SOIC	–40 to +85	DS1666SN–50	50K ohms
	16–Pin SOIC	–40 to +85	DS1666SN–100	100K ohms
DS1667	20–Pin DIP	0 to 70	DS1667–10	10K ohms
	20–Pin DIP	0 to 70	DS1667–50	50K ohms
	20–Pin DIP	0 to 70	DS1667–100	100K ohms
	20–Pin DIP	–40 to +85	DS1667N–10	10K ohms
	20–Pin DIP	–40 to +85	DS1667N–50	50K ohms
	20–Pin DIP	–40 to +85	DS1667N–100	100K ohms
	20–Pin SOIC	0 to 70	DS1667S–10	10K ohms
	20–Pin SOIC	0 to 70	DS1667S–50	50K ohms
	20–Pin SOIC	0 to 70	DS1667S–100	100K ohms
	20–Pin SOIC	–40 to +85	DS1667SN–10	10K ohms
	20–Pin SOIC	–40 to +85	DS1667SN–50	50K ohms
	20–Pin SOIC	–40 to +85	DS1667SN–100	100K ohms
DS1668	6–Pin Pushbutton	0 to 70	DS1668–10	10K ohms
	6–Pin Pushbutton	0 to 70	DS1668–50	50K ohms
	6–Pin Pushbutton	0 to 70	DS1668–100	100K ohms
DS1669	8–Pin DIP	0 to 70	DS1669–10	10K ohms
	8–Pin DIP	0 to 70	DS1669–50	50K ohms
	8–Pin DIP	0 to 70	DS1669–100	100K ohms
	8–Pin DIP	–40 to +85	DS1669N–10	10K ohms
	8–Pin DIP	–40 to +85	DS1669N–50	50K ohms
	8–Pin DIP	–40 to +85	DS1669N–100	100K ohms

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	8–Pin SOIC	0 to 70	DS1669S–10	10K ohms
	8–Pin SOIC	0 to 70	DS1669S–50	50K ohms
	8–Pin SOIC	0 to 70	DS1669S–100	100K ohms
	8–Pin SOIC	–40 to +85	DS1669SN–10	10K ohms
	8–Pin SOIC	–40 to +85	DS1669SN–50	50K ohms
	8–Pin SOIC	–40 to +85	DS1669SN–100	100K ohms
DS1705/06	8–Pin DIP	–40 to +85	DS1705EPA	5V–5% MONITOR
	8–Pin SOIC	–40 to +85	DS1705ESA	5V–5% MONITOR
	8–Pin DIP	–40 to +85	DS1706EPA	5V–10% MONITOR
	8–Pin SOIC	–40 to +85	DS1706ESA	5V–10% MONITOR
	8–Pin DIP	–40 to +85	DS1706LEPA	5V–5% MONITOR
	8–Pin SOIC	–40 to +85	DS1706LESA	5V5% MONITOR
	8–Pin DIP	–40 to +85	DS1706PEPA	3.3V–20% MONITOR
	8–Pin SOIC	–40 to +85	DS1706PESA	3.3V–20% MONITOR
	8–Pin DIP	–40 to +85	DS1706REPA	3.3V–20% MONITOR
	8–Pin SOIC	–40 to +85	DS1706RESA	3.3V–20% MONITOR
	8–Pin DIP	–40 to +85	DS1706SEPA	3.3V–10% MONITOR
	8–Pin SOIC	–40 to +85	DS1706SESA	3.3V–10% MONITOR
	8–Pin SOIC	–40 to +85	DS1706SESA	3.3V–10% MONITOR
	8–Pin DIP	–40 to +85	DS1706TEPA	3.3V–5% MONITOR
	8–Pin SOIC	–40 to +85	DS1706TESA	3.3V–5% MONITOR
DS1707/08	8–Pin DIP	–40 to +85	DS1707EPA	5V–5% MONITOR
	8–Pin SOIC	–40 to +85	DS1707ESA	5V–5% MONITOR
	8–Pin DIP	–40 to +85	DS1708EPA	5V–10% MONITOR
	8–Pin SOIC	–40 to +85	DS1708ESA	5V–10% MONITOR
	8–Pin DIP	–40 to +85	DS1708REPA	3.3V–20% MONITOR
	8–Pin SOIC	–40 to +85	DS1708RESA	3.3V–20% MONITOR
	8–Pin DIP	–40 to +85	DS1708SEPA	3.3V–10% MONITOR
	8–Pin SOIC	–40 to +85	DS1708SESA	3.3V–10% MONITOR
	8–Pin DIP	–40 to +85	DS1708TEPA	3.3V–5% MONITOR
	8–Pin SOIC	–40 to +85	DS1708TESA	3.3V–5% MONITOR
DS1710	16–Pin DIP	0 to 70	DS1710	
	16–Pin SOIC	0 to 70	DS1710S	
	20–Pin TSSOP	0 to 70	DS1710E	
	16–Pin DIP	–40 to +85	DS1710N	
	16–Pin SOIC	–40 to +85	DS1710SN	
	20–Pin TSSOP	–40 to +85	DS1710EN	
DS1800	20–Pin DIP	–20 to +70	DS1800	53K ohms
	20–Pin SOIC	–20 to +70	DS1800S	53K ohms
	20–Pin TSSOP	–20 to +70	DS1800E	53K ohms
	20–Pin DIP	–40 to +85	DS1800N	53K ohms
	20–Pin SOIC	–40 to +85	DS1800SN	53K ohms
	20–Pin TSSOP	–40 to +85	DS1800EN	53K ohms
DS1801	14–Pin DIP	–20 to +70	DS1801	45K ohms
	16–Pin SOIC	–20 to +70	DS1801S	45K ohms
	14–Pin TSSOP	–20 to +70	DS1801E	45K ohms
DS1802	20–Pin DIP	0 to 70	DS1802	50K ohms
	20–Pin SOIC	0 to 70	DS1802S	50K ohms
	20–Pin TSSOP	0 to 70	DS1802E	50K ohms
DS1803	16–Pin DIP	0 to 70	DS1803–xxx	xxx = 010, 050, 100K ohms
	16–Pin SOIC	0 to 70	DS1803S–xxx	xxx = 010, 050, 100K ohms
	14–Pin TSSOP	0 to 70	DS1803E–xxx	xxx = 010, 050, 100K ohms
	16–Pin DIP	–40 to +85	DS1803N–xxx	xxx = 010, 050, 100K ohms
	16–Pin SOIC	–40 to +85	DS1803SN–xxx	xxx = 010, 050, 100K ohms
	14–Pin TSSOP	–40 to +85	DS1803EN–xxx	xxx = 010, 050, 100K ohms
DS1804	8–Pin DIP	0 to 70	DS1804–xxx	xxx = 010, 050, 100K ohms
	8–Pin SOIC	0 to 70	DS1804Z–xxx	xxx = 010, 050, 100K ohms
	8–Pin DIP	–40 to +85	DS1804N–xxx	xxx = 010, 050, 100K ohms
	8–Pin SOIC	–40 to +85	DS1804ZN–xxx	xxx = 010, 050, 100K ohms

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS1806	20–Pin DIP	0 to 70	DS1806–xxx	xxx = 010, 050, 100K ohms
	20–Pin SOIC	0 to 70	DS1806S–xxx	xxx = 010, 050, 100K ohms
	20–Pin TSSOP	0 to 70	DS1806E–xxx	xxx = 010, 050, 100K ohms
	20–Pin DIP	–40 to +85	DS1806N–xxx	xxx = 010, 050, 100K ohms
	20–Pin SOIC	–40 to +85	DS1806SN–xxx	xxx = 010, 050, 100K ohms
	20–Pin TSSOP	–40 to +85	DS1806EN–xxx	xxx = 010, 050, 100K ohms
DS1807	14–Pin DIP	–20 to +70	DS1807	45K ohms
	16–Pin SOIC	–20 to +70	DS1807S	45K ohms
	14–Pin TSSOP	–20 to +70	DS1807E	45K ohms
DS1810	TO–92	0 to 70	DS1810–5	5V–5% MONITOR
	TO–92	0 to 70	DS1810–10	5V–10% MONITOR
	TO–92	0 to 70	DS1810–15	5V–15% MONITOR
	SOT–23	0 to 70	DS1810R–5/T&R	5V–5% MONITOR
	SOT–23	0 to 70	DS1810R–10/T&R	5V–10% MONITOR
	SOT–23	0 to 70	DS1810R–15/T&R	5V–15% MONITOR
DS1811	TO–92	0 to 70	DS1811–5	5V–5% MONITOR
	TO–92	0 to 70	DS1811–10	5V–10% MONITOR
	TO–92	0 to 70	DS1811–15	5V–15% MONITOR
	SOT–23	0 to 70	DS1811R–5/T&R	5V–5% MONITOR
	SOT–23	0 to 70	DS1811R–10/T&R	5V–10% MONITOR
	SOT–23	0 to 70	DS1811R–15/T&R	5V–15% MONITOR
DS1812	TO–92	0 to 70	DS1812–5	5V–5% MONITOR
	TO–92	0 to 70	DS1812–10	5V–10% MONITOR
	TO–92	0 to 70	DS1812–15	5V–15% MONITOR
	SOT–23	0 to 70	DS1812R–5/T&R	5V–5% MONITOR
	SOT–23	0 to 70	DS1812R–10/T&R	5V–10% MONITOR
	SOT–23	0 to 70	DS1812R–15/T&R	5V–15% MONITOR
DS1813	TO–92	0 to 70	DS1813–5	5V–5% MONITOR
	TO–92	0 to 70	DS1813–10	5V–10% MONITOR
	TO–92	0 to 70	DS1813–15	5V–15% MONITOR
	SOT–23	0 to 70	DS1813R–5/T&R	5V–5% MONITOR
	SOT–23	0 to 70	DS1813R–10/T&R	5V–10% MONITOR
	SOT–23	0 to 70	DS1813R–15/T&R	5V–15% MONITOR
DS1815	TO–92	0 to 70	DS1815–10	3.3V–10% MONITOR
	TO–92	0 to 70	DS1815–20	3.3V–20% MONITOR
	SOT–23	0 to 70	DS1815R–10/T&R	3.3V–10% MONITOR
	SOT–23	0 to 70	DS1815R–20/T&R	3.3V–20% MONITOR
DS1816	TO–92	0 to 70	DS1816–10	3.3V–10% MONITOR
	TO–92	0 to 70	DS1816–20	3.3V–20% MONITOR
	SOT–23	0 to 70	DS1816R–10/T&R	3.3V–10% MONITOR
	SOT–23	0 to 70	DS1816R–20/T&R	3.3V–20% MONITOR
DS1817	TO–92	0 to 70	DS1817–10	3.3V–10% MONITOR
	TO–92	0 to 70	DS1817–20	3.3V–20% MONITOR
	SOT–23	0 to 70	DS1817R–10/T&R	3.3V–10% MONITOR
	SOT–23	0 to 70	DS1817R–20/T&R	3.3V–20% MONITOR
DS1818	TO–92	0 to 70	DS1818–10	3.3V–10% MONITOR
	TO–92	0 to 70	DS1818–20	3.3V–20% MONITOR
	SOT–23	0 to 70	DS1818R–10/T&R	3.3V–10% MONITOR
	SOT–23	0 to 70	DS1818R–20/T&R	3.3V–20% MONITOR
DS1820	PR–35	–55 to +125	DS1820	
	8–Pin SOIC	–55 to +125	DS1820S	
DS1821	PR–35	–55 to +125	DS1821	
	8–Pin SOIC	–55 to +125	DS1821S	
	TO–220	–55 to +125	DS1821T	
DS1832	8–Pin DIP	0 to 70	DS1832	
	8–Pin SOIC	0 to 70	DS1832S	
	8–Pin DIP	–40 to +85	DS1832N	
	8–Pin SOIC	–40 to +85	DS1832SN	

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS1833	TO–92	–40 to +85	DS1833–5	5% MONITOR
	TO–92	–40 to +85	DS1833–10	10% MONITOR
	TO–92	–40 to +85	DS1833–15	15% MONITOR
	SOT–223	–40 to +85	DS1833Z–5	5% MONITOR
	SOT–223	–40 to +85	DS1833Z–10	10% MONITOR
	SOT–223	–40 to +85	DS1833Z–15	15% MONITOR
DS1834	8–Pin DIP	–40 to +85	DS1834	Active Low CMOS
	8–Pin SOIC	–40 to +85	DS1834S	Active Low CMOS
	8–Pin DIP	–40 to +85	DS1834A	Active Low Open Drain
	8–Pin SOIC	–40 to +85	DS1834AS	Active Low Open Drain
	8–Pin DIP	–40 to +85	DS1834D	Active High CMOS
	8–Pin SOIC	–40 to +85	DS1834DS	Active High CMOS
DS1866	8–Pin DIP	0 to 70	DS1866	10K ohms
	8–Pin SOIC	0 to 70	DS1866Z	10K ohms
	8–Pin DIP	–40 to +85	DS1866N	10K ohms
	8–Pin SOIC	–40 to +85	DS1866ZN	10K ohms
DS1867	14–Pin DIP	0 to 70	DS1867–10	10K ohms
	14–Pin DIP	0 to 70	DS1867–50	50K ohms
	14–Pin DIP	0 to 70	DS1867–100	100K ohms
	16–Pin SOIC	0 to 70	DS1867S–10	10K ohms
	16–Pin SOIC	0 to 70	DS1867S–50	50K ohms
	16–Pin SOIC	0 to 70	DS1867S–100	100K ohms
	20–Pin TSSOP	0 to 70	DS1867E–10	10K ohms
	20–Pin TSSOP	0 to 70	DS1867E–50	50K ohms
	20–Pin TSSOP	0 to 70	DS1867E–100	100K ohms
DS1868	14–Pin DIP	0 to 70	DS1868–10	10K ohms
	14–Pin DIP	0 to 70	DS1868–50	50K ohms
	14–Pin DIP	0 to 70	DS1868–100	100K ohms
	16–Pin DIP	0 to 70	DS1868S–10	10K ohms
	16–Pin DIP	0 to 70	DS1868S–50	50K ohms
	16–Pin DIP	0 to 70	DS1868S–100	100K ohms
	20–Pin TSSOP	0 to 70	DS1868E–10	10K ohms
	20–Pin TSSOP	0 to 70	DS1868E–50	50K ohms
	20–Pin TSSOP	0 to 70	DS1868E–100	100K ohms
DS1869	8–Pin DIP	0 to 70	DS1869–10	10K ohms
	8–Pin DIP	0 to 70	DS1869–50	50K ohms
	8–Pin DIP	0 to 70	DS1869–100	100K ohms
	8–Pin SOIC	0 to 70	DS1869S–10	10K ohms
	8–Pin SOIC	0 to 70	DS1869S–50	50K ohms
	8–Pin SOIC	0 to 70	DS1869S–100	100K ohms
DS2105	16–Pin SOIC	0 to 70	DS2105S	5% SCSI Terminator
	16–Pin SOIC	0 to 70	DS2105Z	5% SCSI Terminator
DS2108	24–Pin SOIC	0 to 70	DS2108S	Differential SCSI Terminator
DS2109	28–Pin SOIC	0 to 70	DS2109S	Plug and Play SCSI Terminator
DS2112	16–Pin SOIC	0 to 70	DS2112S	BTL Terminator
DS21S07A	16–Pin SOIC	0 to 70	DS21S07AS	2% SCSI Terminator
	20–Pin TSSOP	0 to 70	DS21S07AE	2% SCSI Terminator
DS21S07C	16–Pin SOIC	0 to 70	DS21S07CS	2% SCSI Terminator, reg. active
	20–Pin TSSOP	0 to 70	DS21S07CE	2% SCSI Terminator, reg. active
DS229	20–Pin DIP	0 to 70	DS229	
	20–Pin SOIC	0 to 70	DS229S	
	20–Pin TSSOP	0 to 70	DS229E	
	20–Pin DIP	–40 to +85	DS229N	
	20–Pin SOIC	–40 to +85	DS229SN	

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DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS232A	16–Pin DIP	0 to 70	DS232A	
	16–Pin SOIC	0 to 70	DS232AS	
	20–Pin TSSOP	0 to 70	DS232AE	
	16–Pin DIP	–40 to +85	DS232A–N	
	16–Pin SOIC	–40 to +85	DS232AS–N	
DS233A	20–Pin DIP	0 to 70	DS233A	
	20–Pin SOIC	0 to 70	DS233AS	
DS2434	PR–35	–40 to +85	DS2434	
DS2435	PR–35	–40 to +85	DS2435	

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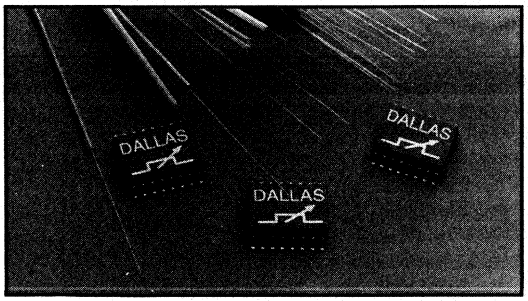
46-87-522-480

Switzerland
Computer Controls AG
41-1-308-6666

Taiwan
Landcol Enterprises
886-2-377-6070

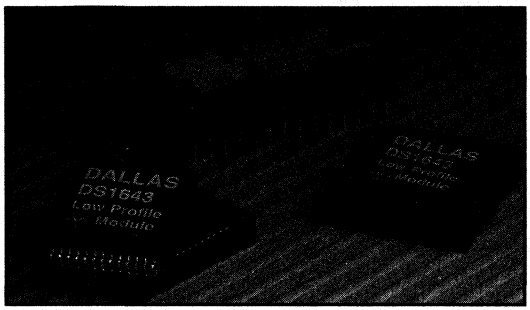
Thailand
Dynamar
66-2-376-0132

Turkey
Politeknik Elektronik
90-232-232-7432



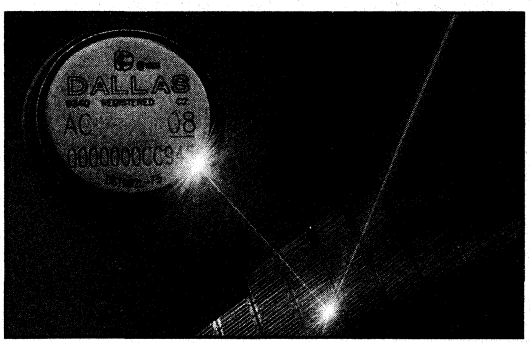
Silicon Timed Circuits

Silicon Timed Circuits (often referred to as delay lines) are chips that make subtle adjustments to the timing of high-performance electronics so that they will perform optimally. Because of the precision that lasers provide, some Silicon Timed Circuits can make timing adjustments down to a fraction of a nanosecond, which is the time it takes light to travel about a foot. For more information, call our Timing Problem Hotline at (214) 450-5348.



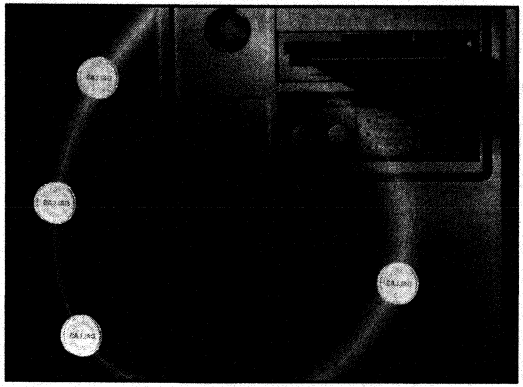
Timekeeping

A self-contained lithium energy source in conjunction with a silicon chip and quartz form a permanently powered clock/calendar within a single component. Various computer interfaces are available including phantom, serial, PC DOS, and bytewide memory.



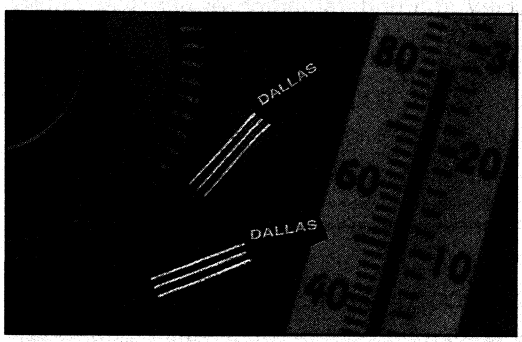
Automatic Identification

Touch Memory™ is a self-stick, Silicon Label™ in a stainless steel can. This MicroCan™ provides all the advantages canning has to offer, such as low cost, ruggedness, and the ability to preserve contents. The MicroCan's greatest advantage, however, is that a standalone chip can leave the confines of the computer and travel virtually anywhere to bring digital data to the point of use. Information can be updated time after time while the label is still affixed to its object. Wherever the silicon-labelled object goes, information is served up on the spot without recourse to remote networks. This family also includes low-cost memory chips in T0-92 packages.



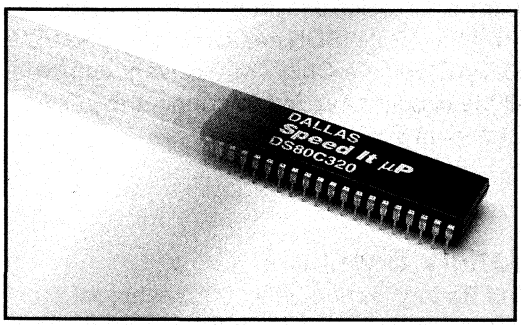
Software Authorization

Software Authorization products protect software applications from unauthorized execution and provide a means for PC and network access control. Software protection is achieved by using a Button as the "on" switch for a software application. The presence of a Button and validity of its contents determine the right to use. Buttons are very effective for implementing time- or count-based metering as a way of extending the temporary right to use software while maintaining protection control.



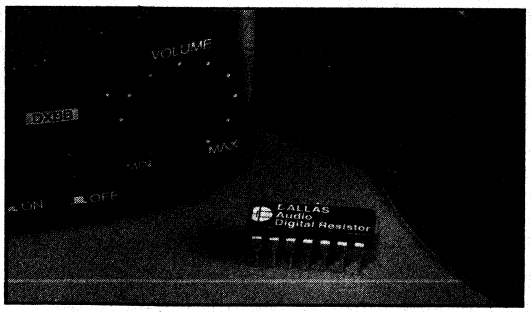
Thermal Management

Dallas Semiconductor makes thermal management easy with its line of direct-to-digital temperature sensors. These sensors provide a digital reading of temperature directly, eliminating the need for A/D converters dedicated to temperature measurement. Factory-calibrated to relieve the user of linearity corrections and other compensation, Dallas' sensors provide a range and accuracy unparalleled in the industry.



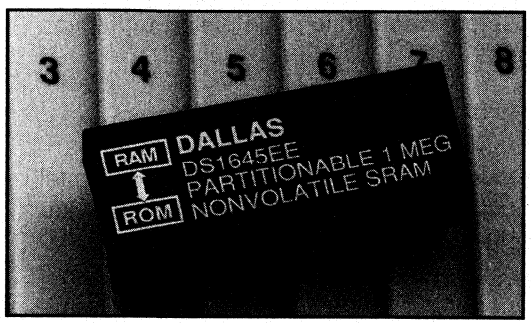
Microcontrollers

The DS80C320 High-Speed Micro is an 8051 family device that offers the highest performance in the industry for an 8-bit microcontroller. Pin- and instruction set-compatible with the standard 80C32, the High-Speed Micro uses only 4 clocks per instruction, as compared with 12 on other 8051's. Our DS500x Soft Micros convert industry-standard bytewide SRAM into high-performance, nonvolatile read/write storage.



System Extension

These products add a variety of special features to systems without encumbering design. A digital potentiometer is an all-silicon version of an electrical element used in almost all electronic equipment. CPU supervisors monitor vital conditions for a microprocessor.

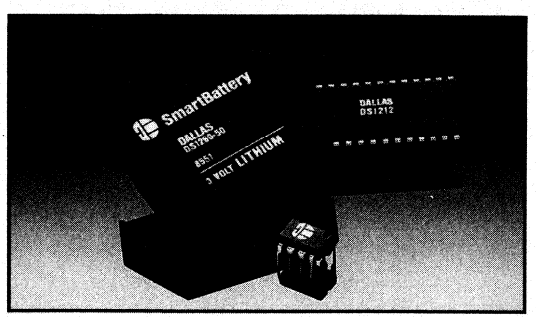


Nonvolatile RAM

Dallas Semiconductor has combined its circuitry and understanding of ultra low-power CMOS SRAM with improvements in long-life lithium power sources to develop a family of nonvolatile RAMs that retain data for more than 10 years in the absence of main power.

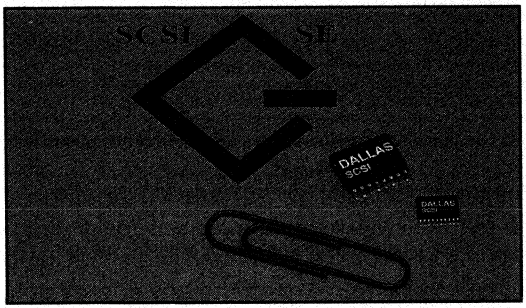
Telecommunications

A comprehensive product family addresses the requirements of high-speed, digital voice/data transmission and monitoring in T1, CEPT, or Primary Rate ISDN networks. The DS2151/53 T1/E1 Single-Chip Transceivers combine all the circuitry needed to connect to a T1 or E1 line in a single package.



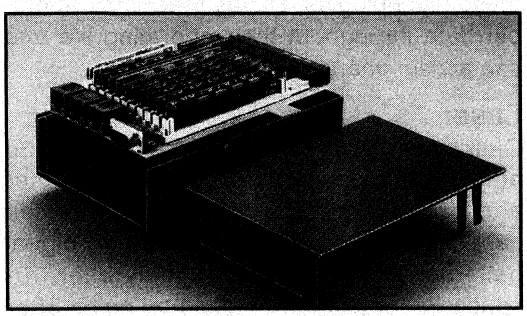
Battery Backup

The Battery Backup chip set crashproofs microprocessor-based systems, ensuring that no information is lost when main power fails. When power returns, computing resumes as if the failure had not occurred.



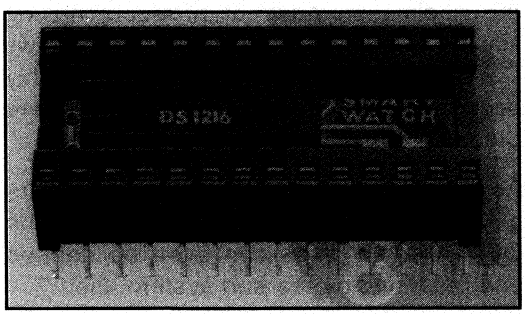
Bus Terminators

Bus termination products provide precise tolerance for high performance systems. SCSI terminators support all parallel SCSI standards including SCSI-3 Parallel Interface (SPI) and SCSI-3 Fast-20. The BTL terminator enhances Futurebus+ and BTL backplane designs by eliminating the specialized 2.1V supply.



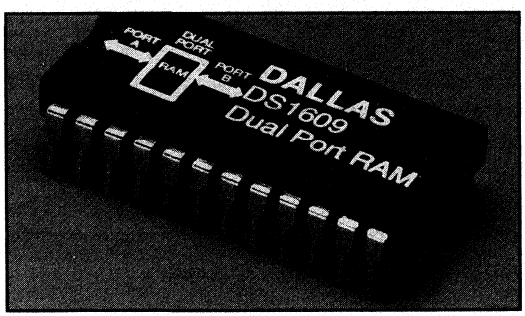
SIP Stik Prefabs

SIP Stiks are pretested subassemblies that snap into locking connectors for rapid construction of electronic systems. SIP Stiks increase density over traditional packing schemes five times by taking advantage of three, rather than the standard two, dimensions. SIP Stiks insert perpendicularly into the motherboard, making efficient use of the height dimension.



Intelligent Sockets

Intelligent Sockets incorporate active electronics in connectors that can be plugged into a system. Each adds an important capability without requiring substantive changes in the system. Some products in this family safeguard data in RAM for more than 10 years in the absence of external power. Others can time stamp and date events as well as nonvolatize RAM.



Multiport Memory

A complete family of FIFOs features identical pinouts that allow them to be interchanged. Designed for first-in, first-out processing for storing and retrieving data, the products are dual-ported for simultaneous reads and writes.

Dallas Semiconductor Corporation designs, manufactures, and markets electronic chips and chip-based subsystems. Founded in 1984, the Company uses customer problems as an entry point to develop products with widespread applications. The Company is committed to new product development as a means to increase future revenues and to diversify its markets, products, and customers.

Advanced technologies have given the Company a competitive edge over traditional approaches to semiconductors. Combining lithium energy cells with low-power CMOS chips powers chips for the useful life of the equipment. Direct laser writing enhances chip capabilities with high levels of precision and unique identities.

In its 11-year history, Dallas Semiconductor has developed 215 base products with over 1,000 variations shipped to more than 8,000 customers worldwide. A direct sales force and distribution network sell to original equipment manufacturers (OEMs) in personal computers and workstations, scientific and medical equipment, industrial controls, automatic identification, telecommunications, consumer electronics, and other markets.

Sales for 1994 totaled $181,432,000. Dallas Semiconductor has 850 employees. On March 19, 1990, the Company started trading on the New York Stock Exchange under the symbol DS.

TECHNOLOGY

Dallas Semiconductor's special technologies make possible Soft Silicon™ solutions—dynamic, flexible, chip-based products that can be molded in the final manufacturing stages or during use. Soft Silicon is made possible by lithium energy and direct laser writing.

Lithium

Using micro energy management techniques, Dallas Semiconductor has reduced power requirements to the point where a miniature lithium energy source powers products for the useful life of the equipment. Chips and Stiks (snap-in subassemblies) are made virtually crashproof with minimum current design techniques and special freshness seals that keep lithium cells from expending any energy until power is applied for the first time. Through these technologies, Dallas products remember data throughout their operating life and can accept change.

Laser

Direct laser writing makes each chip unique at low cost. A sub-micron positioning laser and control software developed at Dallas can engrave individual chips with digital patterns. This ability to routinely alter, reconfigure, or program individual chips after completion of wafer fabrication broadens the application base of products having similar design. Direct laser writing allows Dallas Semiconductor to develop highly accurate products for applications where precision is paramount.

As a result of these Late Definition technologies, exact chip definition can be left to the OEM. Certain chips can even be defined and redefined by the end system itself.

MANUFACTURING AND FACILITIES

As of January 1, 1995, the Company owns 342,500 square feet of building space and 22.9 acres of land in Dallas. The Company's wafer fabrication facility is a model of efficiency. In order to add capacity for growth the Company built a new advanced wafer fabrication facility that began production in 1994. The new fab is an important asset in terms of its capacity and process capabilities.

QUALITY SYSTEM

Product quality at Dallas Semiconductor results from a combination of design techniques, vendor controls, manufacturing methods, process monitors, and quality control inspections. SPC monitors placed at strategic points ensure that potential defects are detected promptly.

QUALITY CONTROL PROCESSES

- *Incoming Quality Control (IQC):* Piece parts and raw materials are inspected by IQC. New vendors and piece parts receive a First Article Inspection; subsequent incoming materials receive a sample inspection per MIL–STD–105.
- *In–Process Inspections:* Each manufacturing operation inspects its own work, ensuring immediate feedback and preventing deviations from going undetected due to subsequent processing.
- *Statistical Process Control (SPC):* Implemented in manufacturing, this process determines what inputs to the product flow are critical and how to track and control those inputs. Quality Engineering provides training, computer analysis, and feedback to manufacturing.
- *In–Process Sample Tests:* In order to guarantee the accuracy and completeness of in–process inspections and SPC monitors, QC Toll Gates at strategic locations perform sample inspections per MIL–STD–105.

RELIABILITY SYSTEM

Reliability is accomplished through a rigorous, comprehensive methodology of qualifying, analyzing, and monitoring new equipment, processes, products, and packages. A state–of–the–art environmental facility allows accelerated stresses to be performed and monitored in–house. In addition, a metallurgical laboratory has been equipped to perform real-time x–ray, x–ray florescence, and solderability measurements.

To minimize the human influence on the outcome of the reliability activity, a dedicated group of technicians and assistants handle all reliability stressing and testing. Reliability data resides on a customized computer–based tracking and retrieval system. Technical support includes oven and chamber calibrations, 100% electrical board checks, and strict electrostatic protection.

PRODUCT QUALIFICATION

Product qualification activity at Dallas Semiconductor involves a series of accelerated stress tests applied to production–ready material and follows a defined qualification plan. Random samples from at least three production lots, equally representing the production version of the product, are tested to meet reliability requirements. Any device failures detected during production qualification or subsequent monitoring are fully analyzed in our Failure Analysis Laboratory.

Products at Dallas Semiconductor fall into one of three classifications: Prototype or Engineering Sample, Prequal, and Fully Qualified.

- *Prototype or Engineering Sample:* Prototype products have not been fully characterized to all data sheet limits. However, based upon limited data, these products will meet data sheet limits. Final test and all processes used to manufacture the product are under engineering control. Qualification of the product has not started. The brand on prototype products will be PROTO or ES.
- *Prequal:* Prequal products meet prototype requirements and are characterized to all data sheet limits. Final test and all processes used to manufacture the product are stable and under manufacturing control. Qualification of the product has started.
- *Fully Qualified:* Fully qualified products meet prototype and prequal requirements. The qualification requirements given in the next section have been completed. Product must statistically meet reliability failure rates and quality requirements as established by Quality and Reliability Engineering.

Tables 1, 2 and 3 list the tests which a Dallas Semiconductor product must pass in order to be classified as fully qualified.

RELIABILITY MONITOR PROGRAM

In order to maintain continuous qualification status on all products, Dallas Semiconductor has implemented an extensive Reliability Monitor Program (RMP). The RMP monitors all design, wafer fabrication, and assembly processes in the qualified products database. Product is selected monthly from finished goods and subjected to a series of reliability tests similar to those used in the original qualification. Any failures generated from these tests require analysis to root cause and corrective action.

Data from the RMP is published quarterly and is available on demand.

FULL QUALIFICATION REQUIREMENTS FOR INTEGRATED CIRCUIT PRODUCTS Table 1

STRESS/TEST	CONDITION	DURATION	ACCEPTANCE CRITERIA (LTPD)
Outgoing Elec. Test	Data Sheet	0 Hr.	0.15%
Infant Life	125°C, 7.0V	48 Hr.	0.3%
High Temperature Operating Life	125°C, 5.5V	1000 Hr.	*0.4%
Use Condition Prediction	55°C, 5.5V	10 years	50 Fits
High Voltage Life	125°C, 7.0V	1000 Hr.	*0.4%
High Temperature Storage	150°C, No Bias	1000 Hr.	2.0%
Temperature Humidity Bias	85°C/85% RH, 5.5V	1000 Hr.	1.0%
Autoclave	121°C, 2 ATM Steam, Unbiased	168 Hr.	1.5%
Temperature Cycle	–55°C to +125°C	1000 cycle	1.0%
X–Ray	MIL–STD–883 Method 2012		15%
Bond Pull	MIL–STD–883 Method 2011	Premold	1.5%
Dimensions	MIL–STD–883 Method 2016		15%
Lead Integrity	MIL–STD–883 Method 2004		3.0%
Solderability	MIL–STD–883 Method 2003	8 Hr. Steamage	3.0%
ESD	MIL–STD–883 Method 3015		> ±1000 volts
Latch–up	JEDEC Std. 17		> 100 mW/pin

* Combined high voltage life and operating life requirement.

FULL QUALIFICATION REQUIREMENTS FOR MODULE PRODUCTS Table 2

STRESS/TEST	CONDITION	DURATION	ACCEPTANCE CRITERIA (LTPD)
Outgoing Elec. Test	Data Sheet	0 Hr.	0.15%
Use Condition Prediction	55°C, 5.5V	10 years	50 Fits
High Temperature Storage	85°C, No Bias	1000 Hr.	2.0%
*Temperature Humidity Bias	85°C/85% RH, 5.5V	959 Hr.	1.0%
Temperature Cycle	–40°C to +85°C	1000 cycle	1.0%
X–Ray	MIL–STD–883 Method 2012		15%
Dimensions	MIL–STD–883 Method 2016		15%
Lead Integrity	MIL–STD–883 Method 2004		3.0%
Solderability	MIL–STD–883 Method 2003	8 Hr. Steamage	3.0%

* Selected products.

FULL QUALIFICATION REQUIREMENTS FOR SIP STIK AND TOUCH MEMORY PRODUCTS Table 3

STRESS/TEST	CONDITION	DURATION	ACCEPTANCE CRITERIA (LTPD)
Outgoing Elec. Test	Data Sheet	0 Hr.	0.15%
High Temperature Storage	85°C, No Bias	1000 Hr.	7.0%
Temperature Humidity	60°C/90% RH	288 Hr.	7.0%
Temperature Cycle	–40°C to +85°C	500 cycle	7.0%

BATTERY MANAGEMENT

1

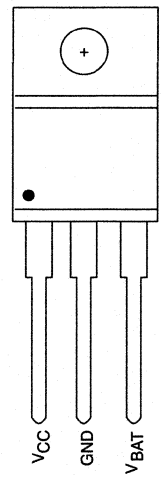
DALLAS SEMICONDUCTOR

DS1633
High–Speed Battery Recharger

FEATURES

- Recharges Lithium, NiCad, NiMH and Lead acid batteries
- Retains battery and power supply limits in onboard memory
- Serial 1–wire interface is used to program operating limits
- 3-pin TO–220 package
- Operating range 0°C to 70°C
- Applications include consumer electronics, portable/ cellular phones, pagers, medical instruments, backup memory systems, security systems
- Configurable to operate with 5V or 6V supplies

PIN ASSIGNMENT TO–220



See Mech. Drawings Section

PIN DESCRIPTION

V_{CC}	–	Supply Voltage
V_{BAT}	–	Battery Output
GND	–	Ground

DESCRIPTION

The DS1633 Battery Recharger is designed to be a complete battery charging system for standard charge or trickle charge applications. It can be configured to be used with either 5V or 6V supplies and battery voltages as high as 4.7V (3.7V for 5V supplies). The device is flexible enough to be used with a variety of battery chemistries and cell capacities. It provides timer termination of standard charge and automatically shifts into trickle charge. Battery voltage can be monitored and charging terminated if it exceeds a preset maximum as a safety feature. The output load line can be specified as the usual constant current recharge with a voltage limit or it can be configured to approximate any practical load line. All parameters, such as power supply range, charge current load line, trickle charge rate, and timer setting, are programmed into nonvolatile memory using the battery pin as a 1–wire communication port. To ease the task of configuring the device to specific application needs, Dallas Semiconductor makes available a programming kit, the DS1633K, containing easy–to–use software and hardware for IBM personal computers.

The DS1633 is able to offer this flexibility due to its unique architecture (see Figure 1). The device monitors the battery voltage and adjusts the values of the output impedance (R_{TH}) and open circuit voltage (V_{OC}) it presents to the battery. These values can be adjusted at 32 user definable points (breakpoints) that occur roughly every 37mV. This allows the device to approximate a wide range of charging lines; it is not limited to constant current or even monotonically decreasing functions.

OPERATION

Normal Mode

Upon application of power, the DS1633 will perform an initialization cycle requiring eight seconds. During this period it will determine if a battery is connected to the battery input by applying a voltage through 5 KΩ output impedance and looking for a non–zero current flow out of the pin. If a battery is connected, the value of the battery voltage will be determined using a 7–bit A/D convertor. This value will be used to determine which of the 32 user–defined breakpoints should be used to set R_{TH} and V_{OC}. Generally, as the battery charges the battery voltage will increase. When the battery voltage reaches or exceeds each user–defined breakpoint, the values of R_{TH} and V_{OC} will be modified accordingly. The battery voltage is measured and adjustments are made every eight seconds. The battery detection is performed at one–second intervals. If the amount of time the battery has been charging exceeds the preset limit, the device will apply the V_{OC} and R_{TH} as before, but only for a fraction of the eight–second cycle time. This duty cycle can be as low as 1/64 or as high as 1. In this way trickle charge can be accomplished by time averaging a short pulse over a longer period. Refer to Figure 2 for a detailed flow diagram of normal operation.

PROGRAMMING MODE

Register Structure

To configure a DS1633 to operate with a unique load line the user must program a set of 25–bit internal registers (Table 1). The first 32 (0–31) of these registers contain the information needed to locate each breakpoint and what the R_{TH} and V_{OC} are at that breakpoint, as well as the duty cycle to be used after the optional timer has expired. The last (32) register contains the bits which select the system power supply level (5V or 6V), the timer option, and the time limit (2 to 32 hours in 2–hour increments).

BREAKPOINT REGISTER STRUCTURE

Break Point Voltage Field

The break point voltage field specifies the range of battery voltage over which the R_{TH}, V_{OC} and pulse frequency information contained in that register is valid. This information is valid when the battery voltage meets or exceeds the breakpoint value, but is less than the next breakpoint value:

$$V_{BPX} \leq V_{BAT} < V_{BP(x+1)}$$

The xth breakpoint voltage (V_{BPX}) is determined according to the following formula:

$$V_{BPX}(n) = (n/127)(4.699V) \text{ ; for } 0 \leq n \leq 127$$

The value for n is entered in the field as a 7–bit binary value, LSB first. For reliable operation the first (x=0) breakpoint should be programmed such that $V_{BP0} = 0$. Successive breakpoints should be programmed with increasing values, that is:

$$V_{BPX} < V_{BP(x+1)}$$

If not all of the available breakpoints are used, the unused points should be assigned the maximum V_{BP} value (n=127) of 4.699V with R_{TH} and V_{OC} set to their maximum values (5060Ω and 5.5V) and the duty cycle field set to its minimum or zero value.

OPEN CIRCUIT VOLTAGE FIELD

The open circuit voltage field specifies the value of V_{OC} to be applied to the battery. V_{OC} can be set for values between 1.3V and 5.5V. This field is entered as a 7–bit binary value, LSB first. The value of $V_{OC}(n)$ is determined as follows:

$$V_{OC}(n) = 1.3V + n(5.5V - 1.3V)/127 \text{ ; for } 0 \leq n \leq 127$$

For reliable operation of the battery detection circuitry, the minimum value of V_{OC} should be greater than the maximum battery voltage.

THEVENIN RESISTANCE FIELD

The Thevenin resistance field specifies the value of output resistance between the low impedance V_{OC} source and the battery pin. This resistance can have one of 128 values ranging from 5060Ω to 7.5Ω with a 5% difference in successive values. This field is entered as a 7–bit binary value, LSB first. The value of $R_{TH}(n)$ is determined as follows:

$$R_{TH}(n) = 7.5(0.95^{n-127}) \text{ ; for } 0 \leq n \leq 127$$

PULSE WIDTH FIELD

The pulse width field specifies the amount of time (PW) during each eight second charging and evaluation cycle that V_{OC} and R_{TH} will be applied after the optional timer has expired. PW can have one of 8 values ranging from 8 seconds to 0. The field is entered as a 3–bit binary value, LSB first. The value of PW is determined as follows:

$$PW(n) = 2^n/16 \text{ ; for } 1 \leq n \leq 7$$

$$PW(n) = 0 \text{ ; for } n = 0$$

CHARGE ON FIELD

This is a one bit field which specifies if V_{OC} and R_{TH} for this breakpoint are to be applied at all for the case of an unexpired timer. Its usefulness is in permitting certain breakpoints to be turned off if the battery voltage exceeds a maximum during standard charge. If the timer has expired or is not used, this is accomplished for those breakpoints using the 3 pulse width bits (PW = 000).

A one in this field means that the V_{OC} and R_{TH} are to be applied when the breakpoint is the current one.

CONFIGURATION REGISTER STRUCTURE

V_{TRIP} Field

This is a one–bit field which specifies the valid supply voltage for the device. A one in this field indicates a 6V system is being used and the part will not begin charging until the applied V_{CC} exceeds 5.7V. Conversely, a zero indicates a 5V system and charging will begin when V_{CC} exceeds 4.75V.

TIMER STATUS FIELD

This is a one bit field which indicates if the timer is to be used. A one in this field indicates that timer is used, a zero that it is not.

TIMER VALUE FIELD

This field specifies the maximum time (T_{MAX}) for standard or non–pulsed charging. During the period when the timer has not expired, V_{OC} and R_{TH} will be applied to the battery input if the charge on bit is a one. When the elapsed charge time exceeds the value in this register, V_{OC} and R_{TH} will be applied at a duty cycle determined by the PW field for each breakpoint. The field is entered as a 4–bit binary value, LSB first. The timer can have values from 2 to 32 hours, determined by the following:

$$T_{MAX}(n) = 2(n + 1) \text{ ; for } 0 \leq n \leq 15$$

PROGRAMMING OPERATION

The data for the 33 registers is stored in nonvolatile memory and can be written only once. All 33 registers must be programmed before any can be read. Note that although the configuration register contains only 6 bits, 25 bits are required to be entered; therefore, fill it with 19 0's. The registers are programmed sequentially, starting at register 0. As each register is programmed, an internal pointer moves to the next register until all 33 have been programmed. To enter the program/read mode, V_{CC} must be taken to 8V for a minimum of 1 ms and returned to 5V. The V_{BAT} pin is now configured to operate as a single wire I/O line. The hardware interface is shown in Figure 3.

RESET TIMING

To issue a reset to the device the V_{BAT} pin must be brought low and held low for a minimum of 480 µs after which it is released and will return to a high level through the internal pullup resistor. After the line is allowed to return high it must not be pulled low for at least 1 µs. Refer to Figure 4.

WRITE TIMING

A logic 0 is written by bringing the V_{BAT} pin low for at least 60 µs, but not more than 120 µs. A logic 1 is written by bringing the V_{BAT} pin low for at least 1 µs, but not more than 15 µs. After the line is allowed to return high it must not be pulled low for at least 60 µs. Refer to Figure 4.

READ TIMING

A read is performed by bringing the V_{BAT} pin low for at least 1 µs, but not more than 5 µs and then releasing it. A logic 1 is indicated by the pin returning high. The state of the V_{BAT} pin should be sampled at most 15 µs after V_{BAT} is pulled low. A high level indicates a read '1', a low level indicates a read '0'.

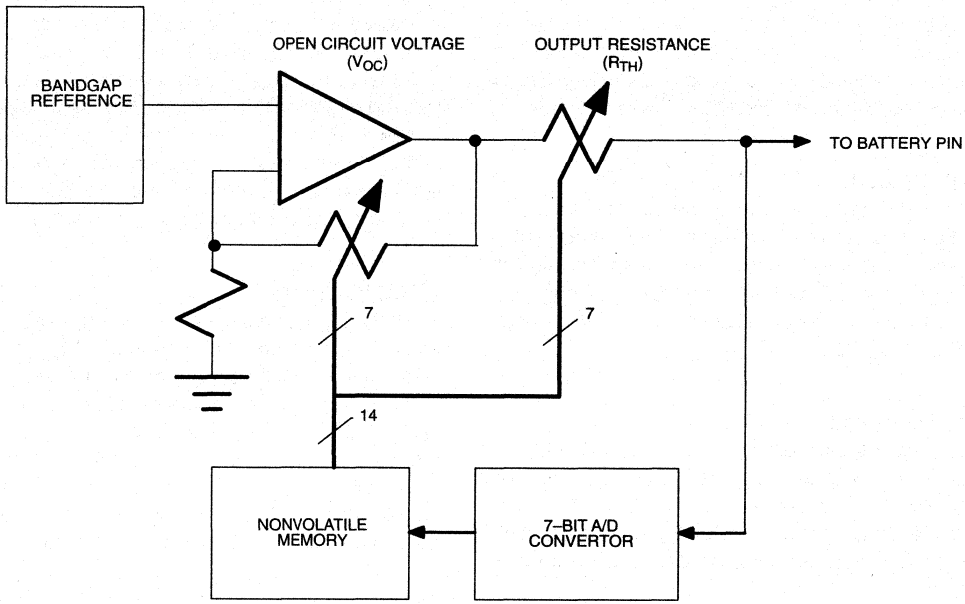
PROGRAMMING

To program the DS1633 the single line I/O must be enabled by bringing V_{CC} to 8V for at least 1 ms and then back to 5V. The first register can now be written. The register data must be preceded by 3 consecutive logic 1 write cycles. The register data can now be entered according to the write cycle timing detailed above, from LSB to MSB. To commit the data to the nonvolatile memory the V_{BAT} pin is brought to 12V, with V_{CC} at 8V, for at least 250 ms. When V_{BAT} is released and returns to 5V and a reset cycle is issued the device is ready for the next register. Be careful not to issue multiple resets as this will move the pointer. This sequence is repeated until all 33 registers are programmed. When all registers have been programmed, the DS1633 disables the serial interface and begins normal operation.

VERIFICATION

To verify the data contained in the registers the single line I/O must be enabled by bringing V_{CC} to 8V for at least 1 ms. Unlike the programming operation, the read operation allows random access of the registers. A read cycle is preceded by 4 logic ones, a 6–bit register address, entered LSB first, and 18 logic ones. The device will now output the contents of the register, LSB first, on the next 25 read cycles. To read another register, issue a reset and repeat the sequence.

SIMPLIFIED BLOCK DIAGRAM Figure 1

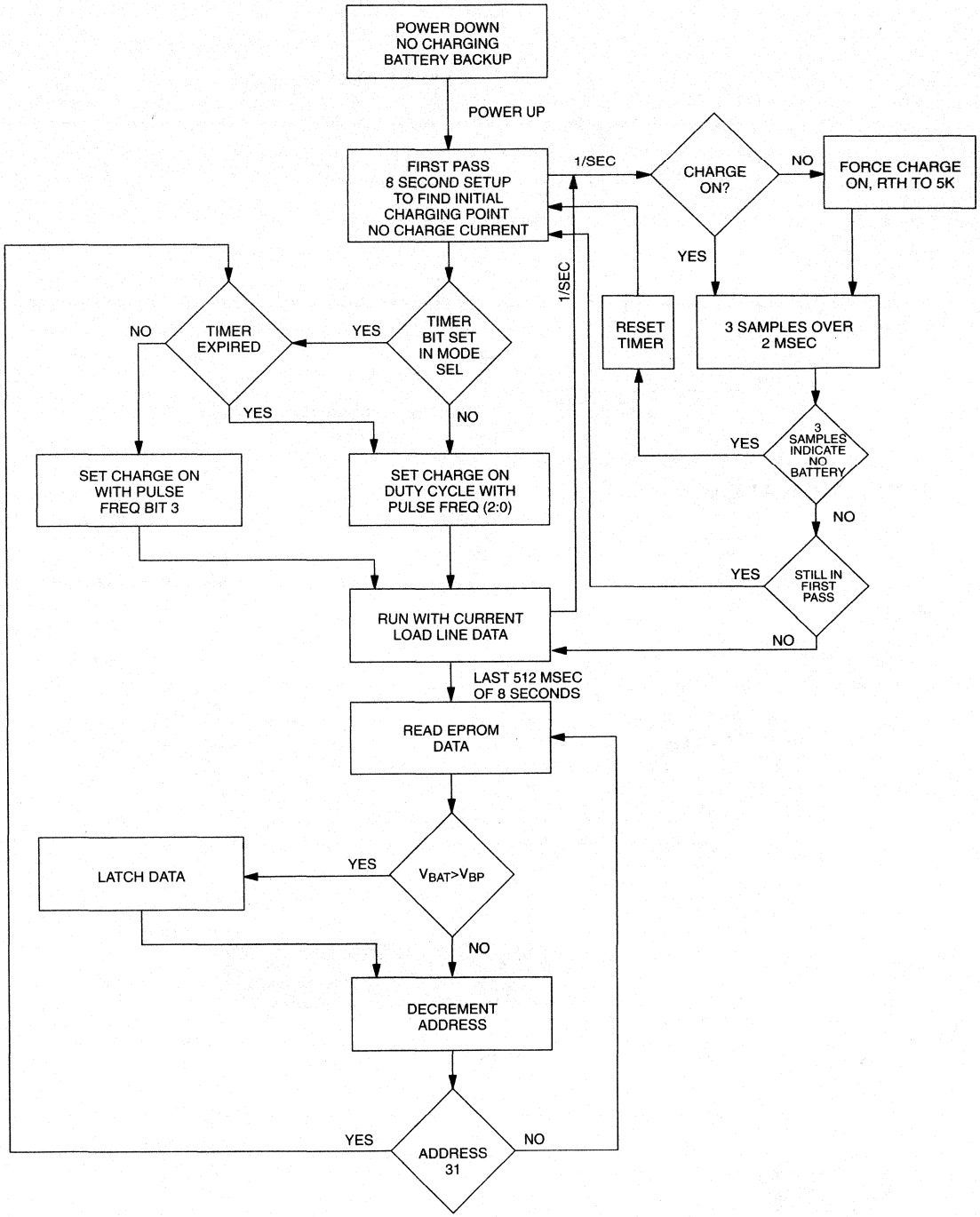


DS1633 REGISTER STRUCTURE Table 1

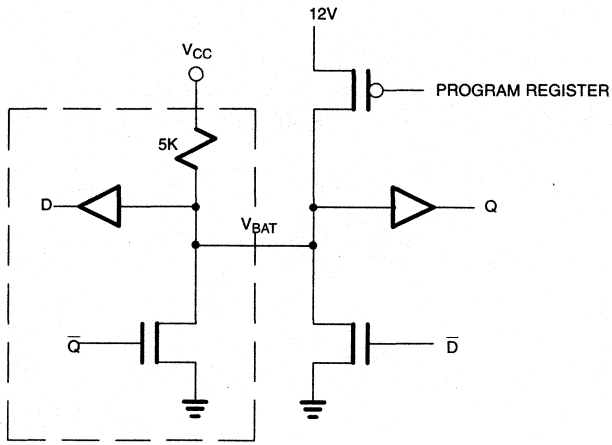
MSB **DS1633 MEMORY ARRAY MAP** **LSB**

REGISTER	CHARGE ON	PULSE WIDTH	THEVENIN RESISTANCE FIELD	OPEN CIRCUIT VOLTAGE	BREAKPOINT VOLTAGE		
0	CO_0	PW_0	R_{TH0}	V_{OC0}	V_{BP0}		
1							
2							
3							
•							
•							
•							
30							
31	CO_{31}	PW_{31}	R_{TH31}	V_{OC31}	V_{BP31}		
32	MUST FILL UNUSED BITS WITH 0'S				TIMER VALUE	TIMER STATUS	V_{TRIP}

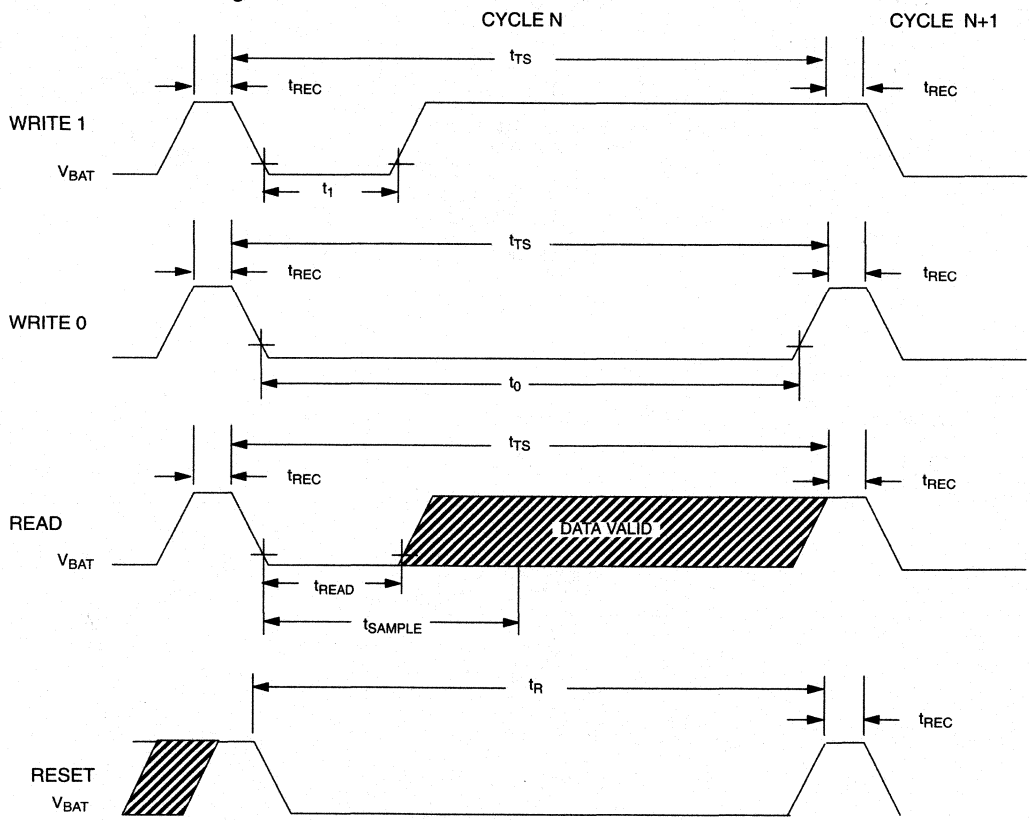
DS1633 OPERATION FLOW CHART Figure 2



HARDWARE INTERFACE FOR PROGRAMMING Figure 3



I/O SIGNAL TIMING Figure 4



REGISTER VALUE CROSS REFERENCE Table 2

HEX	DEC	R_{TH}	V_{OC}	V_{BP}
00	0	5.060E+03	1.30	0.000
01	1	4.807E+03	1.33	0.037
02	2	4.567E+03	1.37	0.074
03	3	4.338E+03	1.40	0.111
04	4	4.122E+03	1.43	0.148
05	5	3.915E+03	1.47	0.185
06	6	3.720E+03	1.50	0.222
07	7	3.534E+03	1.53	0.259
08	8	3.357E+03	1.56	0.296
09	9	3.189E+03	1.60	0.333
0A	10	3.030E+03	1.63	0.370
0B	11	2.878E+03	1.66	0.407
0C	12	2.734E+03	1.70	0.444
0D	13	2.598E+03	1.73	0.481
0E	14	2.468E+03	1.76	0.518
0F	15	2.344E+03	1.80	0.555
10	16	2.227E+03	1.83	0.592
11	17	2.116E+03	1.86	0.629
12	18	2.010E+03	1.90	0.666
13	19	1.909E+03	1.93	0.703
14	20	1.814E+03	1.96	0.740
15	21	1.723E+03	1.99	0.777
16	22	1.637E+03	2.03	0.814
17	23	1.555E+03	2.06	0.851
18	24	1.478E+03	2.09	0.888
19	25	1.404E+03	2.13	0.925
1A	26	1.333E+03	2.16	0.962
1B	27	1.267E+03	2.19	0.999
1C	28	1.203E+03	2.23	1.036
1D	29	1.143E+03	2.26	1.073
1E	30	1.086E+03	2.29	1.110
1F	31	1.032E+03	2.33	1.147
20	32	9.802E+02	2.36	1.184
21	33	9.312E+02	2.39	1.221
22	34	8.846E+02	2.42	1.258
23	35	8.404E+02	2.46	1.295
24	36	7.984E+02	2.49	1.332
25	37	7.585E+02	2.52	1.369
26	38	7.205E+02	2.56	1.406
27	39	6.845E+02	2.59	1.443
28	40	6.503E+02	2.62	1.480
29	41	6.178E+02	2.66	1.517
2A	42	5.869E+02	2.69	1.554
2B	43	5.575E+02	2.72	1.591
2C	44	5.297E+02	2.76	1.628
2D	45	5.032E+02	2.79	1.665
2E	46	4.780E+02	2.82	1.702
2F	47	4.541E+02	2.85	1.739
30	48	4.314E+02	2.89	1.776
31	49	4.098E+02	2.92	1.813
32	50	3.894E+02	2.95	1.850
33	51	3.699E+02	2.99	1.887
34	52	3.514E+02	3.02	1.924
35	53	3.338E+02	3.05	1.961
36	54	3.171E+02	3.09	1.998
37	55	3.013E+02	3.12	2.035
38	56	2.862E+02	2.15	2.072
39	57	2.719E+02	3.19	2.109
3A	58	2.583E+02	3.22	2.146
3B	59	2.454E+02	3.25	2.183
3C	60	2.331E+02	3.28	2.220
3D	61	2.215E+02	3.32	2.257
3E	62	2.104E+02	3.35	2.294
3F	63	1.999E+02	3.38	2.331
40	64	1.899E+02	3.42	2.368
41	65	1.804E+02	3.45	2.405
42	66	1.714E+02	3.48	2.442
43	67	1.628E+02	3.52	2.479
44	68	1.547E+02	3.55	2.516
45	69	1.469E+02	3.58	2.553
46	70	1.396E+02	3.61	2.590
47	71	1.326E+02	3.65	2.627
48	72	1.260E+02	3.68	2.664
49	73	1.197E+02	3.71	2.701
4A	74	1.137E+02	3.75	2.738
4B	75	1.080E+02	3.78	2.775

HEX	DEC	R_{TH}	V_{OC}	V_{BP}
4C	76	1.026E+02	3.81	2.812
4D	77	9.747E+01	3.85	2.849
4E	78	9.260E+01	3.88	2.886
4F	79	8.797E+01	3.91	2.923
50	80	8.357E+01	3.95	2.960
51	81	7.939E+01	3.98	2.997
52	82	7.542E+01	4.01	3.034
53	83	7.165E+01	4.04	3.071
54	84	6.807E+01	4.08	3.108
55	85	6.467E+01	4.11	3.145
56	86	6.143E+01	4.14	3.182
57	87	5.836E+01	4.18	3.219
58	88	5.544E+01	4.21	3.256
59	89	5.267E+01	4.24	3.293
5A	90	5.004E+01	4.28	3.330
5B	91	4.753E+01	4.31	3.367
5C	92	4.516E+01	4.34	3.404
5D	93	4.290E+01	4.38	3.441
5E	94	4.076E+01	4.41	3.478
5F	95	3.873E+01	4.44	3.515
60	96	3.678E+01	4.47	3.552
61	97	3.494E+01	4.51	3.589
62	98	3.320E+01	4.54	3.626
63	99	3.154E+01	4.57	3.663
64	100	2.996E+01	4.61	3.700
65	101	2.846E+01	4.64	3.737

HEX	DEC	R_{TH}	V_{OC}	V_{BP}
66	102	2.704E+01	4.67	3.774
67	103	2.569E+01	4.71	3.811
68	104	2.440E+01	4.74	3.848
69	105	2.318E+01	4.77	3.885
6A	106	2.202E+01	4.81	3.922
6B	107	2.092E+01	4.84	3.959
6C	108	1.988E+01	4.87	3.996
6D	109	1.888E+01	4.90	4.033
6E	110	1.794E+01	4.94	4.070
6F	111	1.704E+01	4.97	4.107
70	112	1.619E+01	5.00	4.144
71	113	1.538E+01	5.04	4.181
72	114	1.461E+01	5.07	4.218
73	115	1.388E+01	5.10	4.255
74	116	1.319E+01	5.14	4.292
75	117	1.253E+01	5.17	4.329
76	118	1.190E+01	5.20	4.366
77	119	1.131E+01	5.24	4.403
78	120	1.074E+01	5.27	4.440
79	121	1.020E+01	5.30	4.477
7A	122	9.693E+00	5.33	4.514
7B	123	9.208E+00	5.37	4.551
7C	124	8.748E+00	5.40	4.588
7D	125	8.310E+00	5.43	4.625
7E	126	7.895E+00	5.47	4.662
7F	127	7.500E+00	5.50	4.699

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
5V Mode Supply Voltage, Operation	V_{CC1}	4.75	5	6.5	V	1,2
6V Mode Supply Voltage, Operation	V_{CC2}	5.7	6	6.5	V	1,3,4
Supply Voltage, V_{BAT}, Programming	V_{BATP}	12	12	13	V	
I_{BAT}, Programming	I_{BATP}			100	µA	
V_{CC} Supply Voltage, Programming	V_{CC3}	8		8.5	V	
Logic 1 Input	V_{IH}	2.0	–	V_{CC}+0.3	V	
Logic 0 Input	V_{IL}	–0.3	–	+0.8	V	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5.75V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current, Operation Mode	$I_{CC1,2}$			1	mA	6
Supply Current, Programming Mode	I_{CC3}			10	mA	
Output Low, Voltage	V_{OL}			0.4	V	
Output Low, Current	I_{OL}	1			mA	
V_{BAT} Leakage Current with V_{CC} at 0V	I_{BAT}			100	nA	5
Pullup resistance on I/O	R_{PU}		5K			
Breakpoint Voltage (n=0)	$V_{BP}(0)$		0		V	
Breakpoint Voltage (n=127)	$V_{BP}(127)$	4.649	4.699	4.749	V	
Open Circuit Voltage (n=0)	$V_{OC}(0)$		1.3		V	
Open Circuit Voltage (n=127)	$V_{OC}(127)$	5.45	5.50	5.55	V	
Thevenin Resistance (n=0)	$R_{TH}(0)$		7.5		Ω	7
Thevenin Resistance (n=127)	$R_{TH}(127)$	4933	5060	5187	Ω	7
Timer Value (n=0)	$T_{MAX}(0)$	1.8	2	2.2	hours	
Timer Value (n=15)	$T_{MAX}(127)$	28.8	32	35.2	hours	

AC ELECTRICAL CHARACTERISTICS: DATA TRANSMISSION PARAMETERS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Reset Active	t_R	480			µs	
Logic 1 Active Low	t_1	1		15	µs	
Logic 0 Active Low	t_0	60		120	µs	
Read Enable Time	t_{READ}	1		5	µs	
Time from Read Enable to I/O Line Sampling	t_{SAMPLE}			15	µs	
Data Transfer Window	t_{TS}	60		120	µs	
Active Signal Pulse Width, Data I/O	t_{PW}	60		120	µs	
Recovery Time Between Windows	t_{REC}	1			µs	
Programming Pulse Width, V_{BAT}	t_{PRG}	250			ms	

NOTES:

1. All voltages referenced to ground.
2. 5V operation conditions.
3. 6V operation conditions.
4. For any $V_{OCMAX} \geq 4.5V$, $V_{TRIP} = 5.7V$ (6V operation) must be used.
5. High impedance isolation between V_{BAT} and V_{CC} with $V_{CC}=0$ is $\geq 45G\Omega$.
6. Does not include current supplied to the battery pin.
7. At 25°C, R_{TH} has a positive temperature coefficient of approximately 800 ppm/°C.

DALLAS SEMICONDUCTOR

DS1633x
High–Speed Battery Charger

1

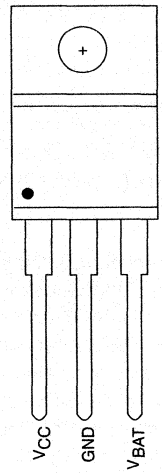
FEATURES

- Preprogrammed versions of DS1633
- Recharges lithium, NiCad, and lead acid batteries
- Retains battery and power supply limits in onboard memory
- Timer–terminated standard charge followed by trickle charge
- 3-pin TO–220 package
- Operating range 0 to 70°C
- Applications include consumer electronics, portable/ cellular phones, pagers, medical instruments, backup memory systems, security systems
- Available in six different preprogrammed variations to meed the needs of 3–cell NiCad battery packs

PRODUCT SELECTION GUIDE Table 1

PART NUMBER	I_{MAX} (mA)	V_{MAX} (V)	TIMER (hours)
DS1633–A	100	4.65	8
DS1633–B	80	4.65	8
DS1633–C	60	4.65	8
DS1633–D	40	4.65	8
DS1633–E	20	4.65	8

PIN ASSIGNMENT TO–220



See Mech. Drawings Section

PIN DESCRIPTION

V_{CC}	Input Voltage, +
V_{BAT}	Battery Voltage Input, +
GND	Ground

DESCRIPTION

The DS1633x High–Speed Battery Recharger automatically provides a constant current recharge to a battery as long as the battery's voltage is below the specified maximum voltage. The DS1633x charges the battery using its V_{CC} input as a source. When V_{CC} is floated, the DS1633x is dormant. When V_{CC} is reapplied, the DS1633x begins charging.

Although a variety of load curves can be used to charge a battery, most do not take advantage of the fact that a battery can accept its maximum current rating for charging purposes over its entire voltage range. The DS1633x takes advantage of this opportunity by constantly readjusting the current supplied to the battery being charged. As the voltage level of the battery being charged rises, and the supply current drops, the DS1633x adjusts to boost the charging current back to its maximum.

111192 1/5

This feature greatly decreases the recharge time required to fully charge a lithium, NiCad, or lead acid type cell.

The DS1633x provides a designer with the ability to use an optimized battery load line by selecting a preprogrammed DS1633x from Dallas Semiconductor. Refer to Table 1 to assist in the selection of the appropriate device. Each DS1633x is designed to constantly adjust the open circuit voltage and supply current to regulate the current flow to the battery being charged. As the battery is being charged, its voltage is being measured. When the voltage has reached a factory-defined voltage breakpoint on its load line, the open circuit voltage and supply current are modified according to the factory pre–set values. The DS1633x uses these new values until the next breakpoint is reached, allowing more adjustments.

The DS1633x Current Supply Diagram and Traditional Battery Charge Load Line illustrate this concept and how it differs from an non–controlled recharge. In the traditional resistor limited battery charge load line (Figure 1), a battery has a specified maximum current and voltage at which it may be recharged. A charging voltage source begins charging the dead or near zero voltage battery at its maximum current rating. As the battery begins to charge, and its voltage increases, the voltage difference across the resistor begins to diminish, decreasing the current supplied to the battery. This costs time because the battery is being charged at a slower rate as time goes on. The DS1633x circumvents this deficiency by modifying the load curve to be pseudo–constant current (Figure 2). Rather than using a very steep load line which terminates at the open circuit voltage of the battery to be charged, the DS1633x uses a shallow load curve, which intersects the voltage axis well beyond the maximum voltage of the battery being charged. The net effect produced is that when the battery is at a very low voltage, it will receive its maximum current at an open circuit charge voltage significantly higher than its rated supply. As the battery being charged begins to gain voltage the load line will begin to reduce the current the battery is receiving to less than its maximum acceptable rate. By periodically decreasing the value of R_N, the current flow between V_{CC} and the battery is increased to compensate for the increase in battery voltage.

OPERATION

Upon power–up, the DS1633x does a dummy cycle of eight seconds with the charge current set to 0 to determine where to start the charging curve. In normal operation the part measures the battery voltage every eight seconds to find what V_{OC}, R_{TH}, and charging duty cycle should be applied to the battery. This continues as long as V_{CC} is greater than 5.7V.

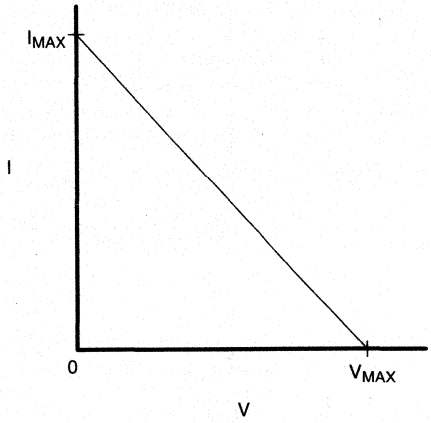
Figure 3, the DS1633x Operational Flow Chart, shows how the DS1633x functions as it charges a battery. The charging termination methods available in the DS1633x are charging time and maximum battery voltage. Each DS1633x when programmed retains the maximum charging current and maximum charge voltage limit of the battery pack according to Table 1. The packs trickle charge requirements is also retained. Lastly, the DS1633x maintains an internal timebase of how long it has been charging a given battery pack, and will terminate high current charging if the maximum allowable time has been exceeded. DS1633's are capable of charging single rechargeable lithium 3.0V cells, or from 1 to 3 Nicad cells (usually 1.55V max/cell) at a maximum current of 100 mA.

The DS1633 is suited for charging a variety of rechargeable lithium chemistry and NiCad chemistry batteries. In order to make implementation as easy as possible, Dallas Semiconductor offers DS1633x's preprogrammed to meet the charging requirements of a variety of industry standard 3–cell pack NiCad batteries.

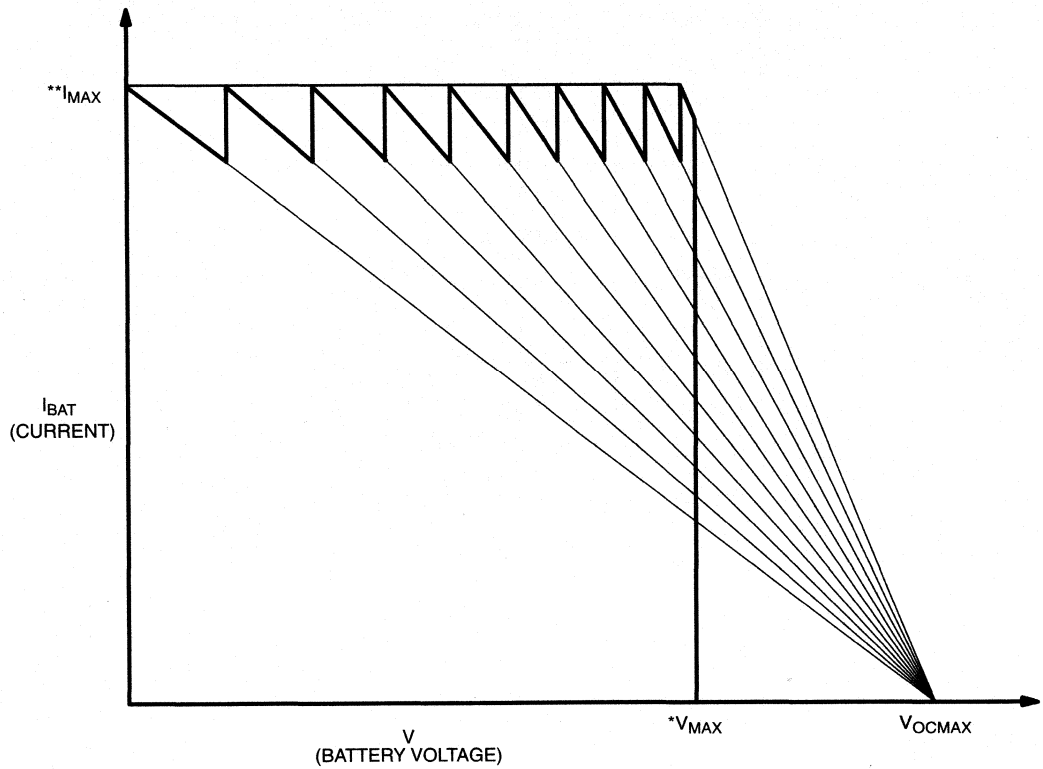
If you would like to create your own load line and test it in DS1633x's, you may purchase a DS1633K kit from Dallas Semiconductor. The kit contains unprogrammed or "blank" DS1633x's, DOS software for helping generate and test your load line in a mouse driven environment, and the necessary interface hardware for taking your unique load line requirement and programming DS1633x's directly through an IBM personal computer serial port.

If you choose to purchase a kit, decide upon a load line, and want to program parts yourself, you can purchase "blank" DS1633x's from Dallas Semiconductor and program your own.

TRADITIONAL BATTERY CHARGE LOAD LINE Figure 1



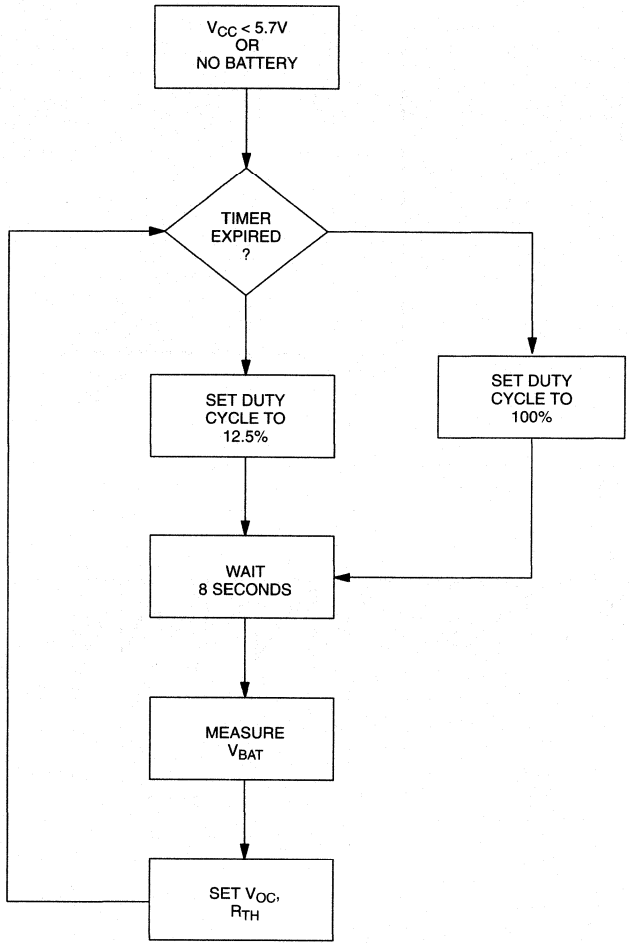
MAXIMUM CURRENT LOAD LINE Figure 2



*The vertical line marked V_{MAX} represents the maximum voltage which the battery may accept.

** The horizontal line marked I_{MAX} represents the maximum current which the battery may accept.

DS1633x OPERATION FLOW CHART Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1V to +7.0V
Operating Temperature	0°C to +70°C
Storage Temperature	–55°C to 125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS

(0°C to+70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	5.7	6.0	6.5	V	

DC ELECTRICAL CHARACTERISTICS

(0°C to +70°C; V_{CC} ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Battery Charge Current	I_{BAT}				mA	
DS1633–A		90	100	110		
DS1633–B		72	80	88		
DS1633–C		54	60	66		
DS1633–D		36	40	44		
DS1633–E		18	20	22		
Supply Current	I_{CC}			I_{BAT} + 2	mA	
Charge Cutoff Voltage	V_{MAX}	4.50	4.65	4.80	V	
Battery Leakage Current	I_{LKG}			100	nA	1

AC ELECTRICAL CHARACTERISTICS

(0°C to +70°C; V_{CC} ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Standard Charge TIme Limit	t_{CHG}	7.2	8.0	8.8	hours	
Trickle Charge Duty Cycle		12.5			%	

NOTE:

1. V_{CC} = 0V.

PRELIMINARY

DALLAS SEMICONDUCTOR

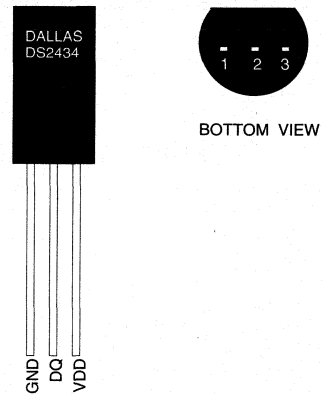
DS2434
Battery Identification Chip

FEATURES

- Provides unique ID number to battery packs
- Eliminates thermistors by sensing battery temperature on–chip
- 256–bit nonvolatile user memory available for storage of user data such as gas gauge and manufacturing information.
- Operating range of –40°C to +85°C
- Applications include portable computers, portable/cellular phones, consumer electronics, and handheld instrumentation.

PACKAGE OUTLINE

PR–35 PACKAGE



See Mech. Drawings Section

PIN DESCRIPTION

GND	–	Ground
DQ	–	Data In/Out
V_{DD}	–	Supply Voltage

DESCRIPTION

The DS2434 Battery Identification Chip provides a convenient method of tagging and identifying battery packs by manufacturer, chemistry, or other identifying parameters. The DS2434 allows the battery pack to be coded with a unique identification number, and also store information regarding the battery life and charge/discharge characteristics in its nonvolatile memory.

The DS2434 also performs the essential function of monitoring battery temperature, without the need for a thermistor in the battery pack.

Information is sent to/from the DS2434 over a 1–wire interface, so that battery packs need only have three output connectors; power, ground, and the 1–wire interface.

DETAILED PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	GND	**Ground pin.**
2	DQ	**Data Input/Output pin** for 1–wire communication port.
3	V_{DD}	**Supply pin** – input power supply.

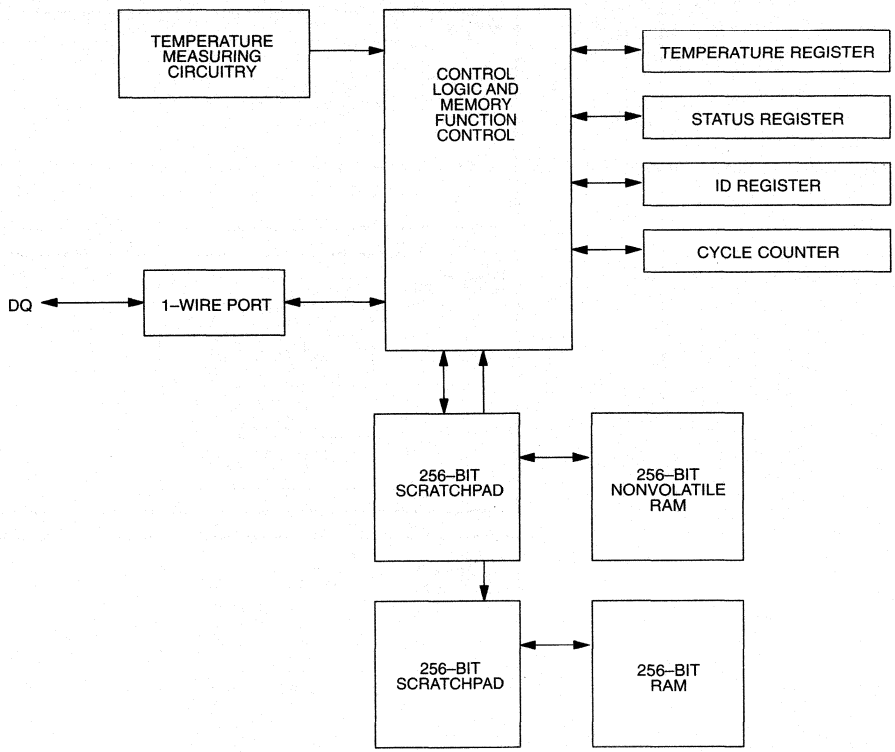
2

OVERVIEW

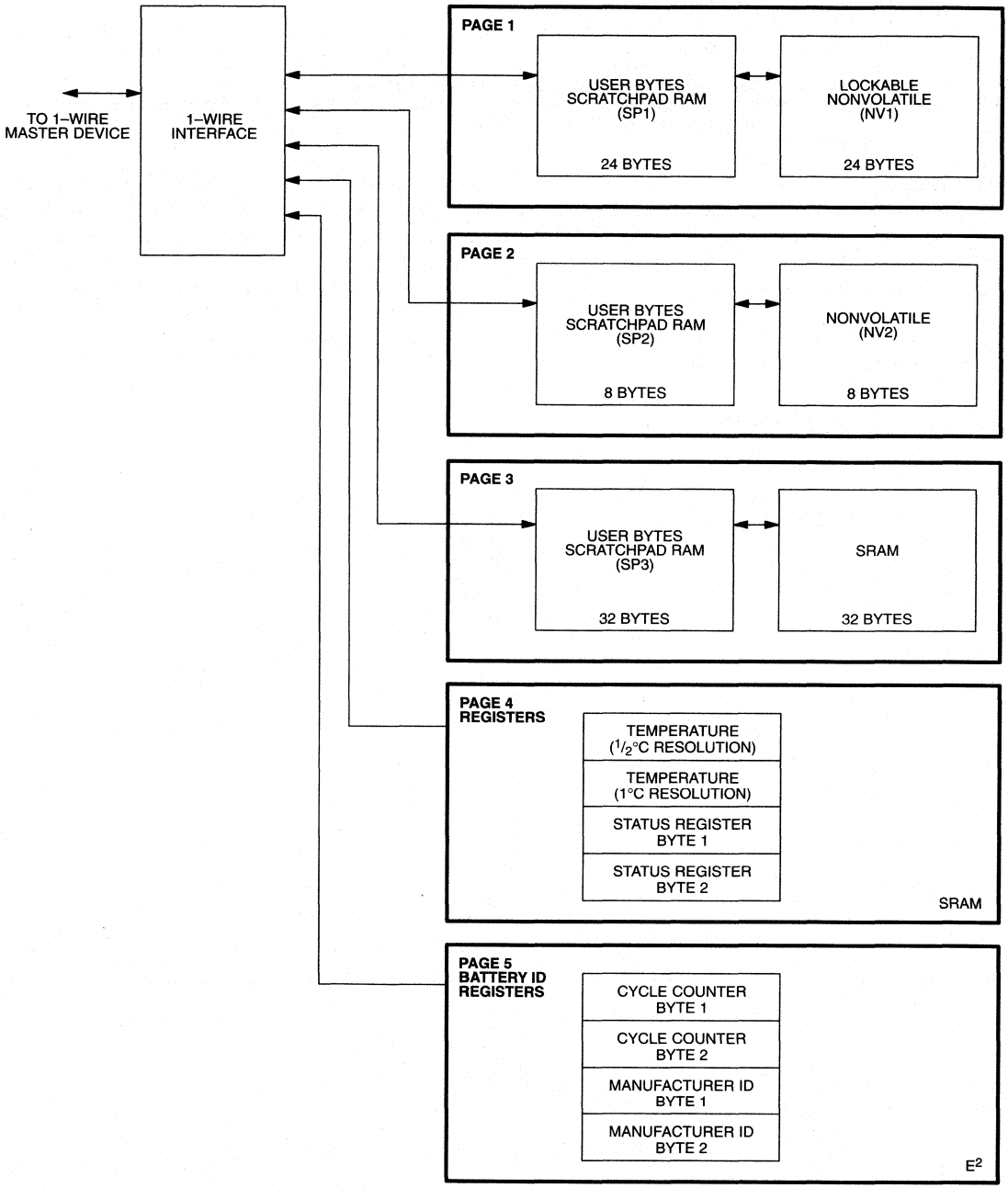
The DS2434 has five major components: 1) Scratchpad Memory, 2) Nonvolatile Memory, 3) On–board SRAM, 4) Temperature Sensor, and 5) ID Register. All data is read and written least significant bit first.

Access to the DS2434 is over a 1–wire interface. Charging parameters and other data such as battery chemistry, gas gauge information, and other user data would be stored in the DS2434, allowing this information to be permanently stored in the battery pack. Nonvolatile (E^2) RAM holds information even if the battery goes dead; as long as the battery remains within typical charge/discharge operating range, the SRAM provides battery–backed storage of information.

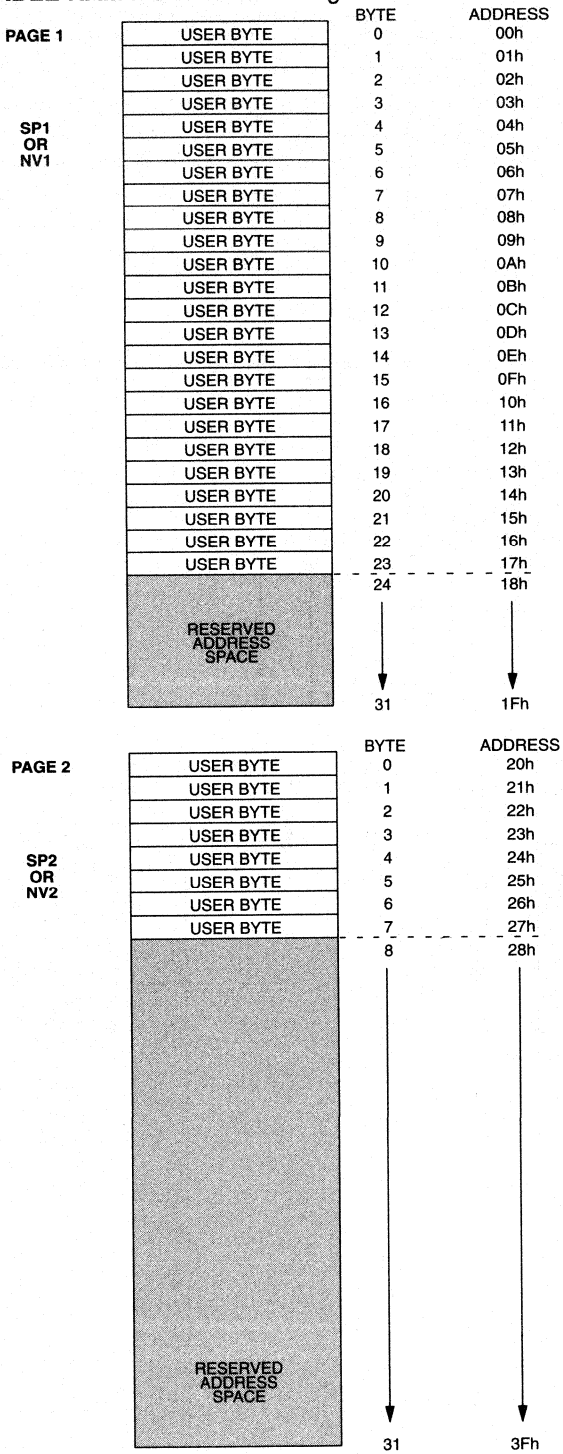
DS2434 BLOCK DIAGRAM Figure 1



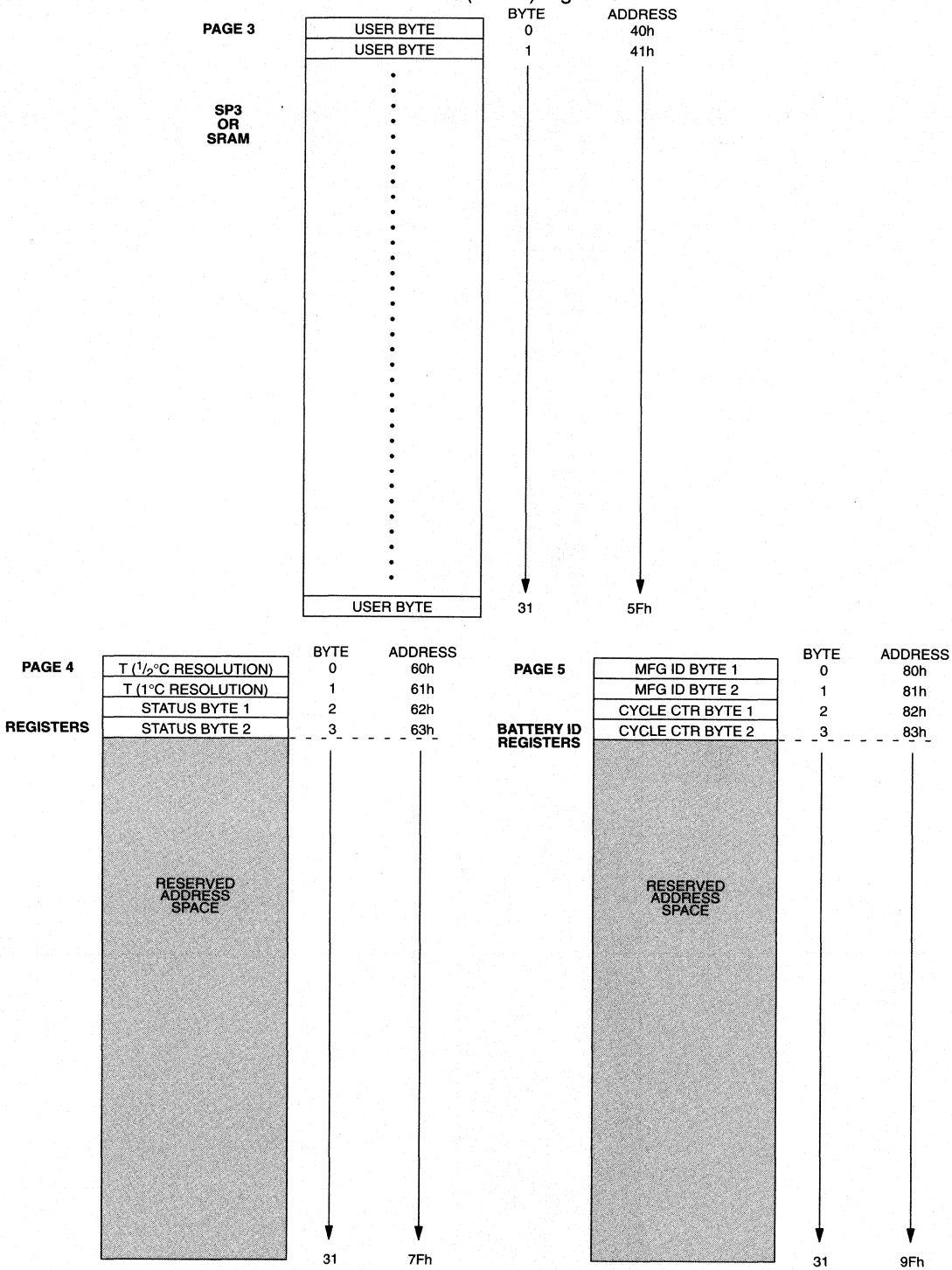
DS2434 MEMORY PARTITIONING Figure 2



DS2434 ADDRESSABLE RAM MEMORY MAP Figure 3



DS2434 ADDRESSABLE RAM MEMORY MAP (cont'd) Figure 3



MEMORY

The DS2434's memory is divided into five pages, each page filling 32 bytes of address space. Not all of the available addresses are used, however. Refer to the memory map of Figure 3 to see actual addresses which are available for use.

The first three pages of memory consist of a scratchpad RAM and then either a nonvolatile RAM (pages 1 and 2) or SRAM (page 3). The scratchpads help insure data integrity when communicating over the 1–wire bus. Data is first written to the scratchpad where it can be read back. After the data has been verified, a copy scratchpad command will transfer the data to the RAM (NV or SRAM). This process insures data integrity when modifying the memory.

The fourth page of memory consists of registers which contain the measured temperature value and status registers for the device; these registers are made from SRAM cells.

The fifth page of memory holds the ID number for the device and the cycle count registers in E^2 RAM, making these registers nonvolatile under all power conditions.

PAGE 1

The first page of memory has 24 bytes. It consists of a scratchpad RAM and a nonvolatile (E^2) RAM. These 24 bytes may be used to store any data the user wishes; such as battery chemistry descriptors, manufacturing lot codes, gas gauge information, etc.

The nonvolatile portion of this page may be locked to prevent data stored here from being changed inadvertantly.

Both the nonvolatile and the scratchpad portions are organized identically, as shown in the memory map of Figure 3. In this page, these two portions are referred to as NV1 and SP1, respectively.

PAGE 2

The second page of memory has 8 bytes. It consists of a scratchpad RAM and a nonvolatile (E^2) RAM. These eight bytes may be used to store any data the user wishes, such as battery chemistry descriptors, manufacturing lot codes, gas gauge information, etc.

PAGE 3

The third page of memory has a full 32 bytes. It consists of a scratchpad RAM and an SRAM. This address space may be used to store any data the user wishes, provided that, should the battery go dead and power to the DS2434 is lost, this data may also be lost without serious repercussions. Data which must remain even if power to the DS2434 is lost should be placed in either Page 1 or Page 2.

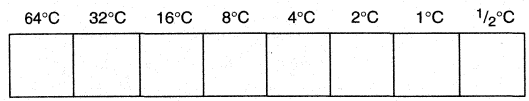
This section of memory may be used to store gas gauge and self discharge information. If the battery dies, and this information is lost, it is moot because the user can easily determine that the battery is dead.

PAGE 4

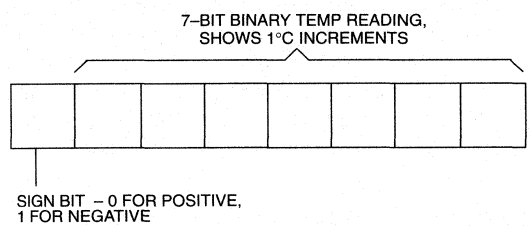
The fourth page of memory is used by the DS2434 to store the converted value of battery temperature. A two–byte status register is also provided.

TEMPERATURE REGISTERS (60h–61h)

The DS2434 can measure temperature without external components. The resulting temperature measurement is placed into two temperature registers. These registers are SRAM, and therefore will hold the values placed in them until the battery voltage falls below the minimum V_{DD} specified. The first register, at address 60h, provides $^1/_2$°C resolution for temperatures between 0°C and 127 $^1/_2$°C, formatted as follows:



The second register, at address 61h, provides 1°C resolution over the –40°C to +85°C range, formatted as follows in the binary two's complement coding.



STATUS/CONTROL REGISTER (62h–63h)

The status register is a two byte register at addresses 62h and 63h (consisting of SRAM). Address 62h is the least significant byte of the status register, and is currently the only address with defined status bits; the other byte at address 63h is reserved for future use. The status register is formatted as follows:

STATUS REGISTER

							LSB	
X	X	X	X	X	LOCK	NVB	TB	62h
X	X	X	X	X	X	X	X	63h

where

X = Don't Care

TB = Temperature Busy flag. "1" = temperature conversion in progress; "0" = temperature conversion complete, valid data in temperature register.

NVB = Nonvolatile memory busy flag. "1" = Copy from scratchpad to NVRAM in progress, "0" = nonvolatile memory is not busy. A copy to NVRAM may take from 2 ms to 10 ms (taking longer at lower supply voltages).

LOCK = NV1 Locked flag. "1" indicates that NV1 is locked; "0" indicates that NV1 is unlocked.

CYCLE COUNTER

MSB			BYTE 2				
32768	16384	8192	4096	2048	1024	512	256

83h

BYTE 1							LSB
128	64	32	16	8	4	2	0

82h

PAGE 5

The fifth page of memory holds the battery manufacturer ID number as well as a two–byte counter for counting the number of battery charge/discharge cycles.

ID REGISTER (80h and 81h)

The ID Register is a 16–bit ROM register that can contain a unique identification code, if purchased from Dallas Semiconductor. This ID number is programmed by Dallas Semiconductor, is unchangeable, and is unique to each customer. This ID number may be used to assure that batteries containing a DS2434 have the same manufacturer ID number as a charger configured to operate with that battery pack. This feature may be used to prevent charging of batteries for which the charging circuit has not been designed.

CYCLE COUNTER (82h and 83h)

The cycle counter register gives an indication of the number of charge/discharge cycles the battery pack has been through. This nonvolatile (E^2) register is incremented by the user through the use of a protocol to the DS2434, and is reset by another protocol. The counter is a straight binary counter, formatted as follows:

MEMORY FUNCTION COMMANDS

The protocols necessary for accessing the DS2434 are described in this section. Only these protocols may be written to the DS2434. Writing other protocols to the device may result in permanent damage to the part. These are summarized in Table 1, and examples of memory functions are provided in Tables 2 and 3.

PAGE 1 THROUGH PAGE 3 COMMANDS

Read Scratchpad [11h]

This command reads the contents of the scratchpad RAM on the DS2434. This command is followed by a start byte address. After issuing this command and providing the start address, the user may begin reading the data. The user may read data through the end of the scratchpad space (address 5Fh), with any reserved data bits reading all logic 1's and after which the data read will be all logic 1's.

Write Scratchpad [17h]

This command writes to the scratchpad RAM on the DS2434. This command is followed by a start byte address. After issuing this command and providing the start address, the user may begin writing data to the DS2434 scratchpad at the starting byte address.

Copy SP1 to NV1 [22h]
This command copies the entire contents (24 bytes) of Scratchpad 1 (SP1) to its corresponding nonvolatile memory (NV1). The nonvolatile RAM memory of the DS2434 cannot be written to directly by the bus master; however, the scratchpad RAM may be copied to the nonvolatile RAM. This prevents accidental overwriting of the nonvolatile RAM, and allows the data to be written first to the scratchpad, where it can be read back and verified before copying to the nonvolatile RAM. This command does not use a start address; the entire contents of the scratchpad will be copied to the nonvolatile RAM. The NVB bit will be set when the copy is in progress. NV1 is made with E^2 type memory cells that will accept at least 50000 changes.

Copy SP2 to NV2 [25h]
This command copies the entire contents (8 bytes) of SP2 (user bytes) to its corresponding nonvolatile memory (NV2). This command does not use a start address; the entire contents of SP2 will be copied to NV2. The NVB bit will be set when the copy is in progress. NV2 is made with E^2 type memory cells that will accept at least 50000 changes.

Copy SP3 to SRAM [28h]
This command copies the entire contents (32 bytes) of SP3 to its corresponding SRAM. This command does not use a start address; the entire contents of SP3 will be copied to the SRAM.

Copy NV1 to SP1 [71h]
This command copies the entire contents (24 bytes) of NV1 to its corresponding scratchpad RAM (SP1). This command does not use a start address; the entire contents of NV1 will be copied to SP1. The nonvolatile RAM memory of the DS2434 cannot be read directly by the bus master; however, the nonvolatile RAM may be copied to the scratchpad RAM.

Copy NV2 to SP2 [77h]
This command copies the entire contents (8 bytes) of NV2 (user bytes) to its corresponding scratchpad RAM (SP2). This command does not use a start address; the entire contents of NV2 will be copied to SP2. The nonvolatile RAM memory of the DS2434 cannot be read directly by the bus master; however, the nonvolatile RAM may be copied to the scratchpad RAM.

Copy SRAM to SP3 [7Ah]
This command copies the entire contents (32 bytes) of SRAM to its corresponding scratchpad RAM (SP3). This command does not use a start address; the entire contents of SRAM will be copied to SP3.The SRAM memory of the DS2434 cannot be read directly by the bus master; however, the SRAM may be copied to the scratchpad RAM.

Lock NV1 [43h]
This command prevents copying SP1 to NV1. This is done as an added measure of data security, preventing data from being changed inadvertently. NV1 may be copied up into SP1 while the part is locked. This allows NV1 to be read at any time. However, NV1 cannot be written to through a Copy SP1 to NV1 command without first unlocking the DS2434.

Unlock NV1 [44h]
This command unlocks NV1, to allow copying SP1 into NV1. This is done as an added measure of data security, preventing data from being changed inadvertently.

PAGE 4 AND 5 COMMANDS

Convert T [D2h]
This command instructs the DS2434 to initiate a temperature conversion cycle. This sets the TB flag. When the temperature conversion is done, the TB flag is reset and the current temperature value is placed in the temperature register. While a temperature conversion is taking place, all other memory functions are still available for use.

Read Registers [B2h]
This command reads the contents of the registers in Page 4 and 5. This command is followed by a start byte address. After issuing this command and providing the start address, the user may begin reading the data. The user may read data through the end of the register space (through address 63h in Page 4, address 83h in Page 5), after which the data read will be all logic 1's.

Increment Cycle [B5h]
This command increments the value in the cycle counter register. This command does not use a start address; no further data is required.

Reset Cycle Counter [B8h]
This command is used to reset the cycle counter register to zero, if desired.

DS2434 COMMAND SET Table 1

INSTRUCTION	DESCRIPTION	PROTOCOL	1–WIRE BUS MASTER STATUS AFTER ISSUING PROTOCOL	1–WIRE BUS DATA AFTER ISSUING PROTOCOL
PAGE 1 THROUGH PAGE 3 MEMORY COMMANDS				
Read Scratchpad	Reads bytes from DS2434 Scratchpad.	11h <addr (00h–5Fh)>	RX	<read data>
Write Scratchpad	Writes bytes to DS2434 Scratchpad.	17h <addr 00h–5Fh)>	TX	<write data>
Copy SP1 to NV1	Copies entire contents of SP1 to NV1.	22h	Idle	{NVB bit in Status Register=1 until copy complete (10ms, typ)}
Copy SP2 to NV2	Copies entire contents of SP2 to NV2.	25h	Idle	{NVB bit in Status Register=1 until copy complete (10ms, typ)}
Copy SP3 to SRAM	Copies entire contents of SP3 to SRAM.	28h	Idle	Idle
Copy NV1 to SP1	Copies entire contents of NV1 to SP1.	71h	Idle	Idle
Copy NV2 to SP2	Copies entire contents of NV2 to SP2.	77h	Idle	Idle
Copy SRAM to SP3	Copies entire contents of SRAM to SP3.	7Ah	Idle	Idle
Lock NV1	Locks 24 bytes of SP1 and NV1 from reading and writing.	43h	Idle	{NVB bit in Status Register=1 until copy complete (10ms, typ)}
Unlock NV1	Unlocks 24 bytes of SP1 and NV1 for reading and writing.	44h	Idle	{NVB bit in Status Register=1 until copy complete (10ms, typ)}
PAGE 4 AND PAGE 5 REGISTER COMMANDS				
Read Registers	Reads bytes from Temperature, Status and ID Registers.	B2h <addr (60h–63h, 80h–83h)>	RX	<read data>
Reset Cycle Counter	Resets cycle counter registers to zero.	B8h	Idle	{NVB bit in Status Register=1 until copy complete (10ms, typ)}
Increment Cycle Counter	Increments the value in the cycle counter register.	B5h	Idle	{NVB bit in Status Register=1 until copy complete (10ms, typ)}
Convert T	Initiates temperature conversion.	D2h	Idle	{TB bit in Status Register=1 until conversion complete}

MEMORY FUNCTION EXAMPLE Table 2
Example: Bus Master writes 24 bytes of data to DS2434 scratchpad, then copies to it to NV1.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480–960 µs)
RX	Presence	Presence pulse
TX	17h	Issue "write scratchpad" command
TX	00h	Start address
TX	<24 bytes>	Write 24 bytes of data to scratchpad
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	11h	Issue "read scratchpad" command
TX	00h	Start address
RX	<24 data bytes>	Read scratchpad data and verify
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	22h	Issue "copy SP1 to NV1" command
RX	<busy indicator>	Wait until NVB in status register=0 (10 ms typical)
TX	Reset	Reset pulse
RX	Presence	Presence pulse, done

MEMORY FUNCTION EXAMPLE Table 3
Example: Bus Master initiates temperature conversion, then reads temperature.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480–960 µs)
RX	Presence	Presence pulse
TX	D2h	Issue "convert T" command
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	B2h	Issue "read registers" command; begin loop
TX	62h	Status register address
RX	<1 data byte>	Read status register and loop until TB=0
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	B2h	Issue "read registers" command
TX	61h	Temperature register address
RX	<1 data byte>	Read temperature register
TX	Reset	Reset pulse
RX	Presence	Presence pulse, done

1–WIRE BUS SYSTEM

The DS2434 1–wire bus is a system which has a single bus master and one slave. The DS2434 behaves as a slave. The DS2434 is not able to be multidropped, unlike other 1–wire devices from Dallas Semiconductor.

The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1–wire signaling (signal types and timing).

HARDWARE CONFIGURATION

The 1–wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1–wire bus must have open drain or 3–state outputs. The 1–wire port of the DS2434 is open drain with an internal circuit equivalent to that shown in Figure 5. The 1–wire bus requires a pull–up resistor of approximately 5KΩ.

The idle state for the 1–wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 480 µs, all components on the bus will be reset.

TRANSACTION SEQUENCE

The protocol for accessing the DS2434 via the 1–wire port is as follows:

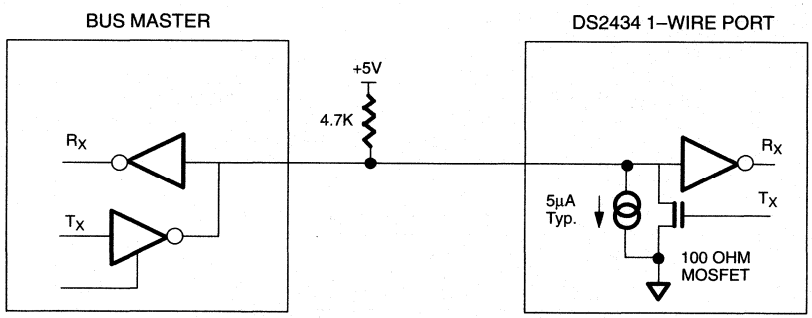
- Initialization
- Memory Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1–wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s).

The presence pulse lets the bus master know that the DS2434 is on the bus and is ready to operate. For more details, see the "1–Wire Signaling" section.

HARDWARE CONFIGURATION Figure 4



I/O SIGNALING

The DS2434 requires strict protocols to insure data integrity. The protocol consists of several types of signaling on one line: reset pulse, presence pulse, write 0, write 1, read 0, and read 1. All of these signals, with the exception of the presence pulse, are initiated by the bus master.

The initialization sequence required to begin any communication with the DS2434 is shown in Figure 5. A reset pulse followed by a presence pulse indicates the DS2434 is ready to send or receive data given the correct memory function command.

The bus master transmits (TX) a reset pulse (a low signal for a minimum of 480 µs). The bus master then releases the line and goes into a receive mode (RX). The 1–wire bus is pulled to a high state via the 5K pull–up resistor. After detecting the rising edge on the I/O pin, the DS2434 waits 15–60 µs and then transmits the presence pulse (a low signal for 60–240 µs).

READ/WRITE TIME SLOTS

DS2434 data is read and written through the use of time slots to manipulate bits and a command word to specify the transaction.

Write Time Slots

A write time slot is initiated when the host pulls the data line from a high logic level to a low logic level. There are two types of write time slots: Write One time slots and Write Zero time slots. All write time slots must be a minimum of 60 µs in duration with a minimum of a 1 µs recovery time between individual write cycles.

The DS2434 samples the I/O line in a window of 15 µs to 60 µs after the I/O line falls. If the line is high, a Write One occurs. If the line is low, a Write Zero occurs (see Figure 6).

For the host to generate a Write One time slot, the data line must be pulled to a logic low level and then released, allowing the data line to pull up to a high level within 15 µs after the start of the write time slot.

For the host to generate a Write Zero time slot, the data line must be pulled to a logic low level and remain low for the duration of the write time slot.

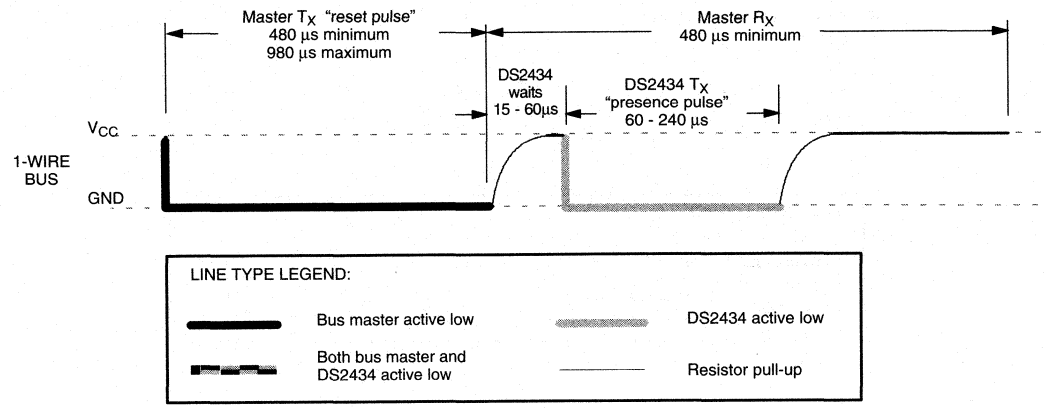
Read Time Slots

The host generates read time slots when data is to be read from the DS2434. A read time slot is initiated when the host pulls the data line from a logic high level to logic low level. The data line must remain at a low logic level for a minimum of 1 µs; output data from the DS2434 is then valid for the next 14 µs maximum. The host therefore must stop driving the I/O pin low in order to read its state 15 µs from the start of the read slot (see Figure 6). By the end of the read time slot, the I/O pin will pull back high via the external pull–up resistor. All read time slots must be a minimum of 60 µs in duration with a minimum of a 1 µs recovery time between individual read slots.

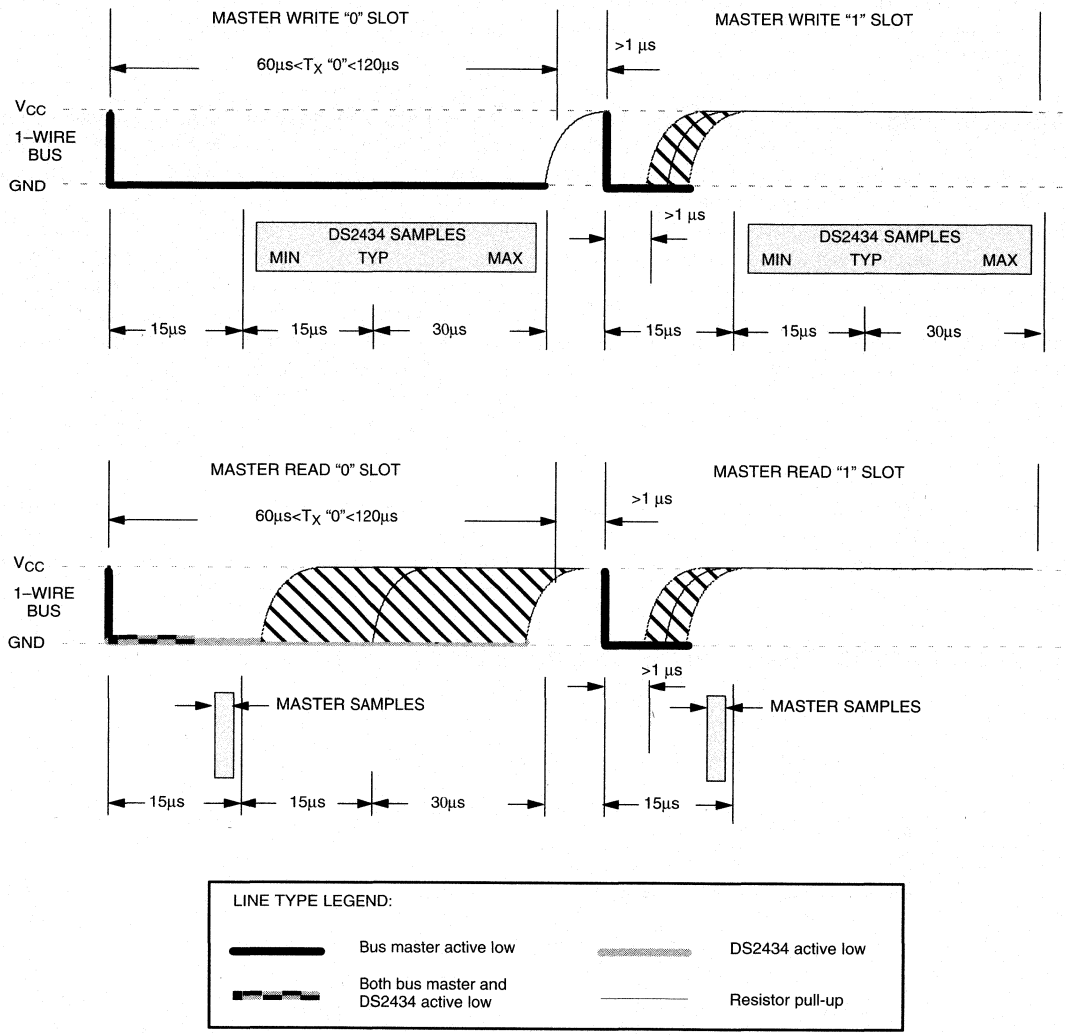
Figure 7 shows that the sum of T_{INIT}, T_{RC}, and T_{SAMPLE} must be less than 15 µs. Figure 9 shows that system timing margin is maximized by keeping T_{INIT} and T_{RC} as small as possible and by locating the master sample time towards the end of the 15 µs period.

2

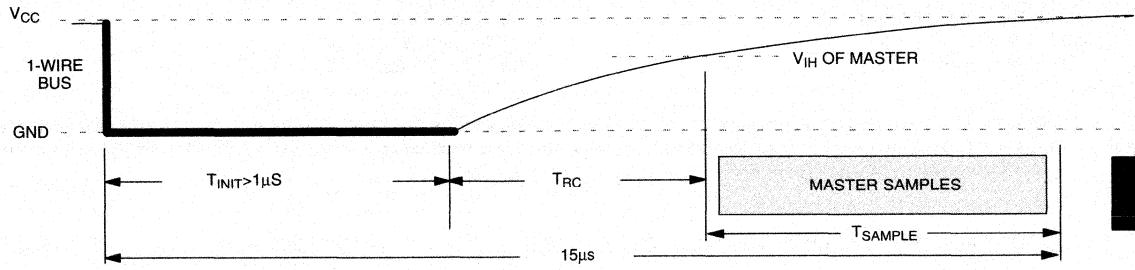
INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 5



READ/WRITE TIMING DIAGRAM Figure 6



DETAILED MASTER READ "1" TIMING Figure 7



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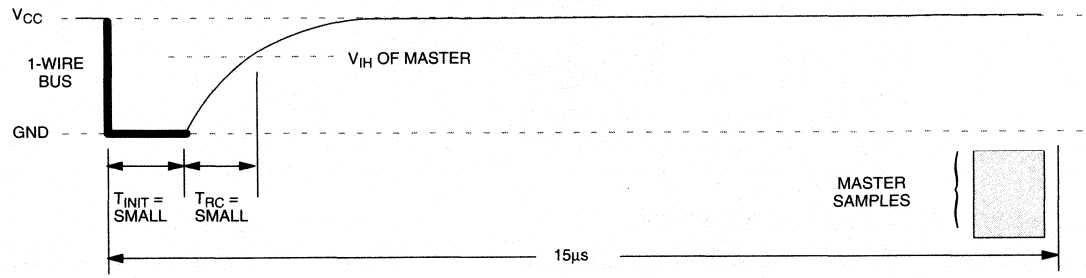
RECOMMENDED MASTER READ "1" TIMING Figure 8



LINE TYPE LEGEND:

	Bus master active low		DS2434 active low
	Both bus master and DS2434 active low		Resistor pull-up

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	–40°C to +85°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(–40°C to +85°C; V_{DD}=3.6V to 6.4V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD}	I/O Functions	2.5		6.4	V	
		NV Copy Functions	2.7		6.4		
		±1/2°C Accurate Temp. Conversions	3.6		6.4		1
Data Pin	$V_{I/O}$		–0.3		V_{CC}+0.3	V	

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{DD}=3.6V to 6.4V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Temperature Accuracy (=T_{ACTUAL} – $T_{MEASURED}$)		T_A=0°C to 70°C			±1/2	°C	
		T_A=–40°C to 0°C and +70°C to +85°C			±1		
Input Logic High	V_{IH}		2.2		V_{CC}+0.3	V	
Input Logic Low	V_{IL}		–0.3		+0.8	V	
Sink Current	I_L	$V_{I/O}$=0.4V	–4.0			mA	
Standby Current	I_Q				1	µA	
Active Current	I_{DD}				1.5	mA	2
Input Resistance	R_I			500		KΩ	2

NOTES:

1. Temperature conversion will work with ±2°C accuracy down to V_{DD}=2.7V.
2. I/O line in "hi–Z" state and $I_{I/O}$=0.

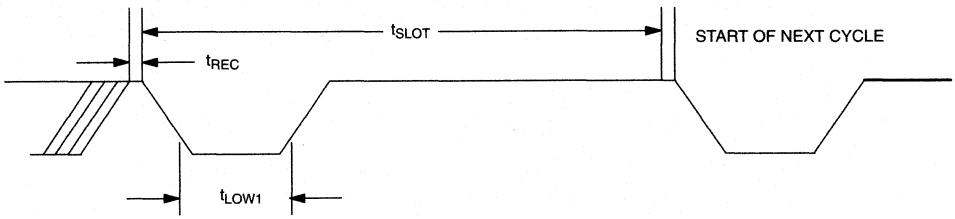
AC ELECTRICAL CHARACTERISTICS: 1–WIRE INTERFACE

(–40°C to +85°C; V_{DD}=3.6V to 6.4V)

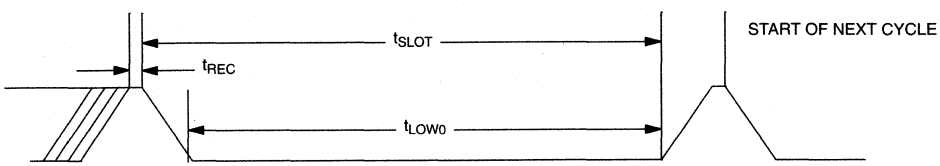
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Temperature Conversion Time	t_{CONV}		700	1000	ms	
Time Slot	t_{SLOT}	60		120	µs	
Recovery Time	t_{REC}	1			µs	
Write 0 Low Time	t_{LOW0}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Read Data Valid	t_{RDV}			15	µs	
Reset Time High	t_{RSTH}	480			µs	
Reset Time Low	t_{RSTL}	480		960	µs	
Presence Detect High	t_{PDHIGH}	15		60	µs	
Presence Detect Low	t_{PDLOW}	60		240	µs	
Capacitance	$C_{IN/OUT}$			25	pF	
NV Write Cycle	t_{WR}		10	50	ms	

2

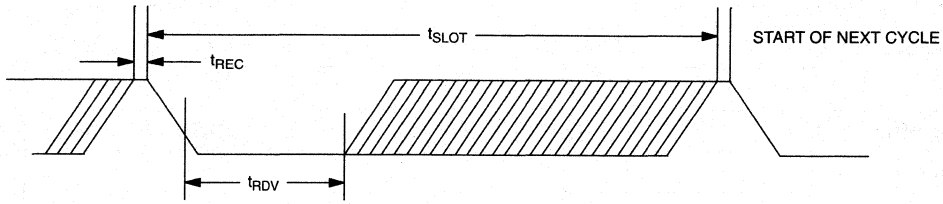
1–WIRE WRITE ONE TIME SLOT



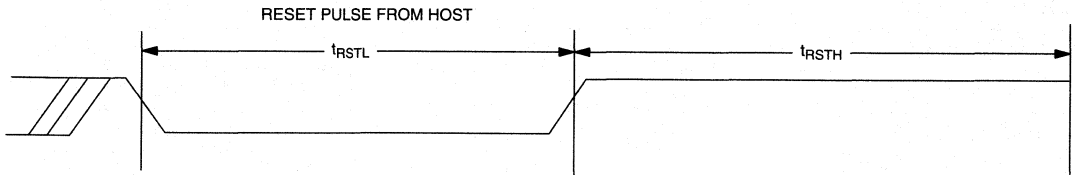
1–WIRE WRITE ZERO TIME SLOT



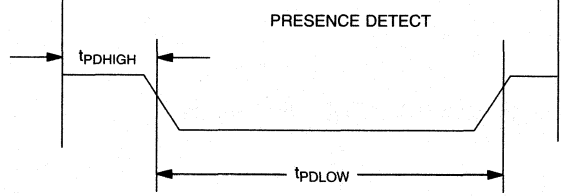
1-WIRE READ ZERO TIME SLOT



1-WIRE RESET PULSE



1-WIRE PRESENCE DETECT



DALLAS SEMICONDUCTOR

DS2435
Battery Identification Chip with Time/Temperature Histogram

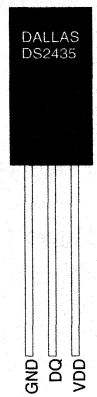
2

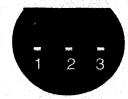
FEATURES

- Provides unique ID number to battery packs
- Eliminates thermistors by sensing battery temperature on–chip
- Elapsed time counter provides indication of battery usage/storage time
- Time/Temperature histogram function provides essential information for determining battery self–discharge
- 256–bit nonvolatile user memory available for storage of user data such as gas gauge and manufacturing information.
- Operating range of –40°C to +85°C
- Applications include portable computers, portable/cellular phones, consumer electronics, and hand held instrumentation.

PACKAGE OUTLINE

PR–35 PACKAGE





BOTTOM VIEW

See Mech. Drawings Section

PIN DESCRIPTION

GND	–	Ground
DQ	–	Data In/Out
V_{DD}	–	Supply Voltage

DESCRIPTION

The DS2435 Battery Identification Chip provides a convenient method of tagging and identifying battery packs by manufacturer, chemistry, or other identifying parameters. The DS2435 allows the battery pack to be coded with a unique identification number, and also store information regarding the battery life and charge/discharge characteristics in its nonvolatile memory.

The DS2435 also performs the essential function of monitoring battery temperature, without the need for a thermistor in the battery pack. A time/temperature histogram function stores the amount of time that the battery has been in up to eight temperature bands, allowing more accurate self–discharge calculations to be carried out by the user for determining remaining battery capacity. In addition, the on–board elapsed time counter provides a method of determining the amount of time that a battery pack has been in storage, to allow more accurate self–discharge determination.

Information is sent to/from the DS2435 over a 1–wire interface, so that battery packs need only have three output connectors; power, ground, and the 1–wire interface.

DETAILED PIN DESCRIPTION

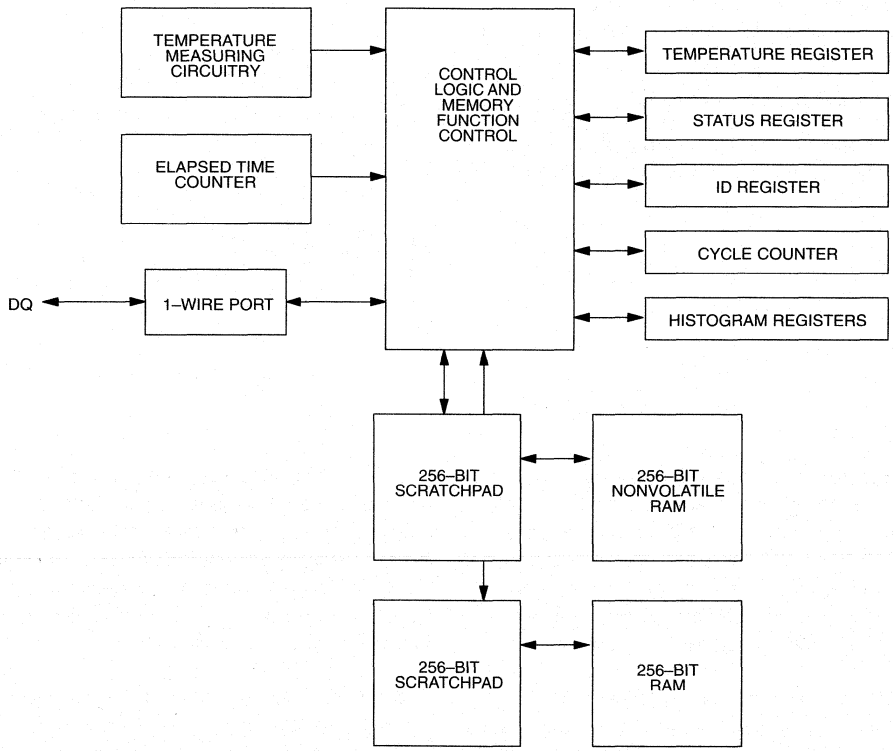
PIN	SYMBOL	DESCRIPTION
1	GND	**Ground pin.**
2	DQ	**Data Input/Output pin** for 1–wire communication port.
3	V_{DD}	**Supply pin** – input power supply.

OVERVIEW

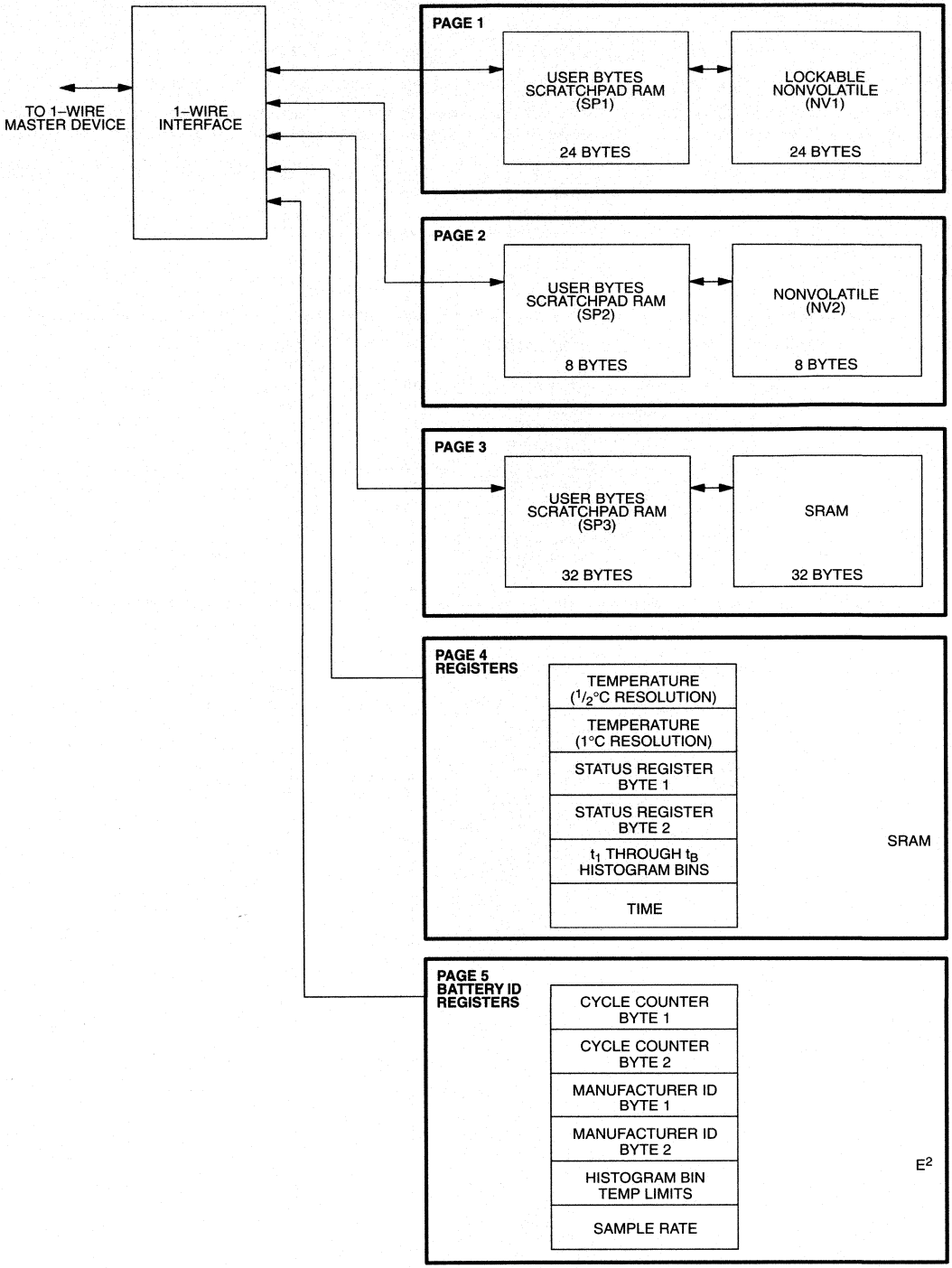
The DS2435 has six major components: 1) Scratchpad Memory, 2) Nonvolatile Memory, 3) On–board SRAM, 4) Temperature Sensor, 5) ID Register, and 6) elapsed time counter. All data is read and written least significant bit first.

Access to the DS2435 is over a 1–wire interface. Charging parameters and other data such as battery chemistry, gas gauge information, and other user data would be stored in the DS2435, allowing this information to be permanently stored in the battery pack. Nonvolatile (E^2) RAM holds information even if the battery goes dead; as long as the battery remains within typical charge/discharge operating range, the SRAM provides battery–backed storage of information.

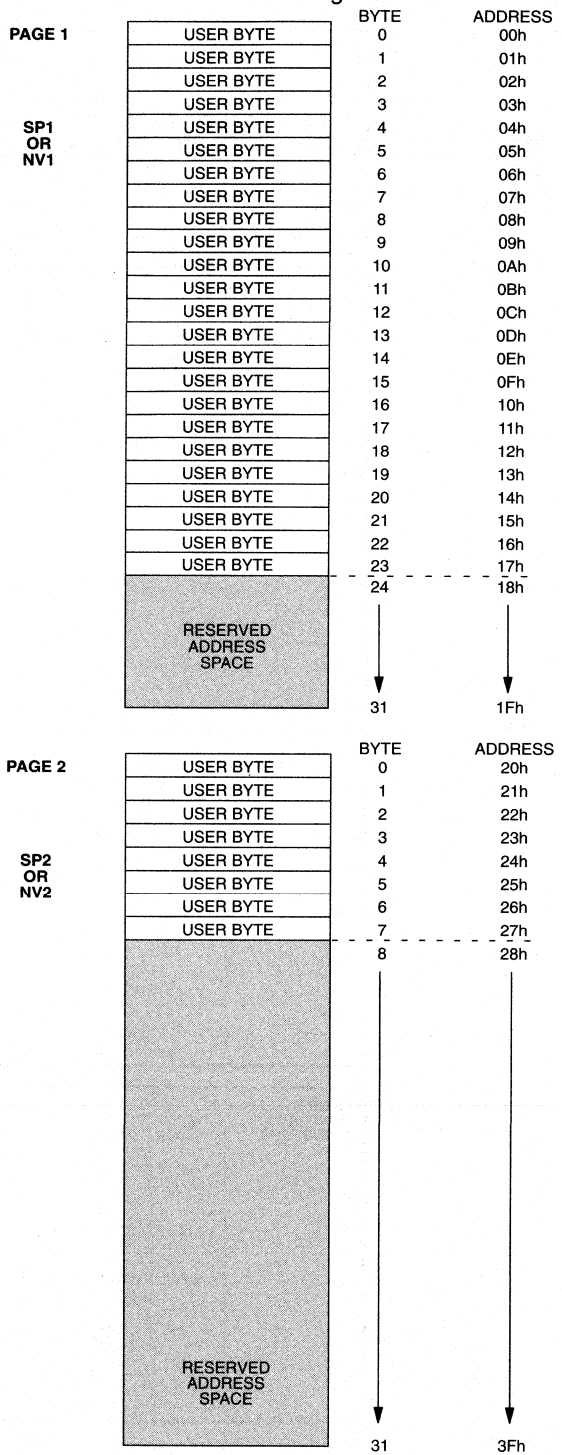
DS2435 BLOCK DIAGRAM Figure 1



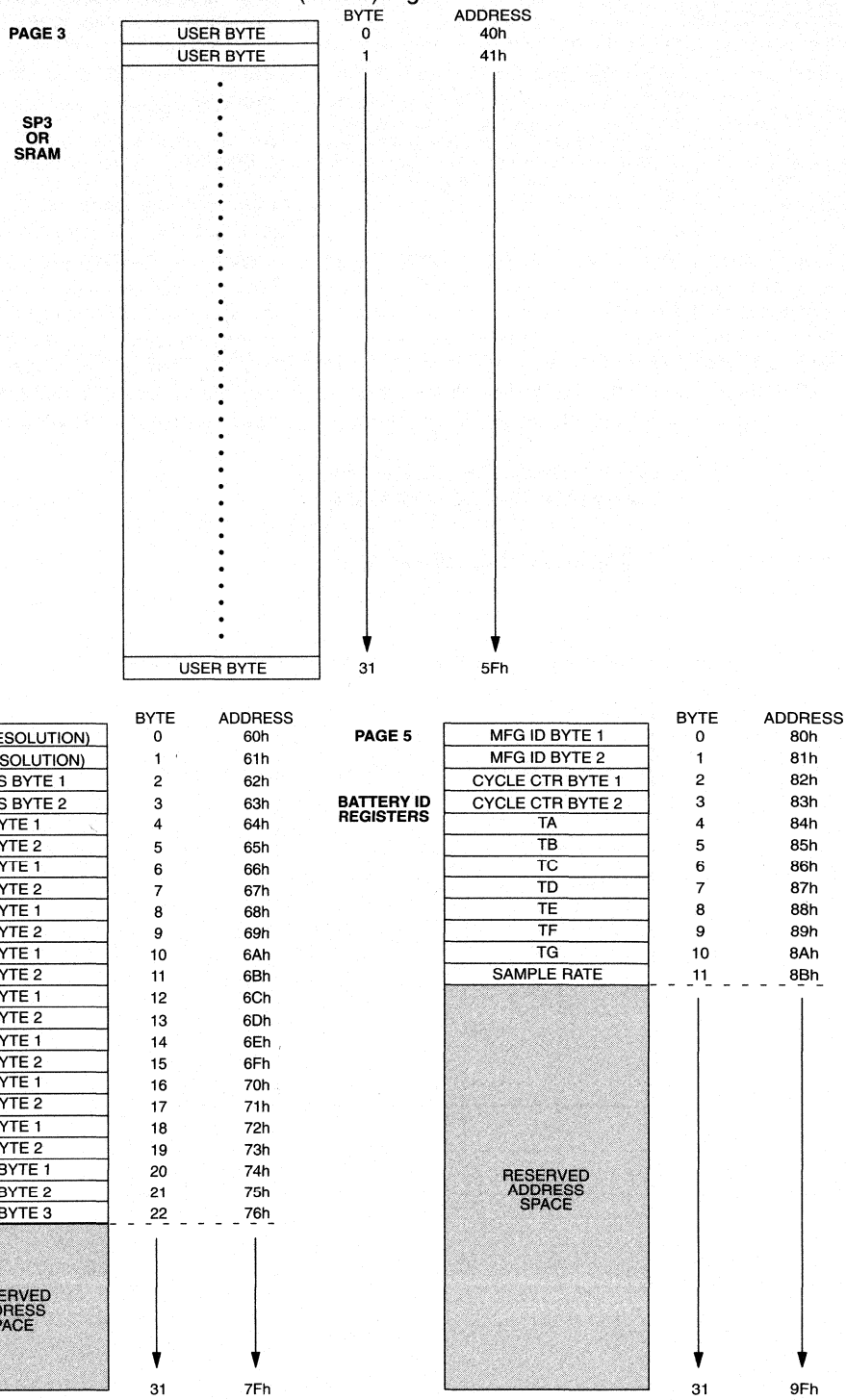
DS2435 MEMORY PARTITIONING Figure 2



DS2435 ADDRESSABLE RAM MEMORY MAP Figure 3



DS2435 ADDRESSABLE RAM MEMORY MAP (Cont'd) Figure 3



OVERVIEW – TIME/TEMPERATURE HISTOGRAM

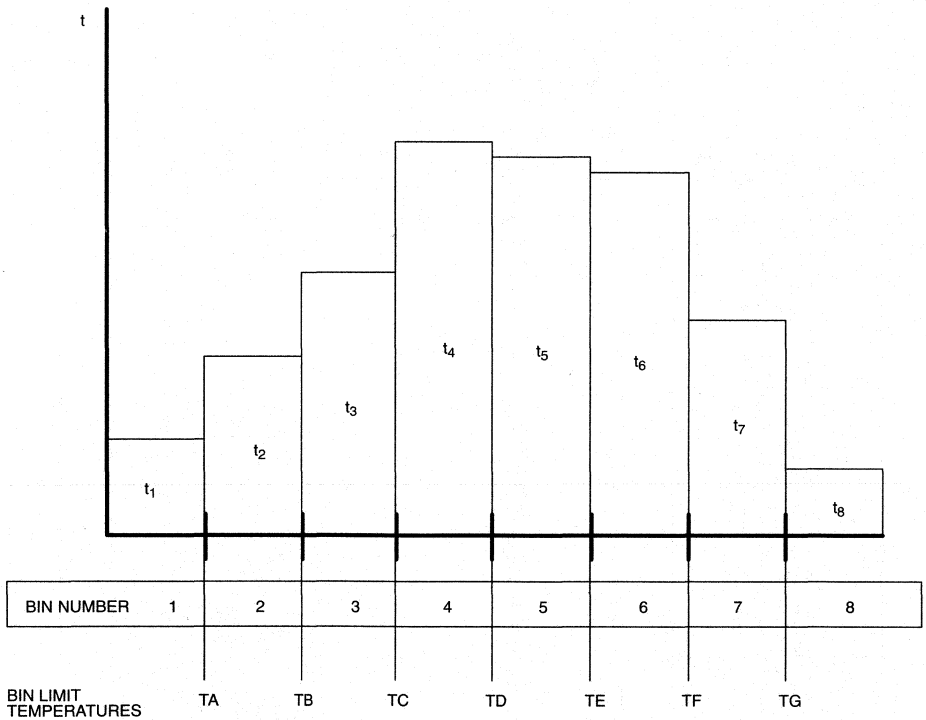
Periods of storage are normal for most battery applications. During this storage time, little or no current is actually drawn from the battery; however, batteries will lose capacity during this storage time due to parasitic side reactions in the cell, as well as other electrochemical mechanisms. This loss of capacity is termed self–discharge.

Since self–discharge is the result of electrochemical reactions, its rate is dependent upon the cell temperature. Knowing the time spent in certain temperature ranges during the storage time of the battery, these temperature effects may be factored into a calculation of self–discharge for the battery, thereby allowing a more accurate determination of retained battery capacity.

The DS2435 measures, tabulates and stores this information in the battery pack. The DS2435 periodically measures the battery temperature, and updates the appropriate temperature "bin" of the time/temperature histogram with the time spent in that temperature range. The resulting histogram data would appear graphically as shown in Figure 4.

The DS2435 allows for eight temperature ranges, or bins, to be specified by fixing the values of the bin limits, TA through TG. Once specified, the time spent in each of the bins (bin 1 being anything less than TA, bin 2 being temperature greater than or equal to TA but less than TB, etc., and bin 8 being anything greater than or equal to TG) is recorded (t_1 being the time spent in bin 1, t_2 the time spent in bin 2, etc.). Using this information and data from the battery manufacturer regarding retained capacity, the actual battery capacity remaining may be closely approximated by the user.

TIME/TEMPERATURE HISTOGRAM Figure 4



MEMORY

The DS2435's memory is divided into five pages, each page filling 32 bytes of address space. Not all of the available addresses are used, however. Refer to the memory map of Figure 3 to see actual addresses which are available for use.

The first three pages of memory consist of a scratchpad RAM and then either a nonvolatile RAM (pages 1 and 2) or SRAM (page 3). The scratchpads help insure data integrity when communicating over the 1–wire bus. Data is first written to the scratchpad where it can be read back. After the data has been verified, a copy scratchpad command will transfer the data to the RAM (NV or SRAM). This process insures data integrity when modifying the memory.

The fourth page of memory consists of registers which contain the measured temperature value, time/temperature histogram registers, elapsed time counter, and status registers for the device; these registers are made from SRAM cells.

The fifth page of memory holds the ID number for the device, the cycle count registers and the histogram bin limits in E^2 RAM, making these registers nonvolatile under all power conditions.

PAGE 1

The first page of memory has 24 bytes. It consists of a scratchpad RAM and a nonvolatile (E^2) RAM. These 24 bytes may be used to store any data the user wishes; such as battery chemistry descriptors, manufacturing lot codes, gas gauge information, etc.

The nonvolatile portion of this page may be locked to prevent data stored here from being changed inadvertently.

Both the nonvolatile and the scratchpad portions are organized identically, as shown in the memory map of Figure 3. In this page, these two portions are referred to as NV1 and SP1, respectively.

PAGE 2

The second page of memory has 8 bytes. It consists of a scratchpad RAM and a nonvolatile (E^2) RAM. These eight bytes may be used to store any data the user wishes, such as battery chemistry descriptors, manufacturing lot codes, gas gauge information, etc.

PAGE 3

The third page of memory has a full 32 bytes. It consists of a scratchpad RAM and an SRAM. This address space may be used to store any data the user wishes, provided that, should the battery go dead and power to the DS2435 is lost, this data may also be lost without serious repercussions. Data which must remain even if power to the DS2435 is lost should be placed in either Page 1 or Page 2.

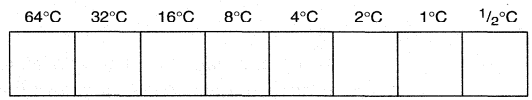
This section of memory may be used to store gas gauge and self discharge information. If the battery dies, and this information is lost, it is moot because the user can easily determine that the battery is dead.

PAGE 4

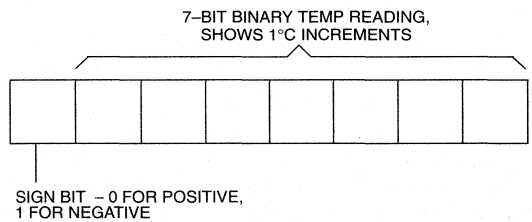
The fourth page of memory is used by the DS2435 to store the converted value of battery temperature, the time/temperature histogram data, and the elapsed time counter. A two–byte status register is also provided.

TEMPERATURE REGISTERS (60h–61h)

The DS2435 can measure temperature without external components. The resulting temperature measurement is placed into two temperature registers. These registers are SRAM, and therefore will hold the values placed in them until the battery voltage falls below the minimum V_{DD} specified. The first register, at address 60h, provides $^1/_2$°C resolution for temperatures between 0°C and 127 $^1/_2$°C, formatted as follows:



The second register, at address 61h, provides 1°C resolution over the –40°C to +85°C range, formatted as follows in the binary two's complement coding as shown in Table 1:



TEMPERATURE/DATA RELATIONSHIPS

Table 1

TEMPERATURE	DIGITAL OUTPUT (Binary)	DIGITAL OUTPUT (Hex)
+85°C	01010101	55h
+25°C	00011001	19h
1°C	00000001	01h
0°C	00000000	00h
–1°C	11111111	FFh
–25°C	11100111	E7h
–40°C	11011000	D8h

STATUS/CONTROL REGISTER (62h–63h)

The status register is a two byte register at addresses 62h and 63h (consisting of SRAM). Address 62h is the least significant byte of the status register, and is currently the only address with defined status bits; the other byte at address 63h is reserved for future use. The status register is formatted as follows:

STATUS REGISTER

							LSB	
X	X	X	X	X	LOCK	NVB	TB	62h
X	X	X	X	X	X	X	X	63h

where

X = Don't Care

TB = Temperature Busy flag. "1" = temperature conversion in progress; "0" = temperature conversion complete, valid data in temperature register.

NVB = Nonvolatile memory busy flag. "1" = Copy from scratchpad to NVRAM in progress, "0" = nonvolatile memory is not busy. A copy to NVRAM may take from 2 ms to 10 ms (taking longer at lower supply voltages).

LOCK = "1" indicates that NV1 is locked; "0" indicates that NV1 is unlocked.

t_1–t_8 REGISTERS (64h–73h)

These registers hold the accumulated time values for the time/temperature histogram. t_1 corresponds to the time spent in histogram bin 1, t_2 the time spent in bin 2, etc., where the bins are defined by the limits set in TA–TG as shown in Figure 4. The format for the time value stored in these two–byte registers depends upon the SAMPLE RATE, and is defined in the paragraph describing the SAMPLE RATE parameter.

t REGISTER (74n–76h)

This three–byte register is the elapsed time counter, formatted as follows:

ELAPSED TIME COUNTER

2^{23} min	2^{22} min	2^{21} min	2^{20} min	2^{19} min	2^{18} min	2^{17} min	2^{16} min	76h
32768 min	16384 min	8192 min	4096 min	2048 min	1024 min	512 min	256 min	75h
128 min	64 min	32 min	16 min	8 min	4 min	2 min	1 min	74h

The elapsed time counter has an LSB value of 1 minute; the total time which the counter can accommodate is 2^{24} minutes, or 31.92 years.

Issuing any protocol to the DS2435 prevents the incrementing of the elapsed time counter and histogram registers, until the protocol is cleared by issuing a reset. Therefore, it is imperative that any protocol issued to the DS2435 be followed by a reset (either after the protocol, if it requires no data, or immediately following data, if required by the protocol). This is necessary to avoid contention between the counter and histogram writing process and external processes.

PAGE 5

The fifth page of memory holds the battery manufacturer ID number, a two–byte counter for counting the number of battery charge/discharge cycles, histogram bin limits, and sample rate.

ID REGISTER (80h and 81h)

The ID Register is a 16–bit ROM register that can contain a unique identification code, if purchased from Dallas Semiconductor. This ID number is programmed by Dallas Semiconductor, is unchangeable, and is unique to each customer. This ID number may be used to assure that batteries containing a DS2435 have the same manufacturer ID number as a charger configured to operate with that battery pack. This feature may be used to prevent charging of batteries for which the charging circuit has not been designed.

CYCLE COUNTER (82h and 83h)

The cycle counter register gives an indication of the number of charge/discharge cycles the battery pack has been through. This nonvolatile (E^2) register is incremented by the user through the use of a protocol to the DS2435, and is reset by another protocol. The counter is a straight binary counter, formatted as follows:

CYCLE COUNTER

MSB

32768	16384	8192	4096	2048	1024	512	256

65h

LSB

128	64	32	16	8	4	2	0

64h

TA–TG REGISTERS (84h–8Ah)

These registers define the boundaries for the temperature bins in the time/temperature histogram, as shown in Figure 4. These temperature values are expressed in the same temperature format as shown in Table 1. These limits therefore may be positive or negative values, expressed with 1°C resolution. The bin limits must be specified in increasing order (i.e., TA<TB, TB<TC, etc.).

SAMPLE RATE (8Bh)

This register defines the periodic interval at which the DS2435 will take a temperature measurement for updating the histogram data. Note that this does not affect the actual time needed to perform a temperature conversion using the Convert T protocol; this sample rate refers only to the periodic interval at which histogram data is updated.

The sample rate is expressed as follows:

SAMPLE RATE

LSB

X	X	X	X	X	S2	S1	S0

S2	S1	S0	SAMPLE RATE
0	0	0	1/2 minute
0	0	1	1 minute
0	1	0	2 minutes
0	1	1	4 minutes
1	0	0	1/8 hour
1	0	1	1/4 hour
1	1	0	1/2 hour
1	1	1	1 hour

The interval specified in this register determines the LSB value for the time/temperature histogram registers, as shown in Figure 5. Examples of time expressions for a given sample rate are shown in Table 2.

HISTOGRAM REGISTER DATA GIVEN FOR SAMPLE RATE Figure 5

SAMPLE RATE — DATA STRUCTURE – NUMBERS EXPRESS MINUTES

LSB

16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1	.	1/2

SAMPLE RATE — DATA STRUCTURE – NUMBERS EXPRESS HOURS

LSB

1/8	4096	2048	1024	512	256	128	64	32	16	8	4	2	1	.	1/2	1/4	1/8
1/4	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1	.	1/2	1/4
1/2	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1	.	1/2
1	32768	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1	.

BYTE 2 — BYTE 1

EXAMPLE CODES FOR 771 HOURS, 22.5 MINUTES WITH DIFFERENT SAMPLE RATES Table 2

SAMPLE RATE	t_X BYTE 1	t_X BYTE 2
1/8	00011000	00011011
1/4	00001100	00001101
1/2	00000110	00000110
1	00000011	00000011

MEMORY FUNCTION COMMANDS

The protocols necessary for accessing the DS2435 are described in this section. These are summarized in Table 3, and examples of memory functions are provided in Tables 4 and 5.

PAGE 1 THROUGH PAGE 3 COMMANDS

Read Scratchpad [11h]

This command reads the contents of the scratchpad RAM on the DS2435. This command is followed by a start byte address. After issuing this command and providing the start address, the user may begin reading the data. The user may read data through the end of the scratchpad space (address 5Fh), with any reserved data bits reading all logic 1's and after which the data read will be a repeat of address 5FH.

Write Scratchpad [17h]

This command writes to the scratchpad RAM on the DS2435. This command is followed by a start byte address. After issuing this command and providing the start address, the user may begin writing data to the DS2435 scratchpad at the starting byte address.

Copy SP1 to NV1 [22h]

This command copies the entire contents (24 bytes) of Scratchpad 1 (SP1) to its corresponding nonvolatile memory (NV1). The nonvolatile RAM memory of the DS2435 cannot be written to directly by the bus master; however, the scratchpad RAM may be copied to the nonvolatile RAM. This prevents accidental overwriting of the nonvolatile RAM, and allows the data to be written first to the scratchpad, where it can be read back and verified before copying to the nonvolatile RAM. This command does not use a start address; the entire contents of the scratchpad will be copied to the nonvolatile RAM. The NVB bit will be set when the copy is in progress. NV1 is made with E^2 type memory cells that will accept at least 50000 changes.

Copy SP2 to NV2 [25h]

This command copies the entire contents (8 bytes) of SP2 (user bytes) to its corresponding nonvolatile memory (NV2). This command does not use a start address; the entire contents of SP2 will be copied to NV2. The NVB bit will be set when the copy is in progress. NV2 is made with E^2 type memory cells that will accept at least 50000 changes.

Copy SP3 to SRAM [28h]

This command copies the entire contents (32 bytes) of SP3 to its corresponding SRAM. This command does not use a start address; the entire contents of SP3 will be copied to the SRAM.

Copy NV1 to SP1 [71h]

This command copies the entire contents (24 bytes) of NV1 to its corresponding scratchpad RAM (SP1). This command does not use a start address; the entire contents of NV1 will be copied to SP1. The nonvolatile RAM memory of the DS2435 cannot be read directly by the bus master; however, the nonvolatile RAM may be copied to the scratchpad RAM.

Copy NV2 to SP2 [77h]

This command copies the entire contents (8 bytes) of NV2 (user bytes) to its corresponding scratchpad RAM (SP2). This command does not use a start address; the entire contents of NV2 will be copied to SP2. The nonvolatile RAM memory of the DS2435 cannot be read directly by the bus master; however, the nonvolatile RAM may be copied to the scratchpad RAM.

Copy SRAM to SP3 [7Ah]
This command copies the entire contents (32 bytes) of SRAM to its corresponding scratchpad RAM (SP3). This command does not use a start address; the entire contents of SRAM will be copied to SP3.The SRAM memory of the DS2435 cannot be read directly by the bus master; however, the SRAM may be copied to the scratchpad RAM.

Lock NV1 [43h]
This command prevents copying SP1 to NV1. This is done as an added measure of data security, preventing data from being changed inadvertently. NV1 may be copied up into SP1 while the part is locked. This allows NV1 to be read at any time. However, NV1 cannot be written to through a Copy SP1 to NV1 command without first unlocking the DS2435.

Unlock NV1 [44h]
This command unlocks NV1, to allow copying SP1 into NV1. This is done as an added measure of data security, preventing data from being changed inadvertently.

PAGE 4 AND 5 COMMANDS

Convert T [D2h]
This command instructs the DS2435 to initiate a temperature conversion cycle. This sets the TB flag. When the temperature conversion is done, the TB flag is reset and the current temperature value is placed in the temperature register. While a temperature conversion is taking place, all other memory functions are still available for use.

Reset Histogram [E1h]
This command resets the accumulated time in all of the histogram temperature registers to zero. In addition, this command also resets the elapsed time counter to zero. This command does not use a start address; no further data is required.

Set Clock [E6h]
This command sets the elapsed time counter to a preset value. This command is followed by three bytes of data, which will be stored at addresses 74h–76h. The transfer of this 3–byte value will occur after reception of the 24th bit following the protocol, at which time the elapsed time counter will begin incrementing the counter registers in 1 minute increments.

Write Registers [EFh]
This command allows writing directly to the TA–TG registers and the sample rate register. This command is followed by a start byte address. After issuing this command and providing the start address, the user may begin writing the data.

Read Registers [B2h]
This command reads the contents of the registers in Page 4 and 5. This command is followed by a start byte address. After issuing this command and providing the start address, the user may begin reading the data. The user may read data through the end of the register space (through address 76h in Page 4, address 8Bh in Page 5), after which the data read will be all logic 1's.

Increment Cycle [B5h]
This command increments the value in the cycle counter register. This command does not use a start address; no further data is required.

Reset Cycle Counter [B8h]
This command is used to reset the cycle counter register to zero, if desired.

DS2435 COMMAND SET Table 3

INSTRUCTION	DESCRIPTION	PROTOCOL	1–WIRE BUS MASTER STATUS AFTER ISSUING PROTOCOL	1–WIRE BUS DATA AFTER ISSUING PROTOCOL
PAGE 1 THROUGH PAGE 3 MEMORY COMMANDS				
Read Scratchpad	Reads bytes from DS2435 Scratchpad.	11h <addr (00h–5Fh)>	RX	<read data>
Write Scratchpad	Writes bytes to DS2435 Scratchpad.	17h <addr 00h–5Fh)>	TX	<write data>
Copy SP1 to NV1	Copies entire contents of SP1 to NV1.	22h	Idle	{NVB bit in Status Register=1 until copy complete (2–5ms, typ)}
Copy SP2 to NV2	Copies entire contents of SP2 to NV2.	25h	Idle	{NVB bit in Status Register=1 until copy complete (2–5ms, typ)}
Copy SP3 to SRAM	Copies entire contents of SP3 to SRAM.	28h	Idle	Idle
Copy NV1 to SP1	Copies entire contents of NV1 to SP1.	71h	Idle	Idle
Copy NV2 to SP2	Copies entire contents of NV2 to SP2.	77h	Idle	Idle
Copy SRAM to SP3	Copies entire contents of SRAM to SP3.	7Ah	Idle	Idle
Lock NV1	Locks 24 bytes of SP1 and NV1 from reading and writing.	43h	Idle	{NVB bit in Status Register=1 until copy complete (2–5ms, typ)}
Unlock NV1	Unlocks 24 bytes of SP1 and NV1 for reading and writing.	44h	Idle	{NVB bit in Status Register=1 until copy complete (2–5ms, typ)}
PAGE 4 AND PAGE 5 REGISTER COMMANDS				
Read Registers	Reads bytes from Temperature, Status and ID Registers.	B2h <addr (60h–76h, 80h–8Bh)>	RX	<read data>
Write Register	Write to TA–TG and Sample Rate Registers	EFh <addr 84h–8Bh>		
Reset Cycle Counter	Resets cycle counter registers to zero.	B8h	Idle	{NVB bit in Status Register=1 until copy complete (2–5ms, typ)}
Increment Cycle Counter	Increments the value in the cycle counter register.	B5h	Idle	{NVB bit in Status Register=1 until copy complete (2–5ms, typ)}
Reset Historgram	Resets all histogram registers to zero	E1h	Idle	Idle
Set Clock	Presets a value for elapsed time counter and begins timing.	E6h	TX·	<3 bytes>
Convert T	Initiates temperature conversion.	D2h	Idle	{TB bit in Status Register=1 until conversion complete}

MEMORY FUNCTION EXAMPLE Table 4
Example: Bus Master writes 24 bytes of data to DS2435 scratchpad, then copies to it to NV1.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480–960 µs)
RX	Presence	Presence pulse
TX	17h	Issue "write scratchpad" command
TX	00h	Start address
TX	<24 bytes>	Write 24 bytes of data to scratchpad
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	11h	Issue "read scratchpad" command
TX	00h	Start address
RX	<24 data bytes>	Read scratchpad data and verify
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	22h	Issue "copy SP1 to NV1" command
RX	<busy indicator>	Wait until NVB in status register=1 (2–5 ms typical)
TX	Reset	Reset pulse
RX	Presence	Presence pulse, done

MEMORY FUNCTION EXAMPLE Table 5
Example: Bus Master initiates temperature conversion, then reads temperature.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480–960 µs)
RX	Presence	Presence pulse
TX	D2h	Issue "convert T" command
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	B2h	Issue "read registers" command; begin loop
TX	62h	Status register address
RX	<1 data byte>	Read status register and loop until TB=0
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	B2h	Issue "read registers" command
TX	61h	Temperature register address
RX	<1 data byte>	Read temperature register
TX	Reset	Reset pulse
RX	Presence	Presence pulse, done

1–WIRE BUS SYSTEM

The DS2435 1–wire bus is a system which has a single bus master and one slave. The DS2435 behaves as a slave. The DS2435 is not able to be multidropped, unlike other 1–wire devices from Dallas Semiconductor.

The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1–wire signaling (signal types and timing).

HARDWARE CONFIGURATION

The 1–wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1–wire bus must have open drain or 3–state outputs. The 1–wire port of the DS2435 is open drain with an internal circuit equivalent to that shown in Figure 6. The 1–wire bus requires a pull–up resistor of approximately 5KΩ.

The idle state for the 1–wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 480 µs, all components on the bus will be reset.

TRANSACTION SEQUENCE

The protocol for accessing the DS2435 via the 1–wire port is as follows:

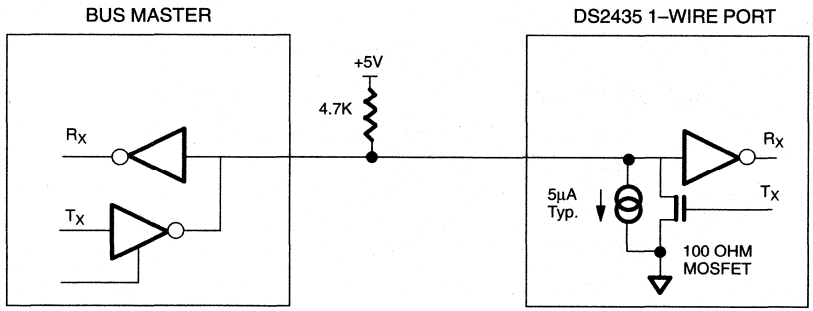
- Initialization
- Memory Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1–wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s).

The presence pulse lets the bus master know that the DS2435 is on the bus and is ready to operate. For more details, see the "I/O Signaling" section.

HARDWARE CONFIGURATION Figure 6



I/O SIGNALING

The DS2435 requires strict protocols to insure data integrity. The protocol consists of several types of signaling on one line: reset pulse, presence pulse, write 0, write 1, read 0, and read 1. All of these signals, with the exception of the presence pulse, are initiated by the bus master.

The initialization sequence required to begin any communication with the DS2435 is shown in Figure 7. A reset pulse followed by a presence pulse indicates the DS2435 is ready to send or receive data given the correct memory function command.

The bus master transmits (TX) a reset pulse (a low signal for a minimum of 480 µs). The bus master then releases the line and goes into a receive mode (RX). The 1–wire bus is pulled to a high state via the 5K pull–up resistor. After detecting the rising edge on the I/O pin, the DS2435 waits 15–60 µs and then transmits the presence pulse (a low signal for 60–240 µs).

READ/WRITE TIME SLOTS

DS2435 data is read and written through the use of time slots to manipulate bits and a command word to specify the transaction.

Write Time Slots

A write time slot is initiated when the host pulls the data line from a high logic level to a low logic level. There are two types of write time slots: Write One time slots and Write Zero time slots. All write time slots must be a minimum of 60 µs in duration with a minimum of a 1 µs recovery time between individual write cycles.

The DS2435 samples the I/O line in a window of 15 µs to 60 µs after the I/O line falls. If the line is high, a Write One occurs. If the line is low, a Write Zero occurs (see Figure 6).

For the host to generate a Write One time slot, the data line must be pulled to a logic low level and then released, allowing the data line to pull up to a high level within 15 µs after the start of the write time slot.

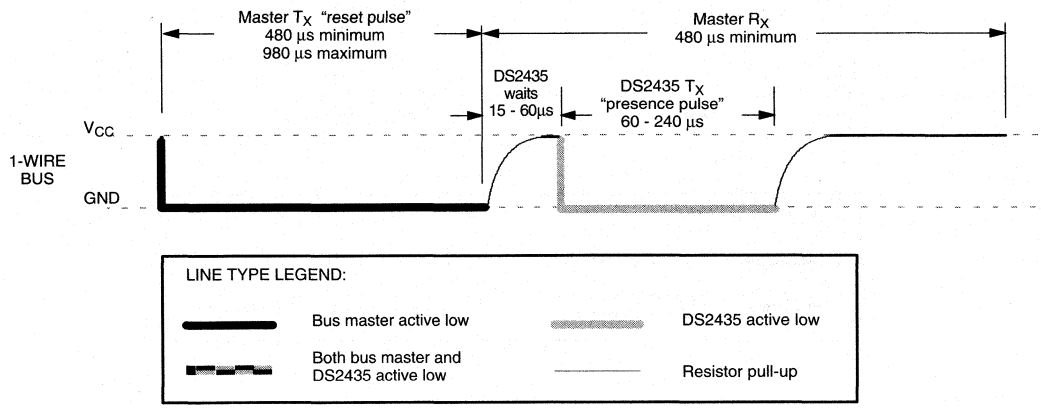
For the host to generate a Write Zero time slot, the data line must be pulled to a logic low level and remain low for the duration of the write time slot.

Read Time Slots

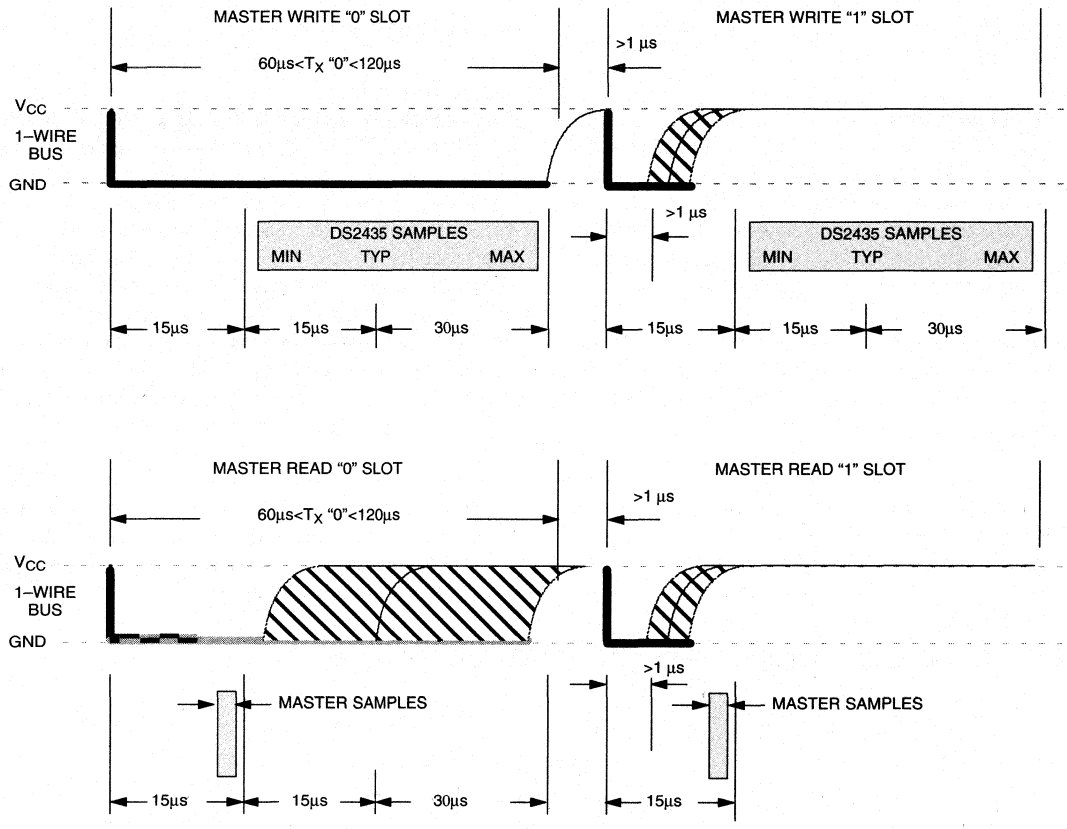
The host generates read time slots when data is to be read from the DS2435. A read time slot is initiated when the host pulls the data line from a logic high level to logic low level. The data line must remain at a low logic level for a minimum of 1 µs; output data from the DS2435 is then valid for the next 14 µs maximum. The host therefore must stop driving the I/O pin low in order to read its state 15 µs from the start of the read slot (see Figure 8). By the end of the read time slot, the I/O pin will pull back high via the external pull–up resistor. All read time slots must be a minimum of 60 µs in duration with a minimum of a 1 µs recovery time between individual read slots.

Figure 9 shows that the sum of T_{INIT}, T_{RC}, and T_{SAMPLE} must be less than 15 µs. Figure 10 shows that system timing margin is maximized by keeping T_{INIT} and T_{RC} as small as possible and by locating the master sample time towards the end of the 15 µs period.

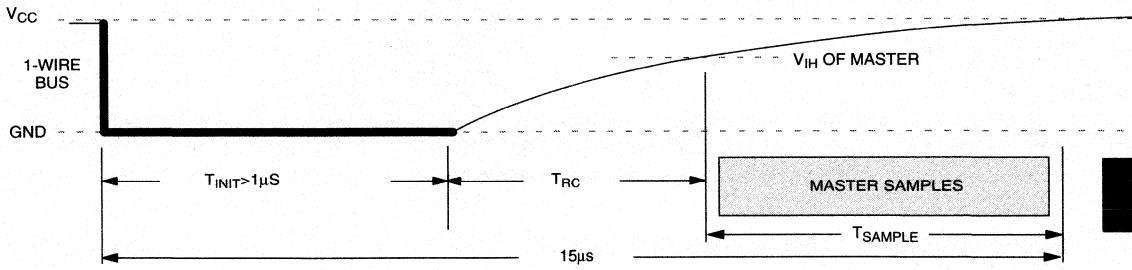
INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 7



READ/WRITE TIMING DIAGRAM Figure 8

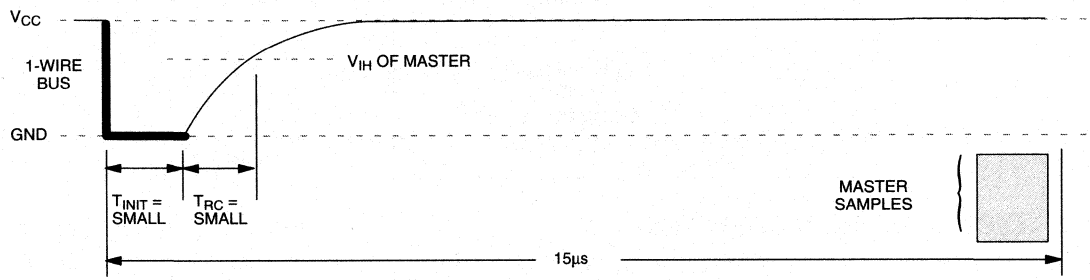


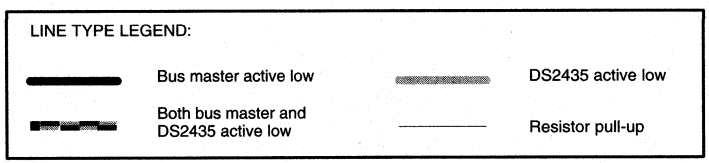
DETAILED MASTER READ "1" TIMING Figure 9



2

RECOMMENDED MASTER READ "1" TIMING Figure 10





ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	–40°C to +85°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(–40°C to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD}	I/O Functions	2.5		6.4	V	
		NV Copy Functions	2.7		6.4		
		$\pm 1/2$°C Accurate Temp. Conversions	3.6		6.4		1
Data Pin	$V_{I/O}$		–0.3		V_{DD}+0.3	V	

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{DD}=3.6V to 6.4V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Temperature Accuracy (=$T_{ACTUAL} - T_{MEASURED}$)		T_A=0°C to 70°C			$\pm 1/2$	°C	
		T_A=–40°C to 0°C and +70°C to +85°C			See typical curve		3
Input Logic High	V_{IH}	V_{DD}=4.8V	2.2		V_{DD}+0.3	V	
Input Logic Low	V_{IL}	V_{DD}=4.8V	–0.3		+0.8	V	
Sink Current	I_L	$V_{I/O}$=0.4V	–4.0			mA	
Standby Current	I_Q	Clock Running		10	25	µA	4
Active Current	I_{DD}	Temp Conversions			1.5	mA	4
Input Resistance	R_I			500		KΩ	2

NOTES:

1. Temperature conversion will work with ±2°C accuracy down to V_{DD}=2.7V.
2. I/O line in "hi–Z" state and $I_{I/O}$=0. Resistance specified from I/O to ground.
3. See typical curve for specification limits outside 0°C to 70°C range.
4. Specified with DQ=V_{DD}.

AC ELECTRICAL CHARACTERISTICS: 1–WIRE INTERFACE

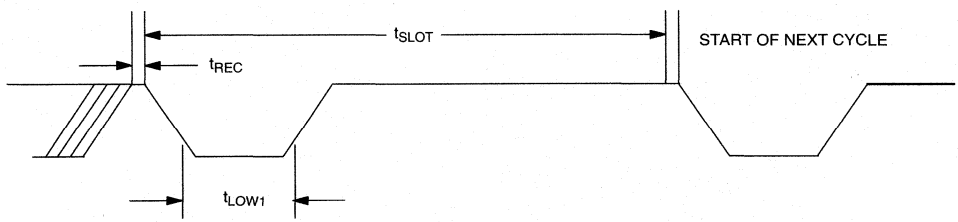
(–40°C to +85°C; V_{DD}=3.6V to 6.4V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Temperature Conversion Time	t_{CONV}		250	500	ms	
Time Slot	t_{SLOT}	60		120	µs	
Recovery Time	t_{REC}	1		20000	µs	5
Write 0 Low Time	t_{LOW0}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Read Data Valid	t_{RDV}			15	µs	
Reset Time High	t_{RSTH}	480			µs	
Reset Time Low	t_{RSTL}	480			µs	
Presence Detect High	t_{PDHIGH}	15		60	µs	
Presence Detect Low	t_{PDLOW}	60		240	µs	
Capacitance	$C_{IN/OUT}$			25	pF	
Timer Accuracy				±10	%	

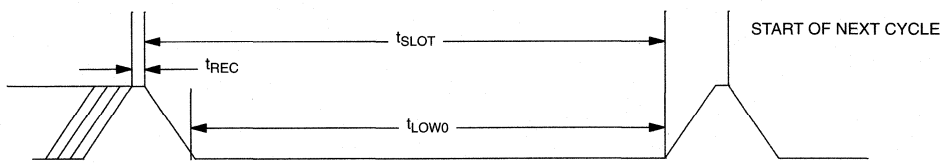
NOTE:

5. The bus should not remain idle for more than 20 ms between bits or between a bit and a reset.

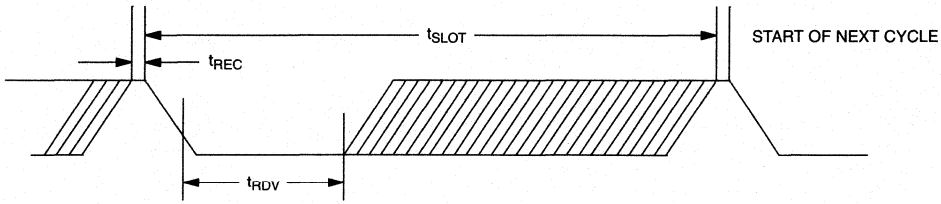
1–WIRE WRITE ONE TIME SLOT



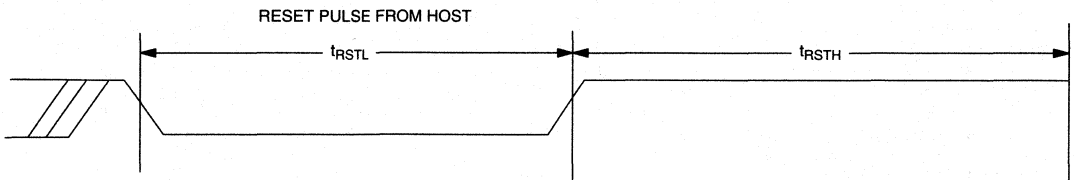
1–WIRE WRITE ZERO TIME SLOT



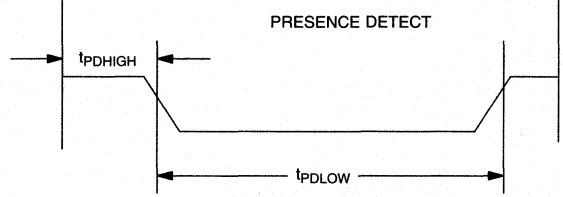
1-WIRE READ ZERO TIME SLOT



1-WIRE RESET PULSE

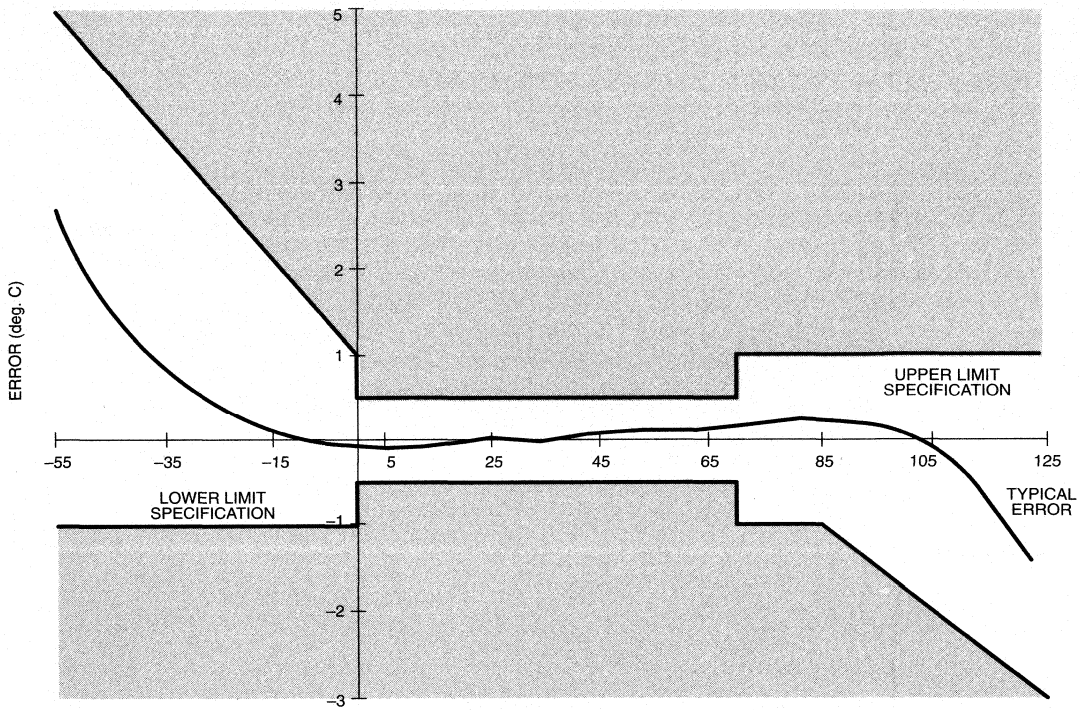


1-WIRE PRESENCE DETECT



TYPICAL PERFORMANCE CURVE

DS2435 DIGITAL THERMOMETER AND THERMOSTAT
TEMPERATURE READING ERROR



CPU SUPERVISORS

3

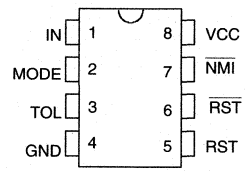
DALLAS SEMICONDUCTOR

DS1231/S
Power Monitor Chip

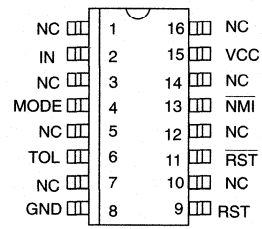
FEATURES

- Warns processor of an impending power failure
- Provides time for an orderly shutdown
- Prevents processor from destroying nonvolatile memory during power transients
- Automatically restarts processor after power is restored
- Suitable for linear or switching power supplies
- Adjusts to hold time of the power supply
- Supplies necessary signals for processor interface
- Accurate 5% or 10% V_{CC} monitoring
- Replaces power-up reset circuitry
- No external capacitors required
- Optional 16-pin SOIC surface mount package

PIN ASSIGNMENT



DS1231 8–Pin DIP
(300 MIL)
See Mech. Drawings
Section



DS1231S 16–Pin SOIC
(300 MIL)
See Mech. Drawings
Section

PIN DESCRIPTION

IN	–	Input
MODE	–	Selects input pin characteristics
TOL	–	Selects 5% or 10% V_{CC} detect
GND	–	Ground
RST	–	Reset (Active High)
$\overline{RST}$	–	Reset (Active Low, open drain)
$\overline{NMI}$	–	Non–Maskable Interrupt
V_{CC}	–	+5V Supply
NC	–	No Connections

DESCRIPTION

The DS1231 Power Monitor Chip uses a precise temperature-compensated reference circuit which provides an orderly shutdown and an automatic restart of a processor-based system. A signal warning of an impending power failure is generated well before regulated DC voltages go out of specification by monitoring high voltage inputs to the power supply regulators. If line isolation is required a UL-approved opto-isolator can be directly interfaced to the DS1231. The time for processor shutdown is directly proportional to the available hold-up time of the power supply. Just before the hold-up time is exhausted, the Power Monitor unconditionally halts the processor to prevent spurious cycles by enabling Reset as V_{CC} falls below a selectable 5 or 10 percent threshold. When power returns, the processor is held inactive until well after power conditions have stabilized, safeguarding any nonvolatile memory in the system from inadvertent data changes.

OPERATION

The DS1231 Power Monitor detects out-of-tolerance power supply conditions and warns a processor-based system of impending power failure. The main elements of the DS1231 are illustrated in Figure 1. As shown, the DS1231 actually has two comparators, one for monitoring the input (Pin 1) and one for monitoring V_{CC} (Pin 8). The V_{CC} comparator outputs the signals RST (Pin 5) and $\overline{RST}$ (Pin 6) when V_{CC} falls below a preset trip level as defined by TOL (Pin 3).

When TOL is connected to ground, the RST and $\overline{RST}$ signals will become active as V_{CC} goes below 4.75 volts. When TOL is connected to V_{CC}, the RST and $\overline{RST}$ signals become active as V_{CC} goes below 4.5 volts. The RST and $\overline{RST}$ signals are excellent control signals for a microprocessor, as processing is stopped at the last possible moments of valid V_{CC}. On power-up, RST and $\overline{RST}$ are kept active for a minimum of 150 ms to allow the power supply to stabilize (see Figure 2).

The comparator monitoring the input pin produces the $\overline{NMI}$ signal (Pin 7) when the input threshold voltage (V_{TP}) falls to a level as determined by Mode (Pin 2). When the Mode pin is connected to V_{CC}, detection occurs at V_{TP}-. In this mode Pin 1 is an extremely high impedance input allowing for a simple resistor voltage divider network to interface with high voltage signals. When the Mode pin is connected to ground, detection occurs at V_{TP}+. In this mode Pin 1 sources 30 µA of current allowing for connection to switched inputs, such as a UL-approved opto-isolator. The flexibility of the input pin allows for detection of power loss at the earliest point in a power supply system, maximizing the amount of time allotted between $\overline{NMI}$ and $\overline{RST}$. On power-up, $\overline{NMI}$ is released as soon as the input threshold voltage (V_{TP}) is achieved and V_{CC} is within nominal limits. In both modes of operation the input pin has hysteresis for noise immunity (Figure 3).

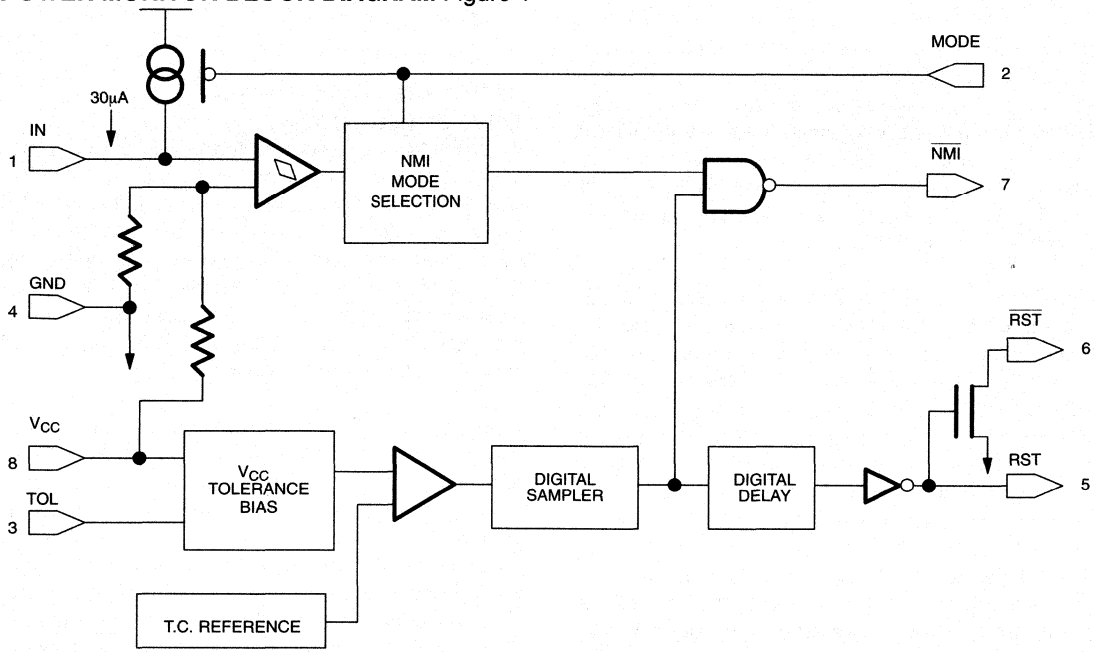
APPLICATION – MODE PIN CONNECTED TO V_{CC}

When the Mode pin is connected to V_{CC}, pin 1 is a high impedance input. The voltage sense point and the level of voltage at the sense point are dependent upon the application (Figure 4). The sense point may be developed from the AC power line by rectifying and filtering the AC. Alternatively, a DC voltage level may be selected which is closer to the AC power input than the regulated +5-volt supply, so that ample time is provided for warning before regulation is lost.

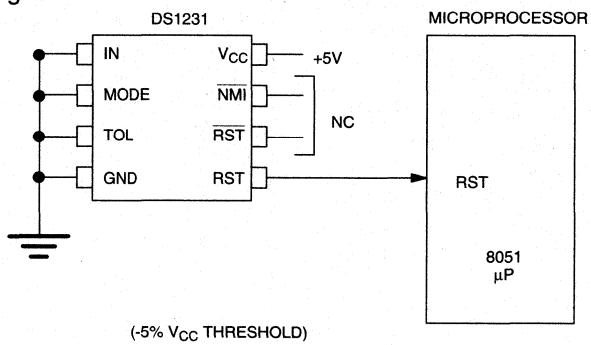
Proper operation of the DS1231 requires a maximum voltage of 5 volts at the input (Pin 1), which must be derived from the maximum voltage at the sense point. This is accomplished with a simple voltage divider network of R1 and R2. Since the IN trip point V_{TP}- is 2.3 volts (using the -20 device), and the maximum allowable voltage on pin 1 is 5 volts, the dynamic range of voltage at the sense point is set by the ratio of 2.3/5.0=.46 min. This ratio determines the maximum deviation between the maximum voltage at the sense point and the actual voltage which will generate $\overline{NMI}$.

Having established the desired ratio, and confirming that the ratio is greater than .46 and less than 1, the proper values for R1 and R2 can be determined by the equation as shown in Figure 4. A simple approach to solving this equation is to select a value for R2 which is high enough impedance to keep power consumption low, and solve for R1. Figure 5 illustrates how the DS1231 can be interfaced to the AC power line when the mode pin is connected to V_{CC}.

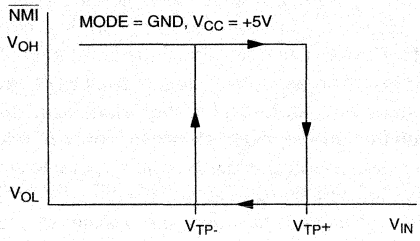
POWER MONITOR BLOCK DIAGRAM Figure 1



POWER-UP RESET Figure 2

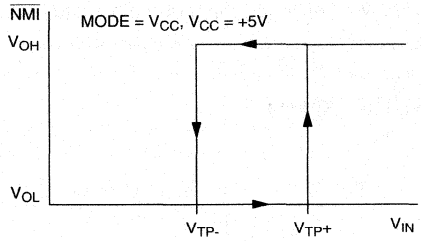


INPUT PIN HYSTERESIS Figure 3



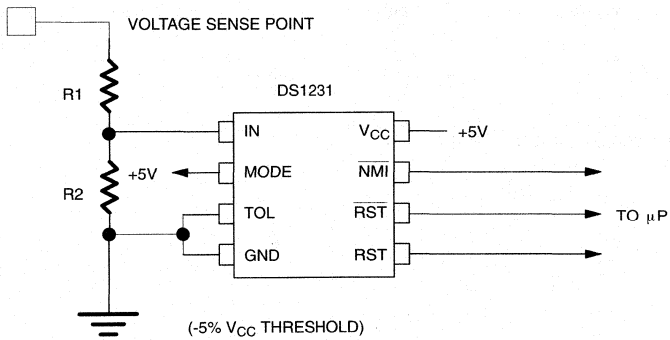
	–20	–35	–50
V_{TP-}	2.3	2.15	2.0
V_{TP+}	2.5	2.5	2.5

NOTE: HYSTERESIS TOLERANCE IS ±60 mV



3

APPLICATION WITH MODE PIN CONNECTED TO V_{CC} Figure 4



$$V\ SENSE = \frac{R1 + R2}{R2} \times 2.3 \qquad V\ MAX = \frac{V\ SENSE}{VTP -} \times 5.0$$

EXAMPLE: V SENSE = 8 VOLTS AT TRIP POINT AND A MAXIMUM VOLTAGE OF 17.5V WITH R2 = 10K

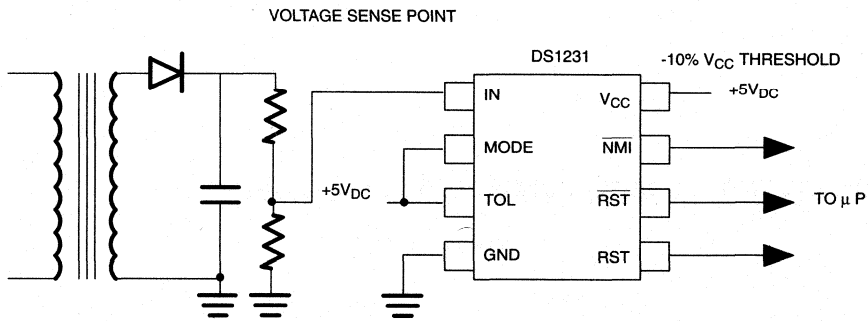
$$THEN\ 8 = \frac{R1 + 10K}{10K} \times 2.3 \qquad R1 = 25K$$

NOTE: $\overline{RST}$ requires a pull–up resister.

APPLICATION – MODE PIN CONNECTED TO GROUND

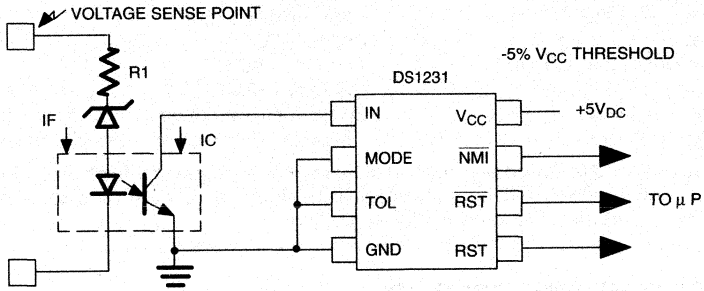
When the Mode pin is connected to ground, pin 1 is a current source of 30 µA with a V_{TP}+ of 2.5 volts. Pin 1 is held below the trip point by a switching device like an opto-isolator as shown in Figure 6. Determination of the sense point has the same criteria as discussed in the previous application. However, determining component values is significantly different. In this mode, the maximum dynamic range of the sense point versus desired trip voltage is primarily determined by the selection of a zener diode. As an example, if the maximum voltage at the sense point is 200V and the desired trip point is 150V, then a zener diode of 150V will approximately set the trip point. This is particularly true if power consumption on the high voltage side of the opto-isolator is not an issue. However, if power consumption is a concern, then it is desirable to make the value of R1 high. As the value of R1 increases, the effect of the LED current in the opto-isolator starts to affect the IN trip point. This can be seen from the equation shown in Figure 6. R1 must also be low enough to allow the opto-isolator to sink the 30 µA of collector current required by pin 1 and still have enough resistance to keep the maximum current through the opto-isolator's LED within data sheet limits. Figure 7 illustrates how the DS1231 can be interfaced to the AC power line when the mode pin is grounded.

AC VOLTAGE MONITOR WITH TRANSFORMER ISOLATION Figure 5



NOTE: $\overline{RST}$ requires a pull–up resister.

APPLICATION WITH MODE PIN GROUNDED Figure 6



$$\text{VOLTAGE SENSE POINT (TRIP VALUE)} = VZ + \frac{IC}{CTR} \times R1$$

$$CTR = \frac{IC}{IF}$$

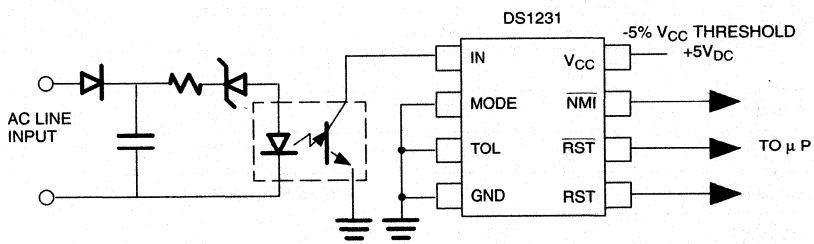
CTR = CURRENT TRANSFER RATIO
VZ = ZENNER VOLTAGE

EXAMPLE: CTR = 0.2 IC = 30 μA IF = 150 μA
VOLTAGE SENSE POINT = 105 AND
VZ = 100 VOLTS

$$\text{THEN } 105 = 100 + \frac{30}{0.2} \times R1 \qquad R1 = 33K$$

NOTE: $\overline{RST}$ requires a pull–up resister.

AC VOLTAGE MONITOR WITH OPTO-ISOLATION Figure 7



NOTE: $\overline{RST}$ requires a pull–up resister.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	-0.5V to +7.0V
Voltage on I/O Relative to Ground	-0.5V to V_{CC} + 0.5V
Operating Temperature	0°C to 70°C
Operating Temperature (Industrial Version)	–40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input Pin 1	V_{IN}			V_{CC}	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Low Level @ RST	V_{OL}			0.4	V	1
Output Voltage @ –500 µA	V_{OH}	V_{CC}–0.5V	V_{CC}–0.1V		V	1, 6
Input Leakage	I_{IL}	-10		+10	µA	2
Output Current @2.4V	I_{OH}	1.0	2.0		mA	5
Output Current @0.4V	I_{OL}	2.0	3.0		mA	
Operating Current	I_{CC}		0.5	2.0	mA	3
Input Pin 1 (Mode=GND)	I_C	15	25	50	µA	
Input Pin 1 (Mode=V_{CC})	I_C			0.1	µA	
IN Trip Piont (Mode=GND)	V_{TP}	See Figure 3				1
IN Trip Point (Mode=V_{CC})	V_{TP}					1
V_{CC} Trip Point (TOL=GND)	V_{CCTP}	4.50	4.62	4.74	V	1
V_{CC} Trip Point (TOL=V_{CC})	V_{CCTP}	4.25	4.37	4.49	V	1

CAPACITANCE

(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

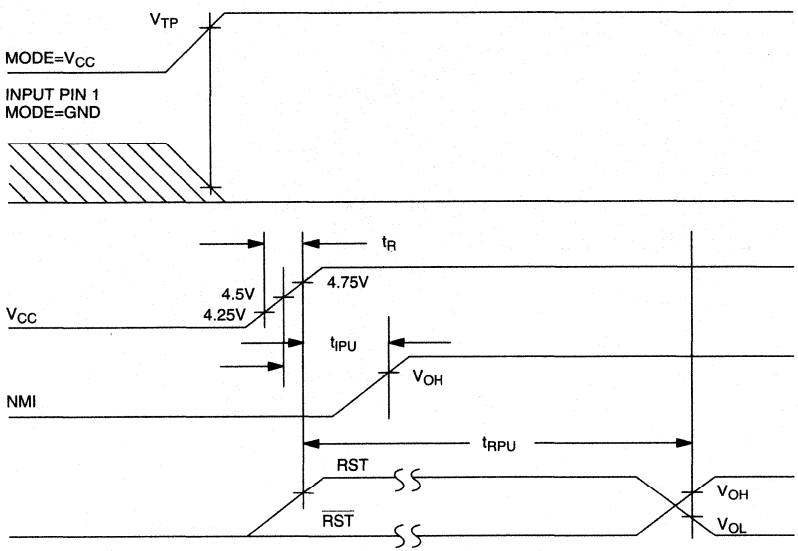
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{TP} to $\overline{NMI}$ Delay	t_{IPD}			1.1	µs	
V_{CC} Slew Rate 4.75-4.25V	t_F	300			µs	
V_{CC} Detect to RST and $\overline{RST}$	t_{RPD}			100	ns	
V_{CC} Detect to $\overline{NMI}$	t_{IPU}			200	µs	4
V_{CC} Detect to RST and $\overline{RST}$	t_{RPU}	150	500	1000	ms	4
V_{CC} Slew Rate 4.25-4.75V	t_R	0			ns	

3

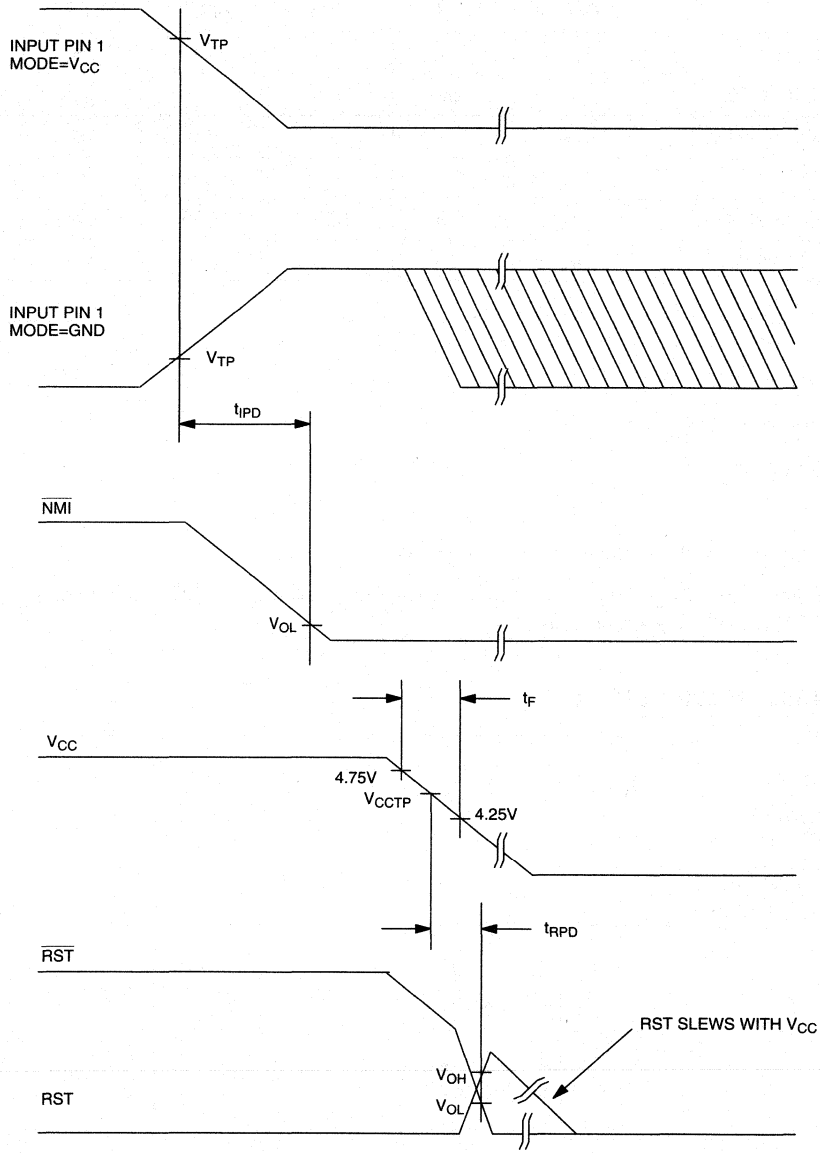
NOTES:

1. All voltages referenced to ground.
2. V_{CC} = +5.0 volts with outputs open.
3. Measured with outputs open.
4. t_R = 5 µs.
5. $\overline{RST}$ is an open drain output and requires a pull–up resister.
6. RST remains within 0.5V of V_{CC} on power–down until V_{CC} drops below 2.0V. $\overline{RST}$ remains within 0.5V of GND on power–down until V_{CC} drops below 2.0V.

TIMING DIAGRAM: POWER-UP



TIMING DIAGRAM: POWER-DOWN



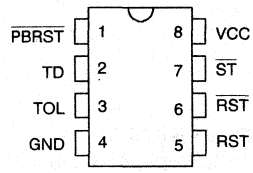
DALLAS SEMICONDUCTOR

DS1232
MicroMonitor Chip

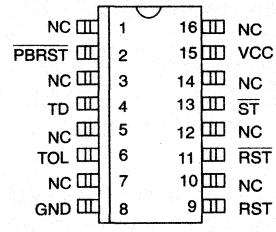
FEATURES

- Halts and restarts an out-of-control microprocessor
- Holds microprocessor in check during power transients
- Automatically restarts microprocessor after power failure
- Monitors pushbutton for external override
- Accurate 5% or 10% microprocessor power supply monitoring
- Eliminates the need for discrete components
- Space-saving, 8-pin mini-DIP
- Optional 16-pin SOIC surface mount package
- Industrial temperature -40°C to +85°C available, designated N

PIN ASSIGNMENT



DS1232 8-Pin DIP
(300 Mil)
See Mech. Drawings
Section



DS1232S 16-Pin SOIC
(300 Mil)
See Mech. Drawings
Section

PIN DESCRIPTION

PBRST	–	Pushbutton Reset Input
TD	–	Time Delay Set
TOL	–	Selects 5% or 10% V_{CC} Detect
GND	–	Ground
RST	–	Reset Output (Active High)
RST	–	Reset Output (Active Low, open drain)
ST	–	Strobe Input
V_{CC}	–	+5 Volt Power
NC	–	No Connections

DESCRIPTION

The DS1232 MicroMonitor Chip monitors three vital conditions for a microprocessor: power supply, software execution, and external override. First, a precision temperature-compensated reference and comparator circuit monitors the status of V_{CC}. When an out-of-tolerance condition occurs, an internal power fail signal is generated which forces reset to the active state. When V_{CC} returns to an in-tolerance condition, the reset signals are kept in the active state for a minimum of 250 ms to allow the power supply and processor to stabilize.

The second function the DS1232 performs is pushbutton reset control. The DS1232 debounces the pushbutton input and guarantees an active reset pulse width of 250 ms minimum. The third function is a watchdog timer. The DS1232 has an internal timer that forces the reset signals to the active state if the strobe input is not driven low prior to time-out. The watchdog timer function can be set to operate on time-out settings of approximately 150 ms, 600 ms, and 1.2 seconds.

OPERATION - POWER MONITOR

The DS1232 detects out-of-tolerance power supply conditions and warns a processor-based system of impending power failure. When V_{CC} falls below a preset level as defined by TOL (Pin 3), the V_{CC} comparator outputs the signals RST (Pin 5) and $\overline{RST}$ (Pin 6). When TOL is connected to ground, the RST and $\overline{RST}$ signals become active as V_{CC} falls below 4.75 volts. When TOL is connected to V_{CC}, the RST and $\overline{RST}$ signals become active as V_{CC} falls below 4.5 volts. The RST and $\overline{RST}$ are excellent control signals for a microprocessor, as processing is stopped at the last possible moments of valid V_{CC}. On power-up, RST and $\overline{RST}$ are kept active for a minimum of 250 ms to allow the power supply and processor to stabilize.

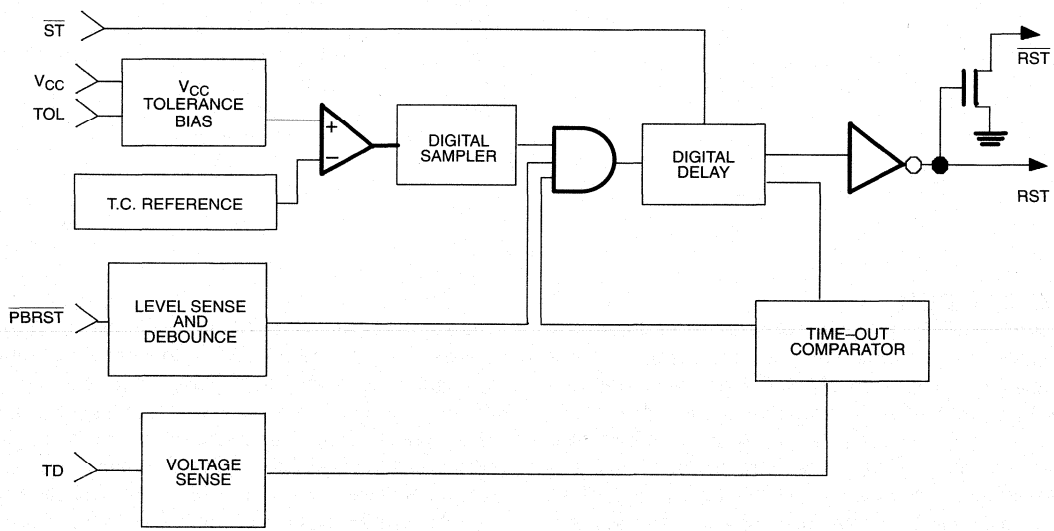
OPERATION - PUSHBUTTON RESET

The DS1232 provides an input pin for direct connection to a pushbutton (Figure 2). The pushbutton reset input requires an active low signal. Internally, this input is debounced and timed such that RST and $\overline{RST}$ signals of at least 250 ms minimum are generated. The 250 ms delay starts as the pushbutton reset input is released from low level.

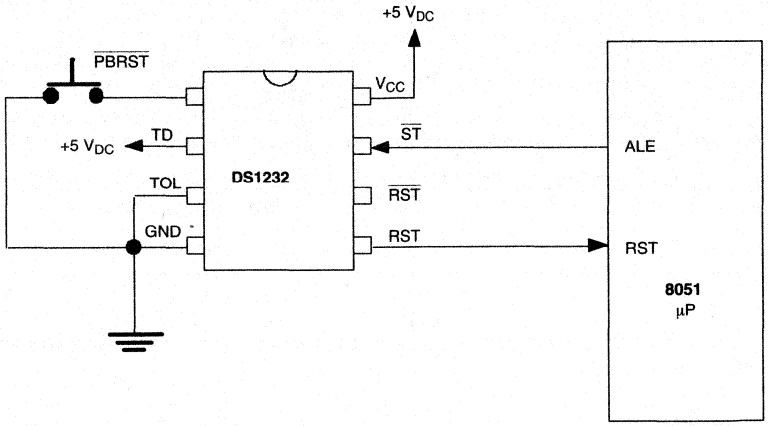
OPERATION - WATCHDOG TIMER

A watchdog timer function forces RST and $\overline{RST}$ signals to the active state when the $\overline{ST}$ input is not stimulated for a predetermined time period. The time period is set by the TD input to be typically 150 ms with TD connected to ground, 600 ms with TD left unconnected, and 1.2 seconds with TD connected to V_{CC}. The watchdog timer starts timing out from the set time period as soon as RST and $\overline{RST}$ are inactive. If a high-to-low transition occurs on the $\overline{ST}$ input pin prior to time-out, the watchdog timer is reset and begins to time-out again. If the watchdog timer is allowed to time-out, then the RST and $\overline{RST}$ signals are driven to the active state for 250 ms minimum. The $\overline{ST}$ input can be derived from microprocessor address signals, data signals, and/or control signals. When the microprocessor is functioning normally, these signals would, as a matter of routine, cause the watchdog to be reset prior to time-out. To guarantee that the watchdog timer does not time-out, a high-to-low transition must occur at or less than the minimum shown in Table 1. A typical circuit example is shown in Figure 3.

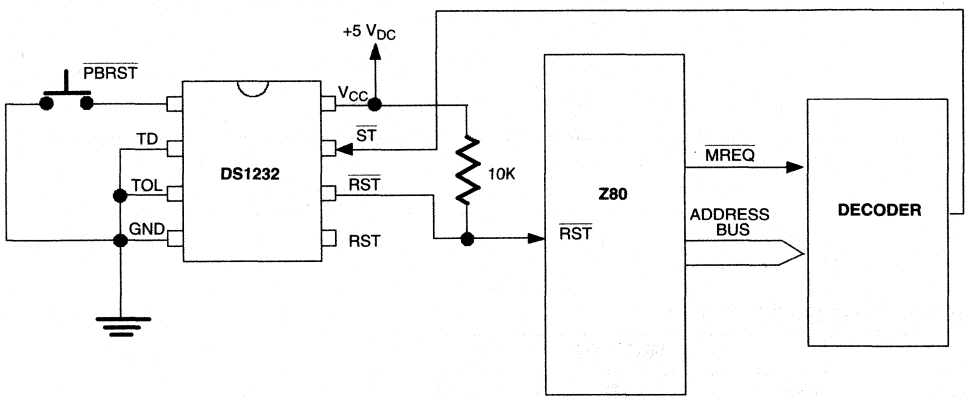
MICROMONITOR BLOCK DIAGRAM Figure 1



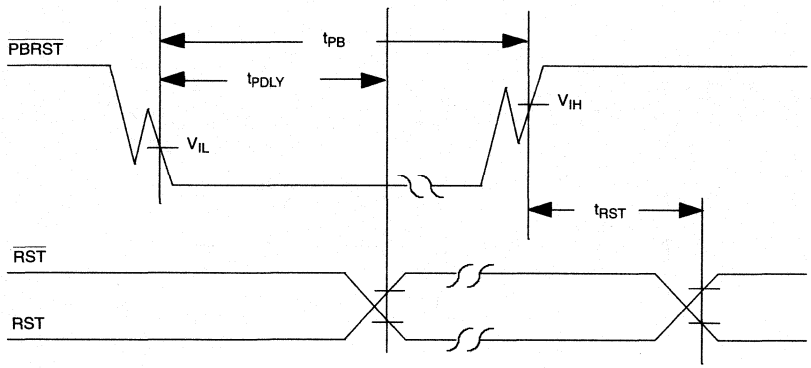
PUSHBUTTON RESET Figure 2



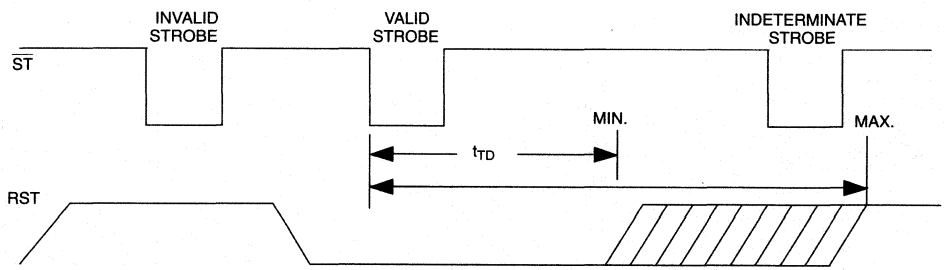
WATCHDOG TIMER Figure 3



TIMING DIAGRAM: PUSHBUTTON RESET Figure 4



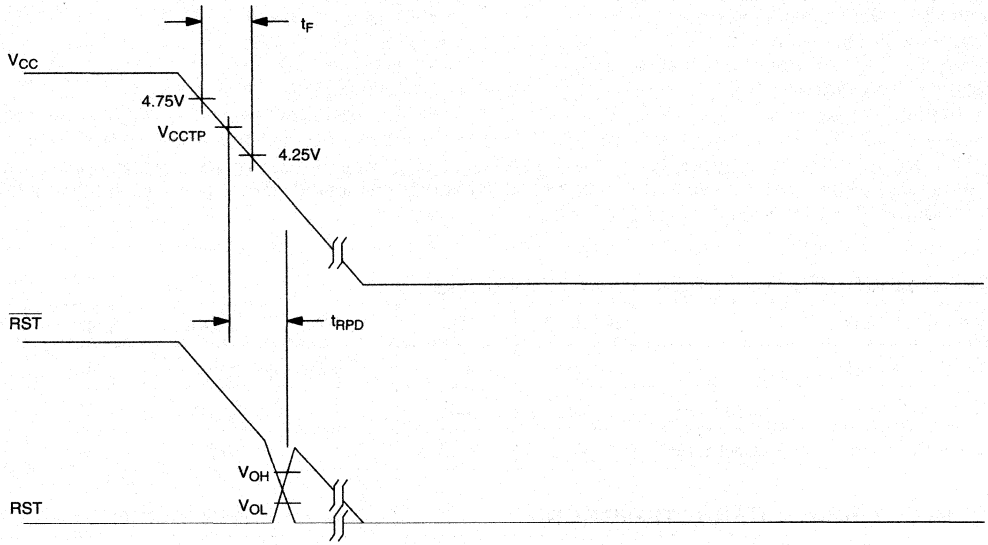
TIMING DIAGRAM: STROBE INPUT Figure 5



WATCHDOG TIMEOUTS Table 1

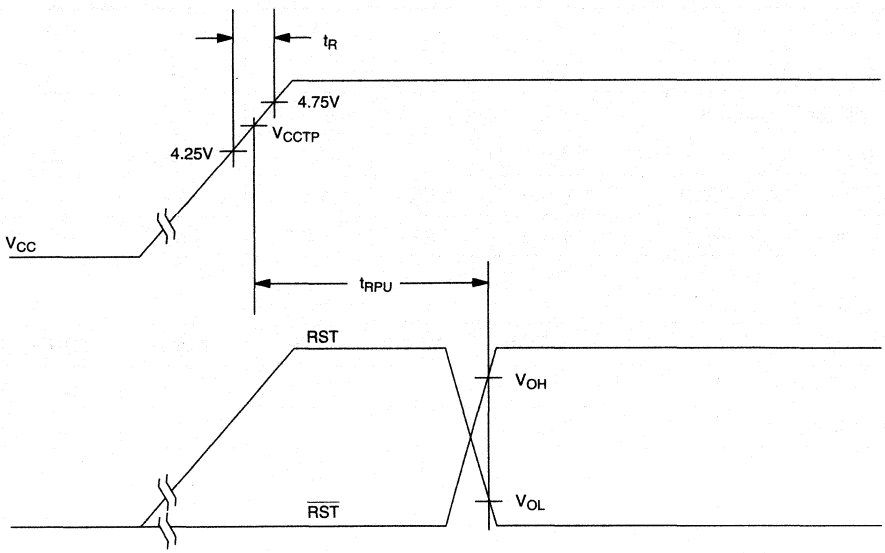
TD PIN	TIME-OUT		
	MIN	TYP	MAX
GND	62.5 ms	150 ms	250 ms
Float	250 ms	600 ms	1000 ms
V_{CC}	500 ms	1200 ms	2000 ms

TIMING DIAGRAM: POWER DOWN Figure 6



3

TIMING DIAGRAM: POWER UP Figure 7



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	-0.5V to +7.0V
Voltage on I/O Relative to Ground	–0.5V to V_{CC} + 0.5V
Operating Temperature	0°C to 70°C
Operating Temperature (Industrial Version)	–40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
$\overline{ST}$ and $\overline{PBRST}$ Input High Level	V_{IH}	2.0		V_{CC}+0.3	V	1
$\overline{ST}$ and $\overline{PBRST}$ Input Low Level	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-1.0		+1.0	µA	3
Output Current @ 2.4V	I_{OH}	-8	-10		mA	5
Output Current @ 0.4V	I_{OL}	8	10		mA	
Low Level @ RST	V_{OL}			0.4	V	1
Output Voltage @ -500 µA	V_{OH}	V_{CC} -0.5V	V_{CC} -0.1V		V	1, 7
Operating Current	I_{CC}		0.5	2.0	mA	2
V_{CC} Trip Point (TOL = GND)	V_{CCTP}	4.50	4.62	4.74	V	1
V_{CC} Trip Point (TOL = V_{CC})	V_{CCTP}	4.25	4.37	4.49	V	1

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{PBRST}$ = V_{IL}	t_{PB}	20			ms	
RESET Active Time	t_{RST}	250	610	1000	ms	
$\overline{ST}$ Pulse Width	t_{ST}	20			ns	6, 8
V_{CC} Fail Detect to RST and $\overline{RST}$	t_{RPD}	40	100	175	µs	
V_{CC} Slew Rate 4.75V to 4.25V	t_F	300			µs	
V_{CC} Detect to RST and $\overline{RST}$ Transition	t_{RPU}	250	610	1000	ms	4
V_{CC} Slew Rate 4.25V to 4.75V	t_R	0	5		µs	
$\overline{PBRST}$ Stable Low to RST and $\overline{RST}$	t_{PDLY}			20	ms	

3

NOTES:

1. All voltages referenced to ground.
2. Measured with outputs open.
3. $\overline{PBRST}$ is internally pulled up to V_{CC} with an internal impedance of 10K typical.
4. t_R = 5 µs.
5. $\overline{RST}$ is an open drain output.
6. Must not exceed t_{TD} minimum. See Table 1.
7. RST remains within 0.5V of V_{CC} on power-down until V_{CC} drops below 2.0V. $\overline{RST}$ remains within 0.5V of GND on power-down until V_{CC} drops below 2.0V.
8. Watchdog can not be disabled. It must be strobed to avoid resets.

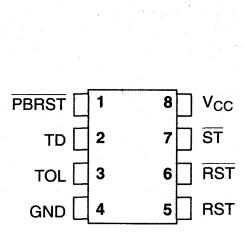
DALLAS SEMICONDUCTOR

DS1232LP/LPS
Low Power MicroMonitor Chip

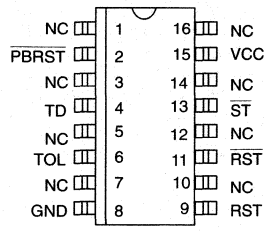
FEATURES

- Super low-power version of DS1232
- 50 µA quiescent current
- Halts and restarts an out-of-control microprocessor
- Automatically restarts microprocessor after power failure
- Monitors pushbutton for external override
- Accurate 5% or 10% microprocessor power supply monitoring
- 8-pin DIP or 8-pin SOIC package
- Optional 16-pin SOIC package available
- Industrial temperature -40°C to +85°C available, designated N

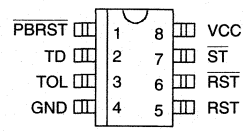
PIN ASSIGNMENT



DS1232LP 8-Pin DIP
(300 Mil)
See Mech. Drawings
Section



DS1232LPS 16-Pin SOIC
(300 Mil)
See Mech. Drawings
Section



DS1232LPS-2 8-Pin SOIC
(150 Mil)
See Mech. Drawings
Section

PIN DESCRIPTION

$\overline{\text{PBRST}}$	–	Pushbutton Reset Input
TD	–	Time Delay Set
TOL	–	Selects 5% or 10% V_{CC} Detect
GND	–	Ground
RST	–	Reset Output (Active High)
$\overline{\text{RST}}$	–	Reset Output (Active Low, open drain)
$\overline{\text{ST}}$	–	Strobe Input
V_{CC}	–	+5 Volt Power

DESCRIPTION

The DS1232LP/LPS Low Power MicroMonitor Chip monitors three vital conditions for a microprocessor: power supply, software execution, and external override. First, a precision temperature-compensated reference and comparator circuit monitors the status of V_{CC}. When an out-of-tolerance condition occurs, an internal power fail signal is generated which forces reset to the active state. When V_{CC} returns to an in-tolerance condition, the reset signals are kept in the active state for a minimum of 250 ms to allow the power supply and processor to stabilize.

The second function the DS1232LP/LPS performs is pushbutton reset control. The DS1232LP/LPS debounces the pushbutton input and guarantees an active reset pulse width of 250 ms minimum. The third function is a watchdog timer. The DS1232LP/LPS has an internal timer that forces the reset signals to the active state if

the strobe input is not driven low prior to time-out. The watchdog timer function can be set to operate on time-out settings of approximately 150 ms, 600 ms, and 1.2 seconds.

OPERATION - POWER MONITOR

The DS1232LP/LPS detects out-of-tolerance power supply conditions and warns a processor-based system of impending power failure. When V_{CC} falls below a preset level as defined by TOL, the V_{CC} comparator outputs the signals RST and $\overline{RST}$. When TOL is connected to ground, the RST and $\overline{RST}$ signals become active as V_{CC} falls below 4.75 volts. When TOL is connected to V_{CC}, the RST and $\overline{RST}$ signals become active as V_{CC} falls below 4.5 volts. The RST and $\overline{RST}$ are excellent control signals for a microprocessor, as processing is stopped at the last possible moments of valid V_{CC}. On power-up, RST and $\overline{RST}$ are kept active for a minimum of 250 ms to allow the power supply and processor to stabilize.

OPERATION - PUSHBUTTON RESET

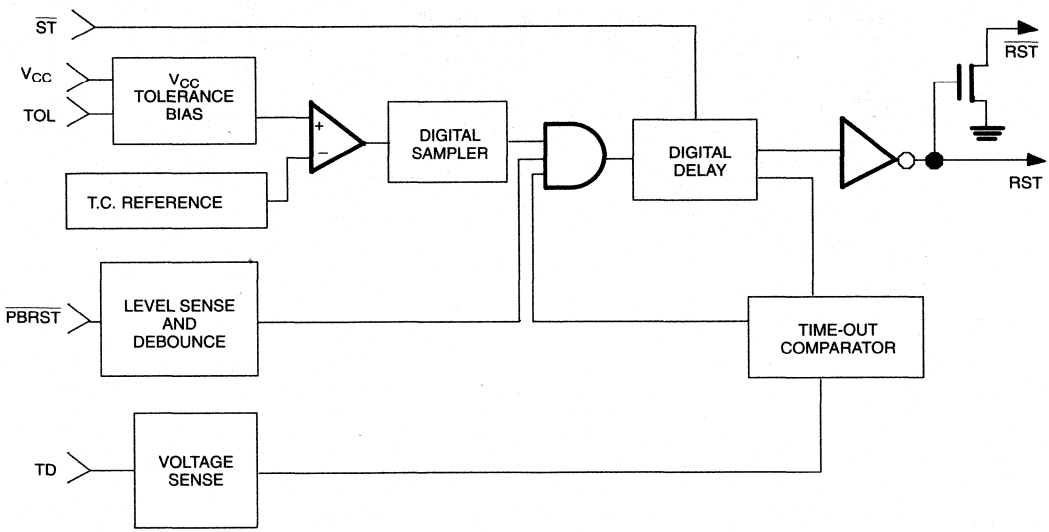
The DS1232LP/LPS provides an input pin for direct connection to a pushbutton (Figure 1). The pushbutton reset input requires an active low signal. Internally, this input is debounced and timed such that RST and $\overline{RST}$ signals of at least 250 ms minimum are generated. The 250 ms delay starts as the pushbutton reset input is released from low level.

OPERATION - WATCHDOG TIMER

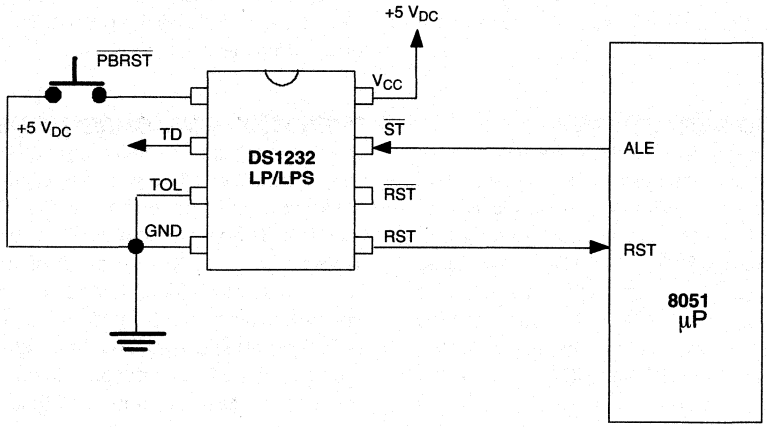
The watchdog timer function forces RST and $\overline{RST}$ signals to the active state when the $\overline{ST}$ input is not stimulated for a predetermined time period. The time period is set by the TD input to be typically 150 ms with TD connected to ground, 600 ms with TD left unconnected, and 1.2 seconds with TD connected to V_{CC}. The watchdog timer starts timing out from the set time period as soon as RST and $\overline{RST}$ are inactive. If a high-to-low transition occurs on the $\overline{ST}$ input pin prior to time-out, the watchdog timer is reset and begins to time-out again. If the watchdog timer is allowed to time-out, then the RST and $\overline{RST}$ signals are driven to the active state for 250 ms minimum. The $\overline{ST}$ input can be derived from microprocessor address signals, data signals, and/or control signals. When the microprocessor is functioning normally, these signals would, as a matter of routine, cause the watchdog to be reset prior to time-out. To guarantee that the watchdog timer does not time-out, a high-to-low transition must occur at or less than the minimum shown in Table 1. A typical circuit example is shown in Figure 2.

3

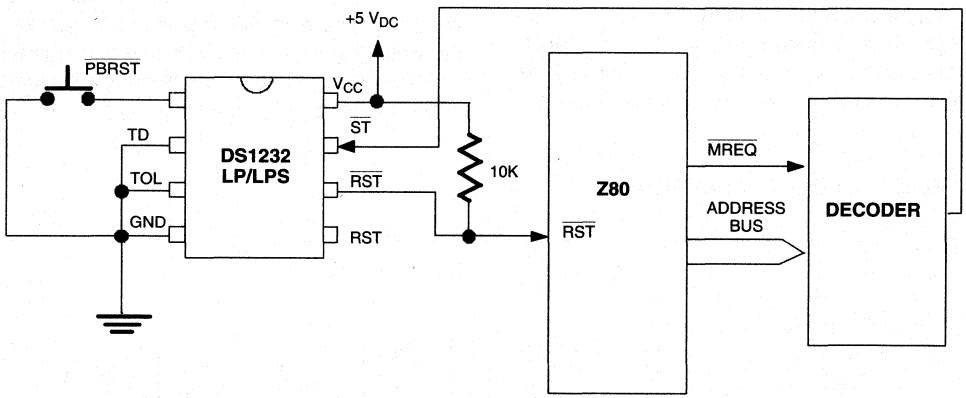
MICROMONITOR BLOCK DIAGRAM



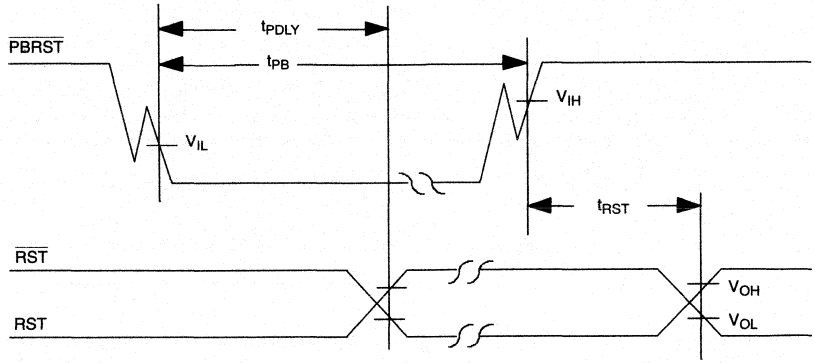
PUSHBUTTON RESET Figure 1



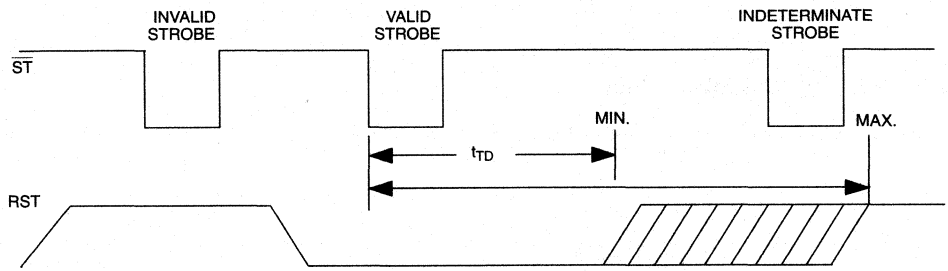
WATCHDOG TIMER Figure 2



TIMING DIAGRAM: PUSHBUTTON RESET Figure 3



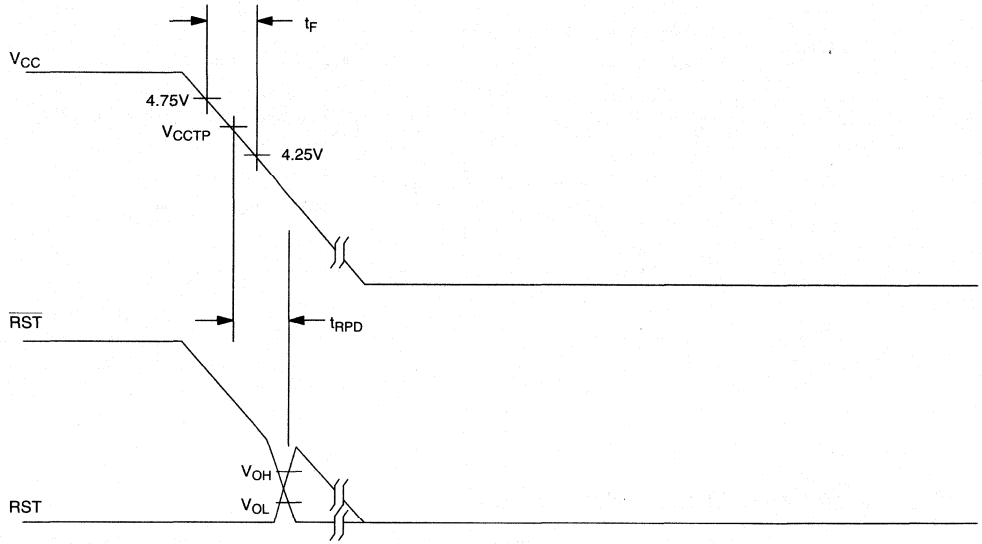
TIMING DIAGRAM: STROBE INPUT Figure 4



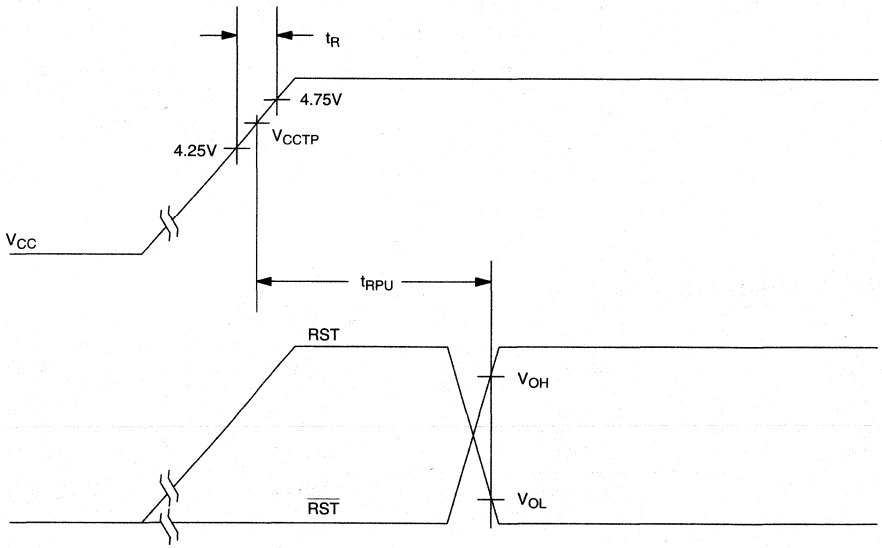
WATCHDOG TIME-OUTS Table 1

TD	TIME-OUT		
	MIN	TYP	MAX
GND	62.5 ms	150 ms	250 ms
Float	250 ms	600 ms	1000 ms
V_{CC}	500 ms	1200 ms	2000 ms

TIMING DIAGRAM: POWER DOWN Figure 5



TIMING DIAGRAM: POWER UP Figure 6



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	-0.5V to +7.0V
Voltage on I/O Relative to Ground	–0.5V to V_{CC} + 0.5V
Operating Temperature	0°C to 70°C
Operating Temperature (Industrial Version)	–40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
$\overline{ST}$ and $\overline{PBRST}$ Input High Level	V_{IH}	2.0		V_{CC}+0.3	V	1
$\overline{ST}$ and $\overline{PBRST}$ Input Low Level	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-1.0		+1.0	µA	3
Output Current @ 2.4V	I_{OH}	-8	-10		mA	5
Output Current @ 0.4V	I_{OL}	10			mA	
Low Level @ RST	V_{OL}			0.4	V	1
Output Voltage @ -500 uA	V_{OH}	V_{CC} -0.5V	V_{CC} -0.1V		V	1, 7
Operating Current (CMOS)	I_{CC1}			50	µA	2
Operating Current (TTL)	I_{CC2}		200	500	µA	8
V_{CC} Trip Point (TOL = GND)	V_{CCTP}	4.50	4.62	4.74	V	1
V_{CC} Trip Point (TOL = V_{CC})	V_{CCTP}	4.25	4.37	4.49	V	1

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{PBRST}$ = V_{IL}	t_{PB}	20			ms	
RESET Active Time	t_{RST}	250	610	1000	ms	
$\overline{ST}$ Pulse Width	t_{ST}	20			ns	6, 9
V_{CC} Fail Detect to RST and $\overline{RST}$	t_{RPD}		50	175	µs	
V_{CC} Slew Rate 4.75V to 4.25V	t_F	300			µs	
V_{CC} Detect to RST and $\overline{RST}$ Inactive	t_{RPU}	250	610	1000	ms	4
V_{CC} Slew Rate 4.25V to 4.75V	t_R	0			ns	
$\overline{PBRST}$ Stable Low to $\overline{RST}$ and RST	t_{PDLY}			20	ms	

NOTES:

1. All voltages referenced to ground.
2. Measured with outputs open and $\overline{ST}$ and $\overline{PBRST}$ within 0.5V of supply rails.
3. $\overline{PBRST}$ is internally pulled up to V_{CC} with an internal impedance of 40K typical.
4. t_R = 5 µs.
5. $\overline{RST}$ is an open drain output.
6. Must not exceed t_{TD} minimum. See Table 1.
7. RST remains within 0.5V of V_{CC} on power-down until V_{CC} drops below 2.0V. $\overline{RST}$ remains within 0.5V of GND on power-down until V_{CC} drops below 2.0V.
8. Measured with outputs open and $\overline{ST}$ and $\overline{PBRST}$ at TTL levels.
9. Watchdog can not be disabled. It must be strobed to avoid resets.

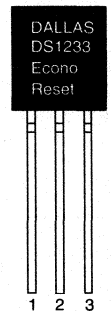
DALLAS SEMICONDUCTOR

DS1233
5V EconoReset

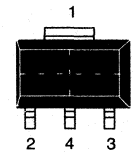
FEATURES

- Automatically restarts microprocessor after power failure
- Monitors pushbutton for external override
- Internal circuitry debounces pushbutton switch
- Maintains reset for 350 ms after V_{CC} returns to an in-tolerance condition or pushbutton released
- Accurate 5%, 10% or 15% microprocessor 5V power supply monitoring
- Reduces need for discrete components
- Precision temperature-compensated voltage reference and voltage sensor
- Low-cost TO-92 package or surface mount SOT-223 package
- Internal 5KΩ pull-up resistor
- Operating temperature of –40°C to +85°C

PIN ASSIGNMENT



TO-92 Package
See Mech. Drawings Section



SOT-223 Package
See Mech. Drawings Section

PIN DESCRIPTION

PIN 1	GROUND
PIN 2	$\overline{\text{RESET}}$
PIN 3	V_{CC}
PIN 4	GROUND (SOT–223 ONLY)

DESCRIPTION

The DS1233 EconoReset monitors two vital conditions for a microprocessor: power supply and external override. A precision temperature compensated reference and comparator circuit are used to monitor the status of the power supply (V_{CC}). When an out-of-tolerance condition is detected, an internal power fail signal is generated which forces reset to the active state. When V_{CC} returns to an in-tolerance condition, the reset signal is kept in the active state for approximately 350 ms to allow the power supply and processor to stabilize. The second function of the DS1233 is pushbutton reset control. The DS1233 debounces a pushbutton closure and will generate a 350 ms reset pulse upon release.

OPERATION - POWER MONITOR

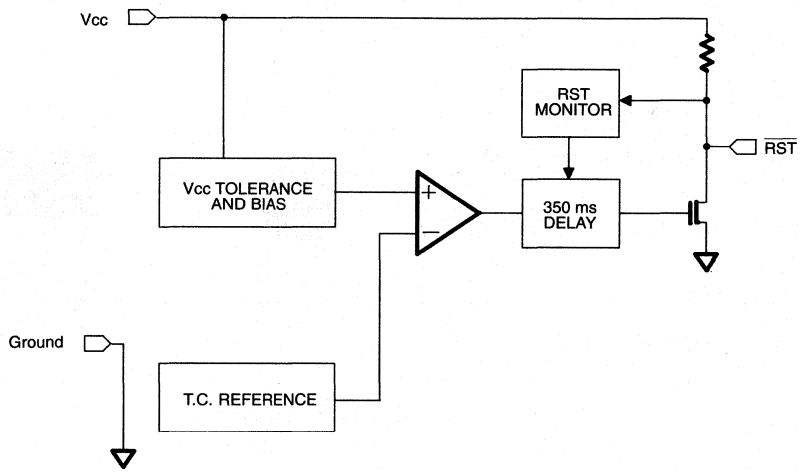
The DS1233 provides the functions of detecting out-of-tolerance power supply conditions and warning a processor-based system of impending power failure. When V_{CC} is detected as out-of-tolerance, as defined by the tolerance of the part selected, the $\overline{RST}$ signal is asserted. On power-up, $\overline{RST}$ is kept active for approximately 350 ms after the power supply has reached the selected tolerance. This allows the power supply and microprocessor to stabilize before $\overline{RST}$ is released.

OPERATION - PUSHBUTTON RESET

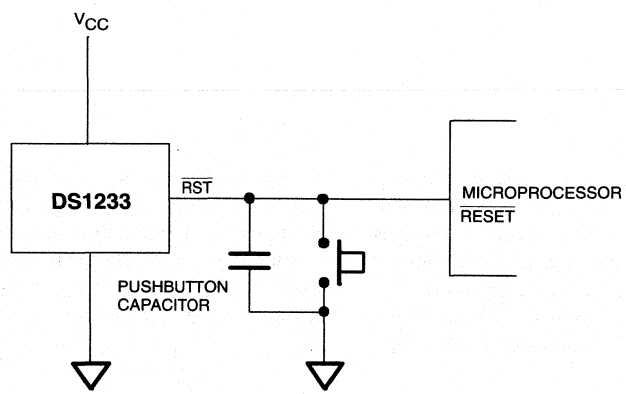
The DS1233 provides for a pushbutton switch to be connected to the $\overline{RST}$ output pin. When the DS1233 is not in a reset cycle, it continuously monitors the $\overline{RST}$ signal for a low going edge. If an edge is detected, the DS1233 will debounce the switch by pulling the $\overline{RST}$ line low. After the internal timer has expired, the DS1233 will continue to monitor the $\overline{RST}$ line. If the line is still low, the DS1233 will continue to monitor the line looking for a rising edge. Upon detecting a release, the DS1233 will force the $\overline{RST}$ line low and hold it low for 350 ms.

NOTE: For proper operation with an external pushbutton, a capacitor between 100 pF and 0.01 µF must be connected between $\overline{RST}$ and ground. In applications where additional reset current is required, a minimum capacitance of 500 pF should be used, along with a parallel external pull-up resistor of 1KΩ minimum.

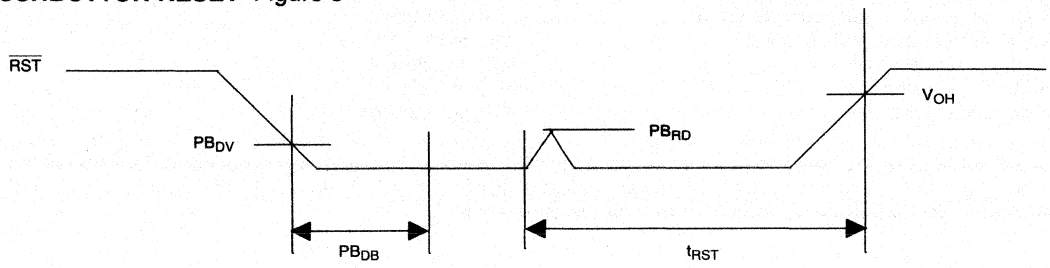
BLOCK DIAGRAM Figure 1



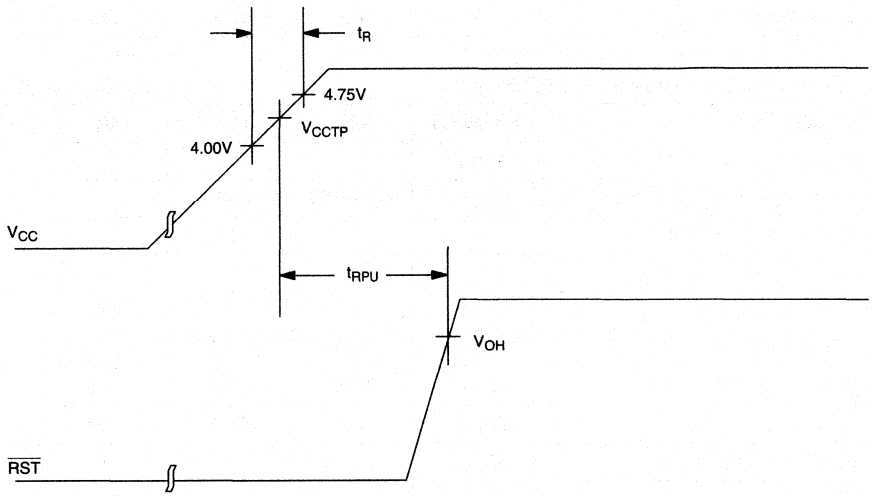
APPLICATION EXAMPLE Figure 2



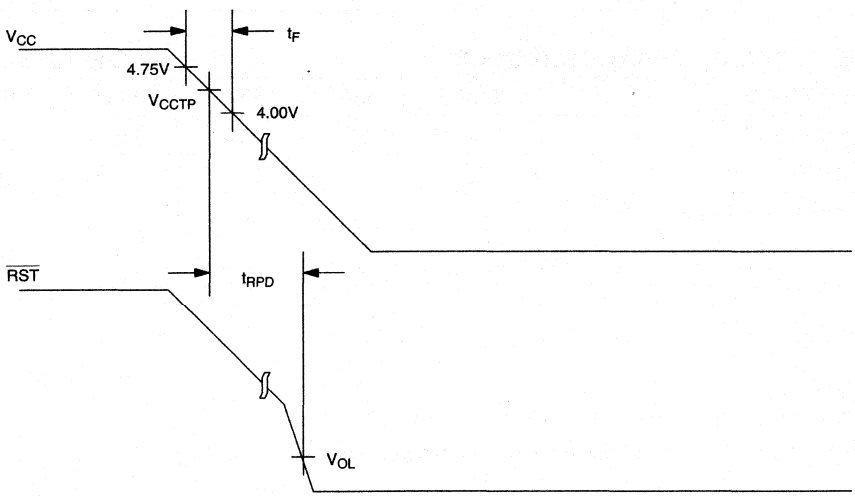
PUSHBUTTON RESET Figure 3



POWER UP Figure 4



POWER DOWN Figure 5



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	-0.5V to +7.0V
Voltage on I/O Relative to Ground	–0.5V to V_{CC} + 0.5V
Operating Temperature	–40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(–40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	1.2	5.0	5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Low Level @ $\overline{RST}$	V_{OL}			0.4	V	1
Output Voltage @ –500 µA	V_{OH}	V_{CC}–0.5V	V_{CC}–0.1V		V	1
Output Current @ 2.4V	I_{OH}		350		µA	
Output Current @ 0.4V	I_{OL}	+10			mA	
Operating Current	I_{CC}			50	µA	
V_{CC} Trip Point 5%	V_{CCTP0}	4.50	4.625	4.75	V	1
V_{CC} Trip Point 10%	V_{CCTP1}	4.25	4.375	4.49	V	1
V_{CC} Trip Point 15%	V_{CCTP2}	4.0	4.125	4.24	V	1
Output Capacitance	C_{OUT}			10	pF	
Pushbutton Detect	PB_{DV}	1.8		3.3	V	1
Pushbutton Release	PB_{RD}		0.3	0.8	V	1,2
Internal Pull-Up Resistor	R_P	3.75	5	6.25	KΩ	

AC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Reset Active Time	t_{RST}	250	350	450	ms	
V_{CC} Detect to $\overline{RST}$	t_{RPD}			100	ns	
V_{CC} Slew Rate (4.75V - 4.00V)	t_F	300			µs	
V_{CC} Slew Rate (4.00V - 4.75V)	t_R	0			ns	
Pushbutton Debounce	PB_{DB}	250	350	450	ms	
V_{CC} detect to RST	t_{RPU}	250	350	450	ms	

NOTES:

1. All voltages are referenced to ground.
2. With a 100 pF to 0.01 µF capacitor connected from $\overline{RST}$ to ground.

ECONORESET SELECTION GUIDE

		VCC TRIP POINT			PUSHBUTTON DETECT		
		MIN	TYP	MAX	MIN	TYP	MAX
5V	DS1233-15	4.0	4.125	4.24	2.4	–	3.3
	DS1233-10	4.25	4.375	4.49	2.4	–	3.3
	DS1233-5	4.5	4.625	4.75	2.4	–	3.3
	DS1233D–15	4.0	4.125	4.24	N/A		N/A
	DS1233D–10	4.25	4.375	4.49	N/A		N/A
	DS1233D–5	4.5	4.625	4.75	N/A		N/A
	DS1833–15	4.0	4.125	4.24	N/A		N/A
	DS1833–10	4.25	4.375	4.49	N/A		N/A
	DS1833–5	4.5	4.625	4.75	N/A		N/A
3.3V	DS1233A-15	2.64	2.72	2.80	1.8	–	3.0
	DS1233A-10	2.8	2.88	2.97	1.8	–	3.0

PRELIMINARY

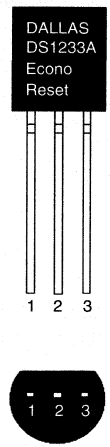
DALLAS SEMICONDUCTOR

DS1233A
3.3V EconoReset

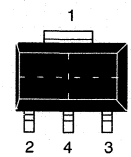
FEATURES

- Automatically restarts microprocessor after power failure
- Monitors pushbutton for external override
- Internal circuitry debounces pushbutton switch
- Maintains reset for 350 ms after V_{CC} returns to an in-tolerance condition or pushbutton released
- Accurate 10% or 15% microprocessor 3.3V power supply monitoring
- Reduces need for discrete components
- Precision temperature-compensated voltage reference and voltage sensor
- Low-cost TO-92 package or surface mount SOT-223 package
- Internal 5KΩ pull-up resistor
- Operating temperature of –40°C to +85°C

PIN ASSIGNMENT



TO-92 Package
See Mech. Drawings
Section



SOT-223 Package
See Mech. Drawings
Section

PIN DESCRIPTION

PIN 1	GROUND
PIN 2	$\overline{\text{RESET}}$
PIN 3	V_{CC}
PIN 4	GROUND (SOT–223 ONLY)

DESCRIPTION

The DS1233A EconoReset monitors two vital conditions for a microprocessor: power supply and external override. A precision temperature compensated reference and comparator circuit are used to monitor the status of the power supply (V_{CC}). When an out-of-tolerance condition is detected, an internal power fail signal is generated which forces reset to the active state. When V_{CC} returns to an in-tolerance condition, the reset signal is kept in the active state for approximately 350 ms to allow the power supply and processor to stabilize. The second function of the DS1233A is pushbutton reset control. The DS1233A debounces a pushbutton closure and will generate a 350 ms reset pulse upon release.

OPERATION – POWER MONITOR

The DS1233A provides the functions of detecting out-of-tolerance power supply conditions and warning a processor-based system of impending power failure. When V_{CC} is detected as out-of-tolerance, as defined by the tolerance of the part selected, the $\overline{RST}$ signal is asserted. On power-up, $\overline{RST}$ is kept active for approximately 350 ms after the power supply has reached the selected tolerance. This allows the power supply and microprocessor to stabilize before $\overline{RST}$ is released.

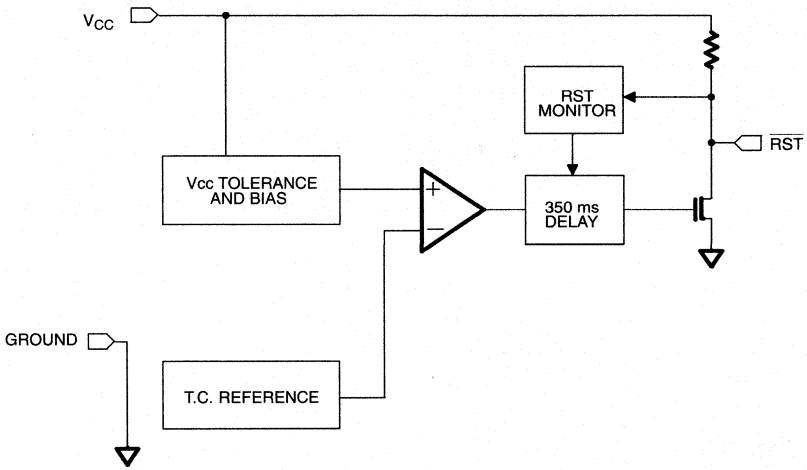
OPERATION – PUSHBUTTON RESET

The DS1233A provides for a pushbutton switch to be connected to the $\overline{RST}$ output pin. When the DS1233A is not in a reset cycle, it continuously monitors the $\overline{RST}$ signal for a low going edge. If an edge is detected, the DS1233A will debounce the switch by pulling the $\overline{RST}$ line low. After the internal timer has expired, the DS1233A will continue to monitor the $\overline{RST}$ line. If the line is still low, the DS1233A will continue to monitor the line looking for a rising edge. Upon detecting a release, the DS1233A will force the $\overline{RST}$ line low and hold it low for 350 ms.

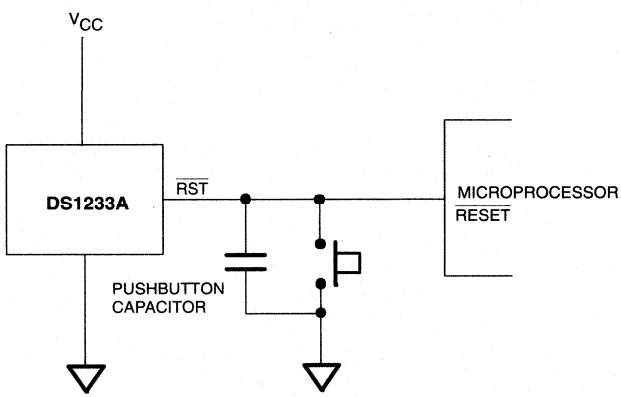
NOTE: For proper operation with an external pushbutton, a capacitor between 100 pF and 0.01 µF must be connected between $\overline{RST}$ and ground. In applications where additional reset current is required, a minimum capacitance of 500 pF should be used, along with a parallel external pull-up resistor of 1KΩ minimum.

3

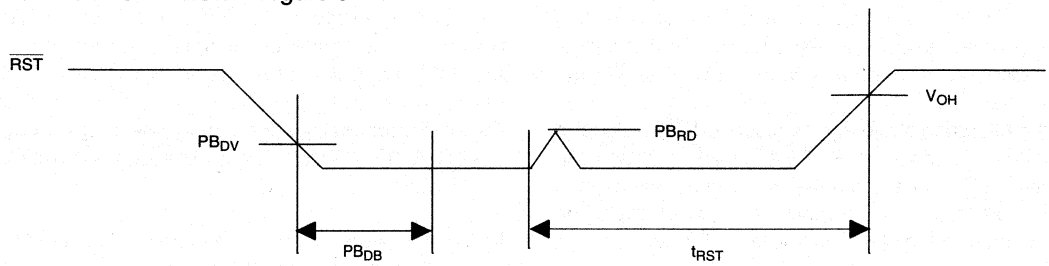
BLOCK DIAGRAM Figure 1



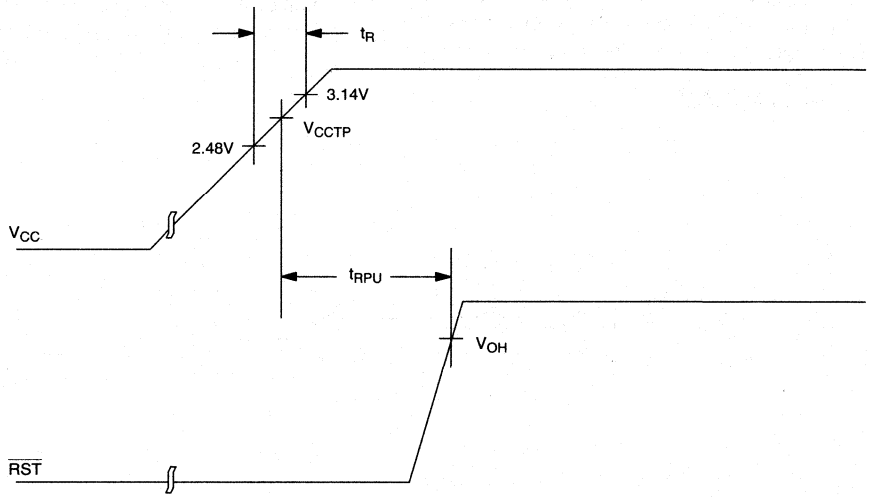
APPLICATION EXAMPLE Figure 2



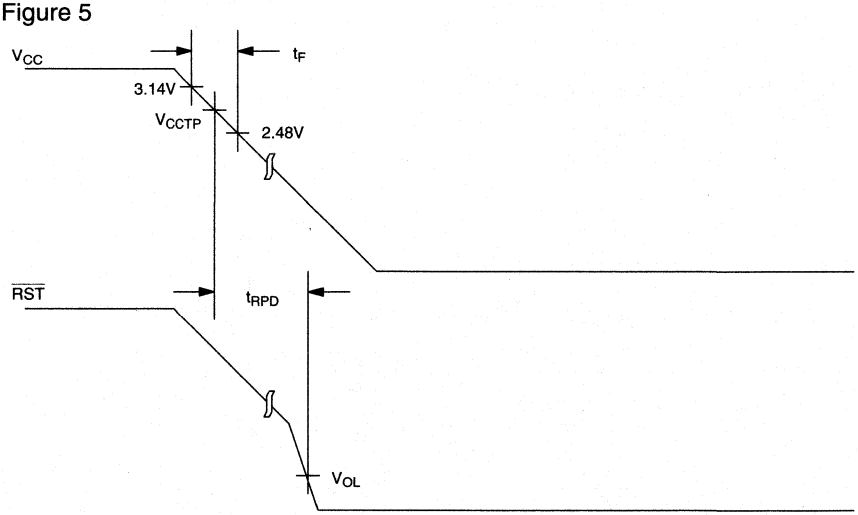
PUSHBUTTON RESET Figure 3



POWER UP Figure 4



POWER DOWN Figure 5



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	–0.5V to +7.0V
Voltage on I/O Relative to Ground	–0.5V to V_{CC} + 0.5V
Operating Temperature	–40°C to +85°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(–40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	1.2	3.3	5.5	V	1

3

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{DD} = 3.3V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Low Level @ $\overline{RST}$	V_{OL}			0.4	V	1
Output Voltage @ –500 µA	V_{OH}	V_{CC}–0.5V	V_{CC}–0.1V		V	1
Output Current @ 2.4V	I_{OH}		350		µA	
Output Current @ 0.4V	I_{OL}	+10			mA	
Operating Current	I_{CC}			50	µA	
V_{CC} Trip Point 10%	V_{CCTP1}	2.80	2.88	2.97	V	1
V_{CC} Trip Point 15%	V_{CCTP2}	2.64	2.72	2.80	V	1
Output Capacitance	C_{OUT}			10	pF	
Pushbutton Detect	PB_{DV}	.8		2.0	V	1
Pushbutton Release	PB_{RD}		0.3	0.8	V	1,2
Internal Pull-Up Resistor	R_P	3.75	5	6.25	KΩ	

AC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC} = 3.3V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Reset Active Time	t_{RST}	250	350	450	ms	
V_{CC} Detect to $\overline{RST}$	t_{RPD}			100	ns	
V_{CC} Slew Rate (2.85V – 2.3V)	t_F	300			µs	
V_{CC} Slew Rate (2.3V – 2.85V)	t_R	0			ns	
Pushbutton Debounce	PB_{DB}	250	350	450	ms	
V_{CC} detect to RST	t_{RPU}	250	350	450	ms	

NOTES:

1. All voltages are referenced to ground.
2. With a 100 pF to 0.01 µF capacitor connected from $\overline{RST}$ to ground.

ECONORESET SELECTION GUIDE

		VCC TRIP POINT			PUSHBUTTON DETECT		
		MIN	TYP	MAX	MIN	TYP	MAX
5V	DS1233-15	4.0	4.125	4.24	2.4	–	3.3
	DS1233-10	4.25	4.375	4.49	2.4	–	3.3
	DS1233-5	4.5	4.625	4.75	2.4	–	3.3
	DS1233D–15	4.0	4.125	4.24	N/A		N/A
	DS1233D–10	4.25	4.375	4.49	N/A		N/A
	DS1233D–5	4.5	4.625	4.75	N/A		N/A
	DS1833–15	4.0	4.125	4.24	N/A		N/A
	DS1833–10	4.25	4.375	4.49	N/A		N/A
	DS1833–5	4.5	4.625	4.75	N/A		N/A
3.3V	DS1233A-15	2.64	2.72	2.80	1.8	–	3.0
	DS1233A-10	2.8	2.88	2.97	1.8	–	3.0

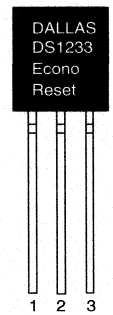
DALLAS SEMICONDUCTOR

DS1233D
5V EconoReset

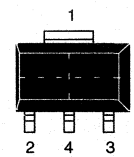
FEATURES

- Automatically restarts microprocessor after power failure
- Maintains reset for 350 ms after V_{CC} returns to an in-tolerance condition
- Accurate 5%, 10% or 15% microprocessor 5V power supply monitoring
- Reduces need for discrete components
- Precision temperature-compensated voltage reference and voltage sensor
- Low-cost TO-92 package or surface mount SOT-223 package
- Internal 5 KΩ pull-up resistor
- Compatible with Motorola 68XXX series and HC16 Microprocessors
- Operating temperature of –40°C to +85°C

PIN ASSIGNMENT



TO-92 Package
See Mech. Drawings Section



SOT-223 Package
See Mech. Drawings Section

PIN DESCRIPTION

PIN 1	GROUND
PIN 2	$\overline{\text{RESET}}$
PIN 3	V_{CC}
PIN 4	GROUND (SOT–223 ONLY)

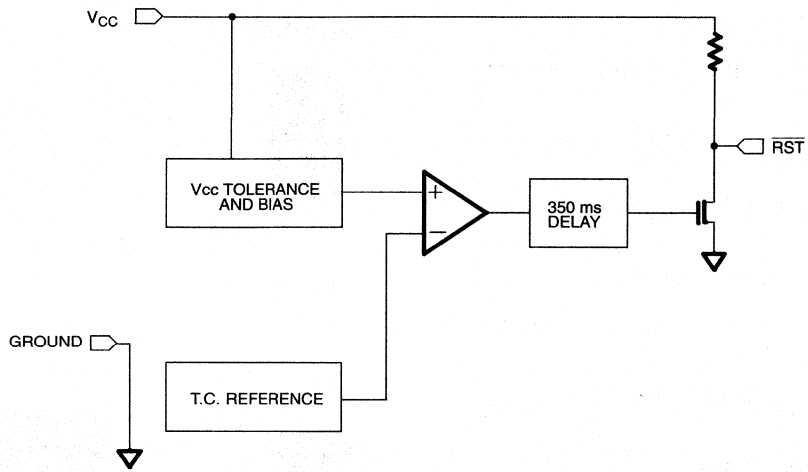
DESCRIPTION

The DS1233D EconoReset uses a precision temperature compensated reference and comparator circuit to monitor the status of the power supply (V_{CC}). When an out-of-tolerance condition is detected, an internal power fail signal is generated which forces reset to the active state. When V_{CC} returns to an in-tolerance condition, the reset signal is kept in the active state for approximately 350 ms to allow the power supply and processor to stabilize.

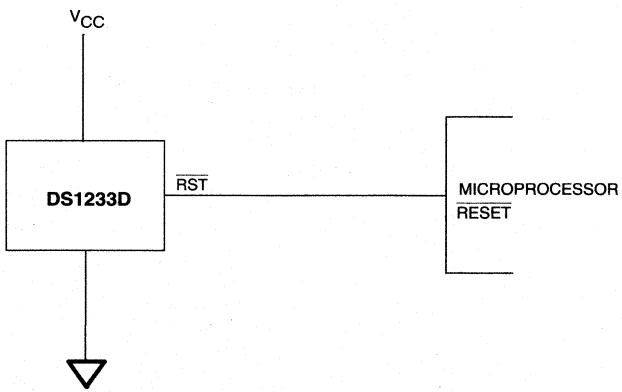
OPERATION - POWER MONITOR

The DS1233D provides the functions of detecting out-of-tolerance power supply conditions and warning a processor-based system of impending power failure. When V_{CC} is detected as out-of-tolerance, as defined by the tolerance of the part selected, the $\overline{RST}$ signal is asserted. On power-up, $\overline{RST}$ is kept active for approximately 350 ms after the power supply has reached the selected tolerance. This allows the power supply and microprocessor to stabilize before $\overline{RST}$ is released.

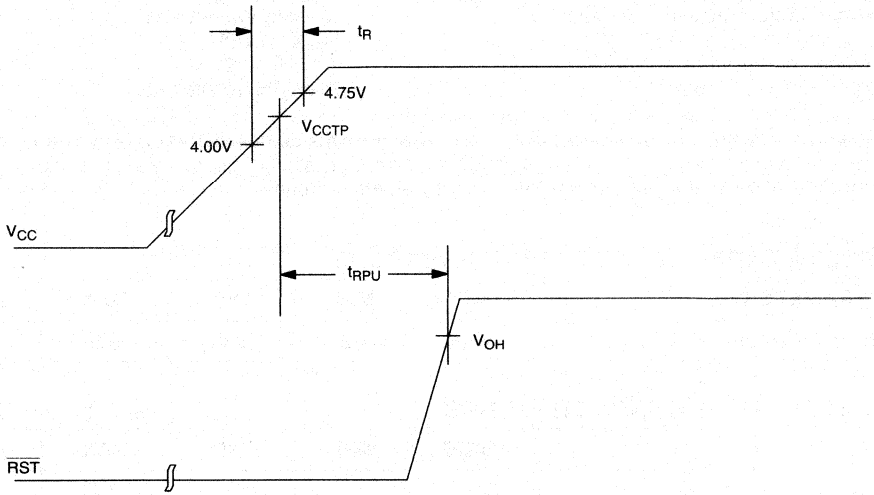
BLOCK DIAGRAM Figure 1



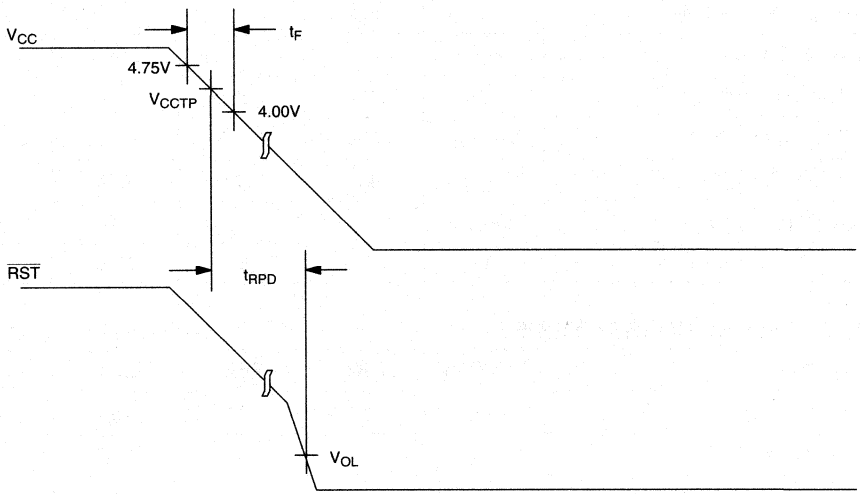
APPLICATION EXAMPLE Figure 2



POWER UP Figure 3



POWER DOWN Figure 4



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	-0.5V to +7.0V
Voltage on I/O Relative to Ground	–0.5V to V_{CC} + 0.5V
Operating Temperature	–40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(–40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	1.2	5.0	5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Low Level @ $\overline{RST}$	V_{OL}			0.4	V	1
Output Voltage @ –500 µA	V_{OH}	V_{CC}–0.5V	V_{CC}–0.1V		V	1
Output Current @ 2.4V	I_{OH}		350		µA	
Output Current @ 0.4V	I_{OL}	+10			mA	2
Operating Current	I_{CC}			50	µA	
V_{CC} Trip Point 5%	V_{CCTP1}	4.5	4.625	4.74	V	1
V_{CC} Trip Point 10%	V_{CCTP2}	4.25	4.375	4.49	V	1
V_{CC} Trip Point 15%	V_{CCTP3}	4.0	4.125	4.24	V	1
Output Capacitance	C_{OUT}			10	pF	
Internal Pull-Up Resistor	R_P	3.75	5	6.25	KΩ	

AC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Reset Active Time	t_{RST}	250	350	450	ms	
V_{CC} Detect to $\overline{RST}$	t_{RPD}			100	ns	
V_{CC} Slew Rate (4.75V - 4.00V)	t_F	300			µs	
V_{CC} Slew Rate (4.00V - 4.75V)	t_R	0			ns	
V_{CC} detect to RST	t_{RPU}	250	350	450	ms	

NOTES:

1. All voltages are referenced to ground.
2. A 1KΩ external resistor may be required for proper operation of the microprocessor reset control circuit.

ECONORESET SELECTION GUIDE

		VCC TRIP POINT			PUSHBUTTON DETECT		
		MIN	TYP	MAX	MIN	TYP	MAX
5V	DS1233-15	4.0	4.125	4.24	2.4	–	3.3
	DS1233-10	4.25	4.375	4.49	2.4	–	3.3
	DS1233-5	4.5	4.625	4.75	2.4	–	3.3
	DS1233D–15	4.0	4.125	4.24	N/A		N/A
	DS1233D–10	4.25	4.375	4.49	N/A		N/A
	DS1233D–5	4.5	4.625	4.75	N/A		N/A
	DS1833–15	4.0	4.125	4.24	N/A		N/A
	DS1833–10	4.25	4.375	4.49	N/A		N/A
	DS1833–5	4.5	4.625	4.75	N/A		N/A
3.3V	DS1233A-15	2.64	2.72	2.80	1.8	–	3.0
	DS1233A-10	2.8	2.88	2.97	1.8	–	3.0

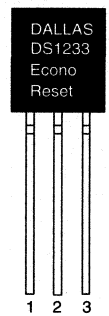
DALLAS SEMICONDUCTOR

DS1233M
EconoReset

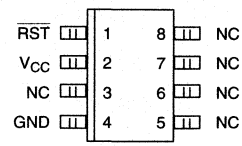
FEATURES

- Automatically restarts microprocessor after power failure
- Maintains reset for 350 ms after V_{CC} returns to an in-tolerance condition
- Reduces need for discrete components
- Precision temperature-compensated voltage reference and voltage sensor
- Low-cost TO-92 package or surface mount 8–pin SOIC packages available
- Internal 5 KΩ pull-up resistor
- Compatible with Motorola 68XXX series and HC16 Microprocessors
- Pin function compatible with the Motorola MC33064, MC34064, MC33164, and MC34164
- Operating temperature of –40°C to +85°C

PIN ASSIGNMENT



DS1233M
TO-92 Package
See Mech. Drawings
Section



DS1233M 8–PIN SOIC
(150 MIL)
See Mech. Drawings
Section

PIN DESCRIPTIONS

TO–92

1	$\overline{RST}$	– Active Low Reset Output
2	V_{CC}	– Power Supply
3	GND	– Ground

8–Pin SOIC

$\overline{RST}$	– Active Low Reset Output
V_{CC}	– Power Supply
NC	– No Connect
GND	– Ground

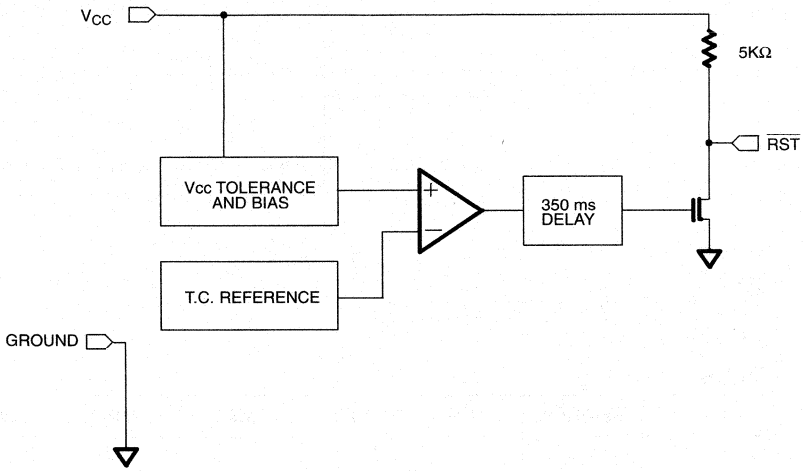
DESCRIPTION

The DS1233M EconoReset uses a precision temperature compensated reference and comparator circuit to monitor the status of the power supply (V_{CC}). When an out-of-tolerance condition is detected, an internal power fail signal is generated which forces reset to the active (low) state. When V_{CC} returns to an in-tolerance condition, the reset signal is kept in the active state for approximately 350 ms to allow the power supply and processor to stabilize.

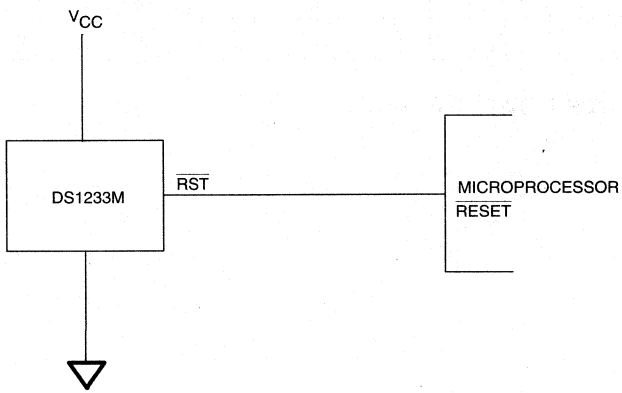
OPERATION – POWER MONITOR

The DS1233M provides the functions of detecting out-of-tolerance power supply conditions and warning a processor-based system of impending power failure. When V_{CC} is detected as out-of-tolerance, as defined by the tolerance of the part selected, the $\overline{RST}$ signal is asserted. On power-up, $\overline{RST}$ is kept active for approximately 350 ms after the power supply has reached the selected tolerance. This allows the power supply and microprocessor to stabilize before $\overline{RST}$ is released.

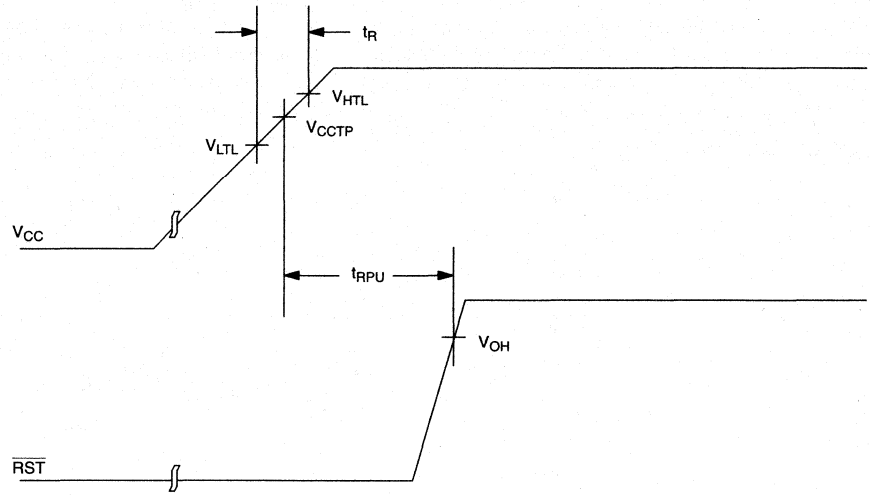
BLOCK DIAGRAM Figure 1



APPLICATION EXAMPLE Figure 2



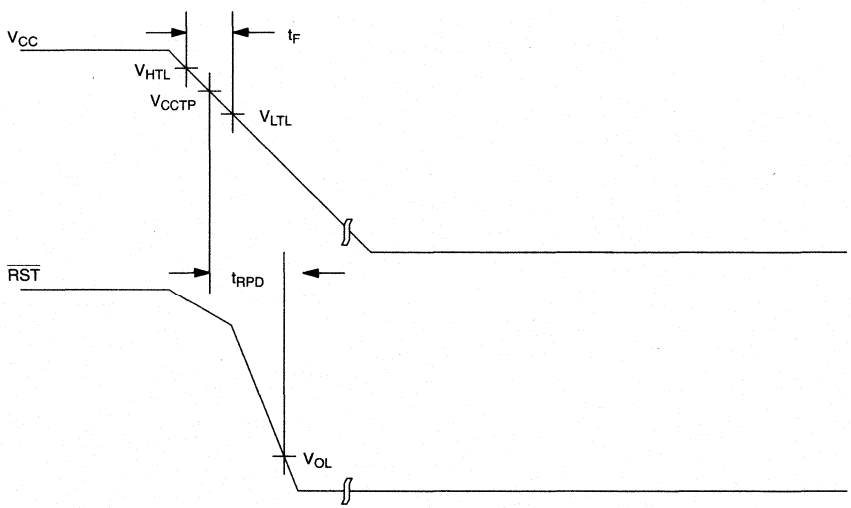
TIMING DIAGRAM: POWER UP Figure 3



VOLTAGE TRIP LEVELS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Voltage High Trip Level	V_{HTL}			4.75	V	DS1233M–5, DS1233M–55
Voltage Low Trip Level	V_{LTL}			4.00	V	DS1233M–5, DS1233M–55
Voltage High Trip Level	V_{HTL}			3.14	V	DS1233M–3
Voltage Low Trip Level	V_{LTL}			2.48	V	DS1233M–3

TIMING DIAGRAM: POWER DOWN Figure 4



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	-0.5V to +7.0V
Voltage on I/O Relative to Ground	–0.5V to V_{CC} + 0.5V
Operating Temperature	–40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(–40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	1.2		5.5	V	1

3

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC} = 1.2V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Voltage @ –500 µA	V_{OH}	V_{CC}–0.5V	V_{CC}–0.1V		V	1
Output Current @ 0.4V	I_{OL}	+8			mA	2, 3
Operating Current	I_{CC}			50	µA	4
V_{CC} Trip Point (DS1233M–5)	V_{CCTP}	4.25	4.375	4.49	V	1
V_{CC} Trip Point (DS1233M–55)	V_{CCTP}	4.5	4.625	4.75	V	1
V_{CC} Trip Point (DS1233M–3)	V_{CCTP}	2.64	2.72	2.8	V	1
Output Capacitance	C_{OUT}			10	pF	
Internal Pull-Up Resistor	R_P	3.75	5	6.50	KΩ	

AC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC} = 1.2V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Reset Active Time	t_{RST}	200	350	500	ms	
V_{CC} Detect to $\overline{RST}$	t_{RPD}		2	10	µs	
V_{CC} Slew Rate ($V_{HTL} - V_{LTL}$)	t_F	300			µs	
V_{CC} Slew Rate ($V_{LTL} - V_{HTL}$)	t_R	0			ns	
V_{CC} detect to RST	t_{RPU}	200	350	500	ms	5

NOTES:

1. All voltages are referenced to ground.
2. Measured with $V_{CC} \geq 2.7V$.
3. A 1KΩ external resistor may be required in some applications for proper operation of the microprocessor reset control circuit.
4. Measured with outputs open.
5. t_R = 5 µs.

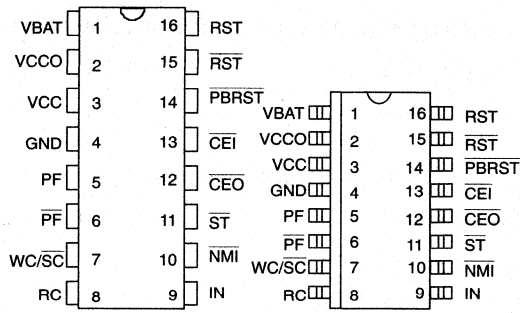
DALLAS SEMICONDUCTOR

DS1236
MicroManager Chip

FEATURES

- Holds microprocessor in check during power transients
- Halts and restarts an out-of-control microprocessor
- Monitors pushbutton for external override
- Warns microprocessor of an impending power failure
- Converts CMOS SRAM into nonvolatile memory
- Unconditionally write protects memory when power supply is out of tolerance
- Consumes less than 100 nA of battery current at 25°C
- Controls external power switch for high current applications
- Accurate 10% power supply monitoring
- Optional 5% power supply monitoring designated DS1236-5
- Provides orderly shutdown in nonvolatile microprocessor applications
- Supplies necessary control for low-power "stop mode" in battery operated hand-held applications
- Standard 16-pin DIP or space-saving 16-pin SOIC
- Optional industrial temperature range -40°C to +85°C

PIN ASSIGNMENT



16-Pin DIP (300 Mil.)
See Mech. Drawings Section

16-Pin SOIC (300 Mil.)
See Mech. Drawings Section

PIN DESCRIPTION

V_{BAT}	–	+3 Volt Battery Input
V_{CCO}	–	Switched SRAM Supply Output
V_{CC}	–	+5 Volt Power Supply Input
GND	–	Ground
PF	–	Power Fail (Active High)
$\overline{PF}$	–	Power Fail (Active Low)
WC/$\overline{SC}$	–	Wake-Up Control (Sleep)
RC	–	Reset Control
IN	–	Early Warning Input
$\overline{NMI}$	–	Non-Maskable Interrupt
$\overline{ST}$	–	Strobe Input
$\overline{CEO}$	–	Chip Enable Output
$\overline{CEI}$	–	Chip Enable Input
$\overline{PBRST}$	–	Pushbutton Reset Input
$\overline{RST}$	–	Reset Output (Active Low)
RST	–	Reset Output (Active High)

DESCRIPTION

The DS1236 MicroManager Chip provides all the necessary functions for power supply monitoring, reset control, and memory backup in microprocessor-based systems. A precise internal voltage reference and comparator circuit monitor power supply status. When an out-of-tolerance condition occurs, the microprocessor reset and power fail outputs are forced active, and static RAM control unconditionally write protects external memory. The DS1236 also provides early warning detection of a user-defined threshold by driving a non-maskable interrupt. External reset control is provided by a pushbutton reset input which is debounced and activates reset outputs. An internal watchdog timer can also force the reset outputs to the active state if the strobe input is not driven low prior to watchdog time-out. Reset control and wake-up/sleep control inputs also provide the necessary signals for orderly shutdown and start-up in battery backup and battery operated applications. A block diagram of the DS1236 is shown in Figure 1.

PIN DESCRIPTION

PIN NAME	DESCRIPTION
V_{BAT}	+3V battery input provides nonvolatile operation of control functions.
V_{CCO}	V_{CC} output for nonvolatile SRAM applications.
V_{CC}	+5V primary power input.
PF	Power fail indicator, active high, used for external power switching as shown in Figure 9.
$\overline{PF}$	Power fail indicator, active low.
WC/$\overline{SC}$	Wake-up and Sleep control. Invokes low-power mode.
RC	Reset control input. Determines reset output . Normally low for NMOS processors and high for battery-backed CMOS processors.
IN	Early warning power fail input. This voltage sense point can be tied (via resistor divider) to a user-selected voltage.
$\overline{NMI}$	Non-maskable interrupt. Used in conjunction with the IN pin to indicate an impending power failure.
$\overline{ST}$	Strobe input. A high-to-low transition will reset the watchdog timer, indicating that software is still in control.
$\overline{CEO}$	Chip enable output. Used with nonvolatile SRAM applications.
$\overline{CEI}$	Chip enable input.
$\overline{PBRST}$	Pushbutton reset input.
$\overline{RST}$	Active low reset output.
RST	Active high reset output.

3

PROCESSOR MODE

A distinction is often made between CMOS and NMOS processor systems. In a CMOS system, power consumption may be a concern, and nonvolatile operation is possible by battery backing both the SRAM and the CMOS processor. All resources would be maintained in the absence of V_{CC}. A power-down reset is not issued since the low-power mode of most CMOS processors (Stop) is terminated with a Reset. A pulsed interrupt ($\overline{NMI}$) is issued to allow the CMOS processor to invoke a sleep mode to save power. For this case, a power-on reset is desirable to wake up and initialize the processor. The CMOS mode is invoked by connecting RC to V_{CCO}.

An NMOS processor consumes more power, and consequently may not be battery backed. In this case, it is desirable to notify the processor of a power fail, then keep it in reset during the loss of V_{CC}. This avoids intermittent or aberrant operation. On power-up, the processor will continue to be reset until V_{CC} reaches an operational level to provide an orderly start. The NMOS mode is invoked by connecting RC to ground.

POWER MONITOR

The DS1236 employs a band gap voltage reference and a precision comparator to monitor the 5-volt supply (V_{CC}) in microprocessor-based systems. When an out-of-tolerance condition occurs, the RST and $\overline{RST}$ outputs are driven to the active state. Th e V_{CC} trip point (V_{CCTP}) is set for 10% operation so that the RST and $\overline{RST}$ outputs will become active as V_{CC} falls below 4.5 volts (4.37 typical). The V_{CCTP} for the 5% operation option (DS1236-5) is set for 4.75 volts (4.62 typical). The RST and $\overline{RST}$ signals are excellent for microprocessor reset control, as processing is stopped at the last possible moment of in-tolerance V_{CC}. On power-up, the RST and $\overline{RST}$ signals are held active for a minimum of 25 ms (100 ms typical) after V_{CCTP} is reached to allow the power supply and microprocessor to stabilize. Note: The operation described above is obtained with the reset control pin (RC) connected to GND (NMOS mode). Please review the reset control section for more information.

WATCHDOG TIMER

The DS1236 provides a watchdog timer function which forces the RST and $\overline{RST}$ signals to the active state when the strobe input ($\overline{ST}$) is not stimulated for a predetermined time period. This time period is 400 ms typically with a maximum time-out of 600 ms. The watchdog time-out period begins as soon as RST and $\overline{RST}$ are inactive. If a high-to-low transition occurs at the $\overline{ST}$ input prior to time-out, the watchdog timer is reset and begins to time out again. The $\overline{ST}$ input timing is shown in Figure 2. To guarantee the watchdog timer does not time out, a high-to-low transition on $\overline{ST}$ must occur at or less than 100 ms (minimum time-out) from a reset. If the watchdog timer is allowed to time out, the RST and $\overline{RST}$ outputs are driven to the active state for 25 ms minimum. The $\overline{ST}$ input can be derived from microprocessor address, data, and/or control signals. Under normal operating conditions, these signals would routinely reset the watchdog timer prior to time-out. If the watchdog timer is not required, two methods have been provided to disable it.

Permanently grounding the IN pin in the CMOS mode (RC=1) will disable the watchdog. In normal operation with RC=1, the watchdog is disabled as soon as the IN pin is below V_{TP}. With IN grounded, an $\overline{NMI}$ output will occur only at power-up, or when the $\overline{ST}$ pin is strobed. As shown in the Figure 3, a falling edge on $\overline{ST}$ will generate an $\overline{NMI}$ when IN is below V_{TP}. This allows the processor to verify that power is between V_{TP} and V_{CCTP}, as an $\overline{NMI}$ will be returned immediately after the $\overline{ST}$ strobe. The watchdog timer is not affected by the IN pin when in NMOS mode (RC=0).

If the $\overline{NMI}$ signal is required to monitor supply voltages, the watchdog may also be disabled by leaving the $\overline{ST}$ input open. Independent of the state of the RC pin, the watchdog is also disabled as soon as V_{CC} falls to V_{CCTP}.

PUSHBUTTON RESET

An input pin is provided on the DS1236 for direct connection to a pushbutton. The pushbutton reset input requires an active low signal. Internally, this input is pulled high by a 10K resistor whenever V_{CC} is greater than V_{BAT}. The $\overline{PBRST}$ pin is also debounced and timed such that the RST and $\overline{RST}$ outputs are driven to the active state for 25 ms minimum. This 25 ms delay begins as the pushbutton is released from a low level. A typical example of the power monitor, watchdog timer, and pushbutton reset connections are shown in Figure 4. The $\overline{PBRST}$ input is disabled whenever the IN pin voltage level is less than V_{TP} and the reset control (RC) is tied high (CMOS mode). The $\overline{PBRST}$ input is also disabled whenever V_{CC} is below V_{BAT}. Timing of the $\overline{PBRST}$-generated RST is illustrated in Figure 5.

NON-MASKABLE INTERRUPT

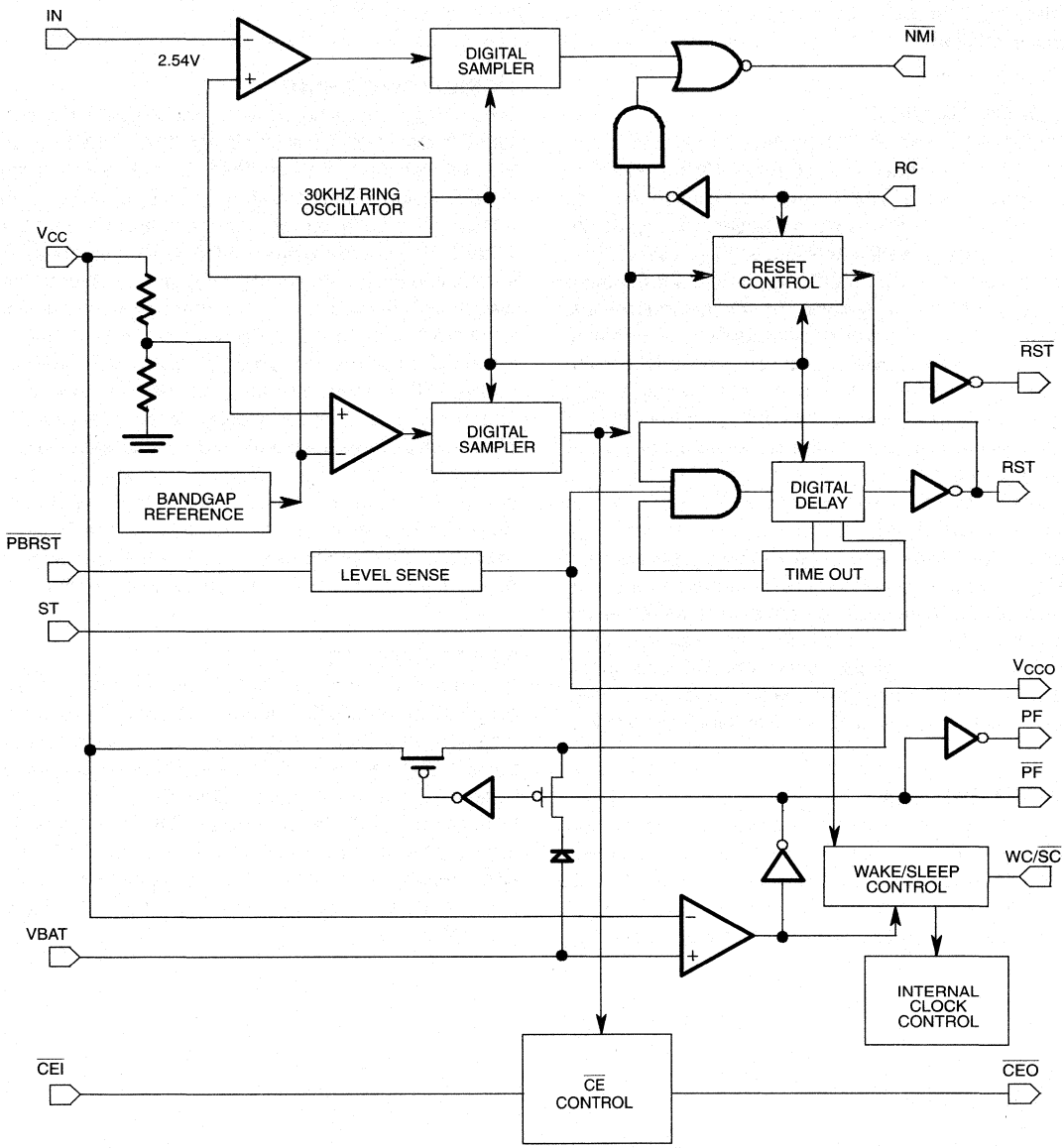
The DS1236 generates a non-maskable interrupt $\overline{NMI}$ for early warning of power failure to a microprocessor. A precision comparator monitors the voltage level at the IN pin relative to a reference generated by the internal band gap. The IN pin is a high impedance input allowing for a user-defined sense point. An external resistor voltage divider network (Figure 6) is used to interface with high voltage signals. This sense point may be derived from the regulated 5-volt supply or from a higher DC voltage level closer to the main system power input. Since the IN trip point V_{TP} is 2.54 volts, the proper values for R1 and R2 can be determined by the equation as shown in Figure 6. Proper operation of the DS1236 requires that the voltage at the IN pin be limited to V_{IN}. Therefore, the maximum allowable voltage at the supply being monitored (V_{MAX}) can also be derived as shown in Figure 6. A simple approach to solving this equation is to select a value for R2 high enough to keep power consumption low, and solve for R1. The flexibility of the IN input pin allows for detection of power loss at the earliest point in a power supply system, maximizing the amount of time for microprocessor shut-down between $\overline{NMI}$ and RST or $\overline{RST}$.

When the supply being monitored decays to the voltage sense point, the DS1236 pulses the $\overline{NMI}$ output to the active state for a minimum of 200 µs. The $\overline{NMI}$ power fail detection circuitry also has built-in time domain hysteresis. That is, the monitored supply is sampled periodically at a rate determined by an internal ring oscillator running at approximately 30 KHz (33 µs/cycle). Three consecutive samplings of out-of-tolerance supply (below V_{SENSE}) must occur at the IN pin to activate $\overline{NMI}$. Therefore, the supply must be below the voltage sense point for approximately 100 µs or the comparator will reset. In this way, power supply noise is removed from the monitoring function, preventing false trips. During a power-up , any IN pin levels below V_{TP} are disabled from reaching the $\overline{NMI}$ pin until V_{CC} rises to V_{CCTP}. As a result, any potential $\overline{NMI}$ pulse will not be initiated until V_{CC} reaches V_{CCTP}.

Removal of an active low level on the $\overline{NMI}$ pin is controlled by either an internal time-out (when IN pin is less than V_{TP}) or by the subsequent rise of the IN pin above

V_{TP}. The initiation and removal of the $\overline{NMI}$ signal during power-up results in an $\overline{NMI}$ pulse of from 0 µs minimum to 500 µs maximum, depending on the relative voltage relationship between V_{CC} and the IN pin voltage. As an example, when the IN pin is tied to ground during power-up, the internal time-out will result in a pulse of 200 µs minimum to 500 µs maximum. In contrast, if the IN pin is tied to V_{CCO} during power-up, $\overline{NMI}$ will not produce a pulse on power-up. Note that a fast slewing power supply may cause the $\overline{NMI}$ to be virtually non-existent on power-up. This is of no consequence, however, since a $\overline{RST}$ will be active.

DS1236 FUNCTIONAL BLOCK DIAGRAM Figure 1



If the IN pin is connected to V_{CCO}, the $\overline{NMI}$ output will pulse low as V_{CC} decays to V_{CCTP} in the NMOS mode (RC=0). In the CMOS mode (RC=V_{CCO}) the power-down of V_{CC} out-of-tolerance at V_{CCTP} will not produce a pulse on the $\overline{NMI}$ pin. Given that any $\overline{NMI}$ pulse has been completed by the time V_{CC} decays to V_{CCTP}, the $\overline{NMI}$ pin will remain high. The $\overline{NMI}$ voltage will follow V_{CC} down until V_{CC} decays to V_{BAT}. Once V_{CC} decays to V_{BAT}, the $\overline{NMI}$ pin will either remain at V_{OHL} or enter tri-state mode as determined by the RC pin (see "Reset Control" section).

MEMORY BACKUP

The DS1236 provides all of the necessary functions required to battery back a static RAM. First, a switch is provided to direct SRAM power from the incoming 5 volt supply (V_{CC}) or from an external battery (V_{BAT}), whichever is greater. This switched supply (V_{CCO}) can also be used to battery back a CMOS microprocessor. For more information about nonvolatile processor applications, review the "Reset Control" and "Wake Control" sections. Second, the same power fail detection described in the power monitor section is used to hold the chip enable output ($\overline{CEO}$) to within 0.3 volts of V_{CC} or to within 0.7 volts of V_{BAT}. This write protection mechanism occurs as V_{CC} falls below V_{CCTP} as specified. If $\overline{CEI}$ is low at the time power fail detection occurs, $\overline{CEO}$ is held in its present state until $\overline{CEI}$ is returned high, or the period t_{CE} expires. This delay of write protection until the current memory cycle is completed prevents the corruption of data. If $\overline{CEO}$ is in an inactive state at the time of V_{CC} fail detection, $\overline{CEO}$ will be unconditionally disabled within t_{CF}. During nominal supply conditions $\overline{CEO}$ will follow $\overline{CEI}$ with a maximum propagation delay of 20 ns. Figure 7 shows a typical nonvolatile SRAM application.

FRESHNESS SEAL

In order to conserve battery capacity during storage and/or shipment of an end system, the DS1236 provides a freshness seal to electrically disconnect the battery. Figure 8 depicts the three pulses below ground on the IN pin required to invoke the freshness seal. The freshness seal will be disconnected and normal operation will begin when V_{CC} is cycled and reapplied to a level above V_{BAT}.

To prevent negative pulses associated with noise from setting the freshness mode in system applications, a series diode and resistor can be used to shunt noise to ground. During manufacturing, the freshness seal can still be set by holding TP2 at -3 volts while applying the 0 to -3 volt clock to TP1.

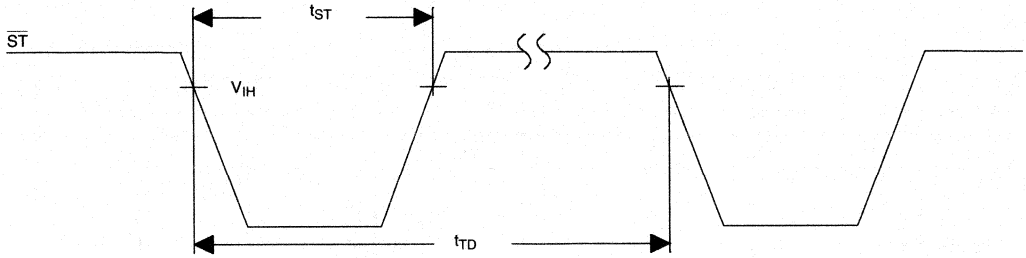
POWER SWITCHING

When larger operating currents are required in a battery-backed system, the 5-volt supply and battery supply switches internal to the DS1236 may not be large enough to support the required load through V_{CCO} with a reasonable voltage drop. For these applications, the PF and $\overline{PF}$ outputs are provided to gate external power switching devices. As shown in Figure 9, power to the load is switched from V_{CC} to battery on power-down, and from battery to V_{CC} on power- up. The DS1336 is designed to use the $\overline{PF}$ output to switch between V_{BAT} and V_{CC}. It provides better leakage and switchover performance than currently available discrete components. The transition threshold for PF and $\overline{PF}$ is set to the external battery voltage V_{BAT}, allowing a smooth transition between sources. The load applied to the PF pin from the external switch will be supplied by the battery. Therefore, if a discrete switch is used, this load should be taken into consideration when sizing the battery.

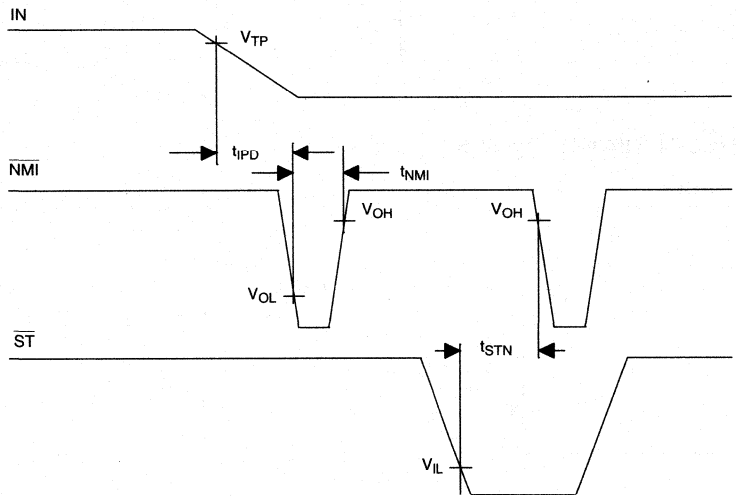
RESET CONTROL

As mentioned above, the DS1236 supports two modes of operation. The CMOS mode is used when the system incorporates a CMOS microprocessor which is battery backed. The NMOS mode is used when a non-battery backed processor is incorporated. The mode is selected by the RC (Reset Control) pin. The level of this pin distinguishes timing and level control on RST, $\overline{RST}$, and $\overline{NMI}$ outputs for volatile processor operation versus nonvolatile battery backup or battery-operated processor applications.

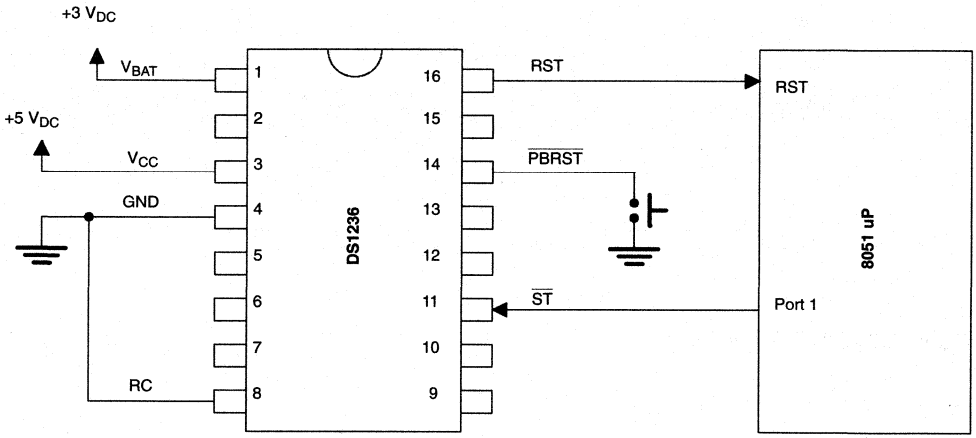
ST/INPUT TIMING Figure 2



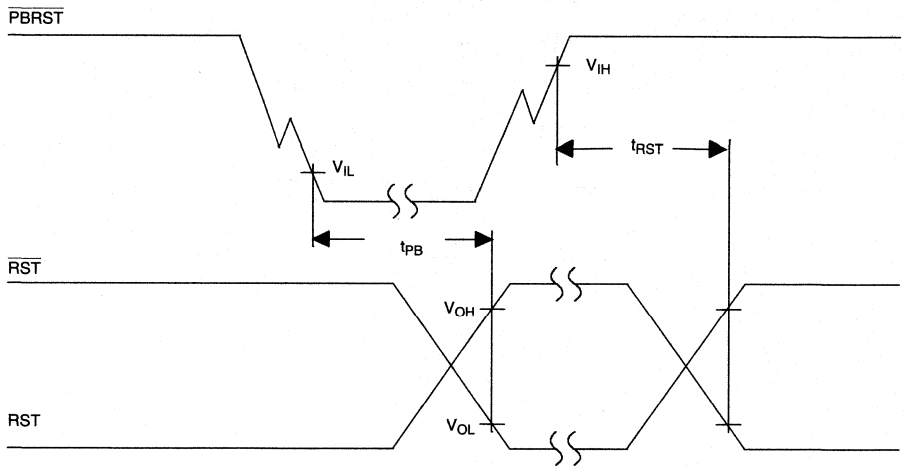
NMI/FROM ST/INPUT Figure 3



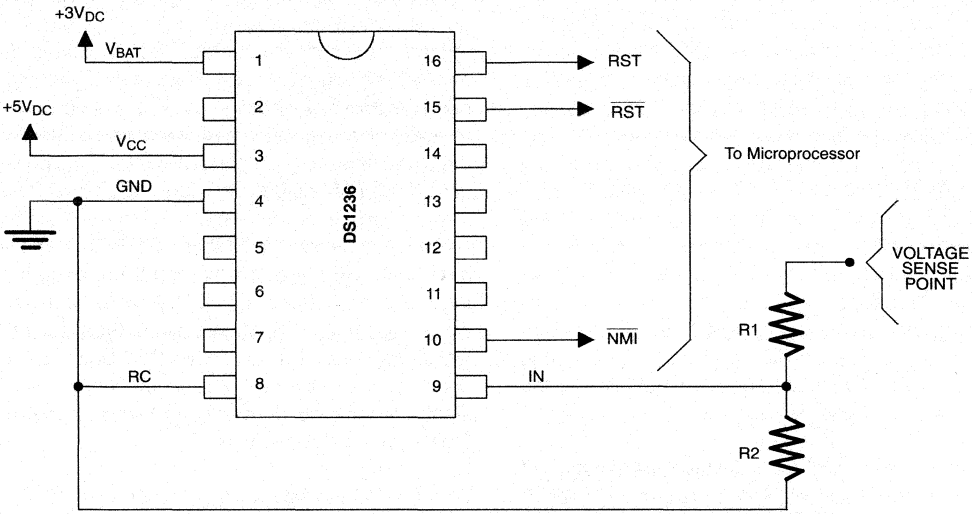
POWER MONITOR, WATCHDOG Figure 4



PUSH BUTTON RESET TIMING Figure 5



NON-MASKABLE INTERRUPT Figure 6



EXAMPLE 1: 5 VOLT SUPPLY, R2 = 10K OHM, V_{SENSE} = 4.80 VOLTS

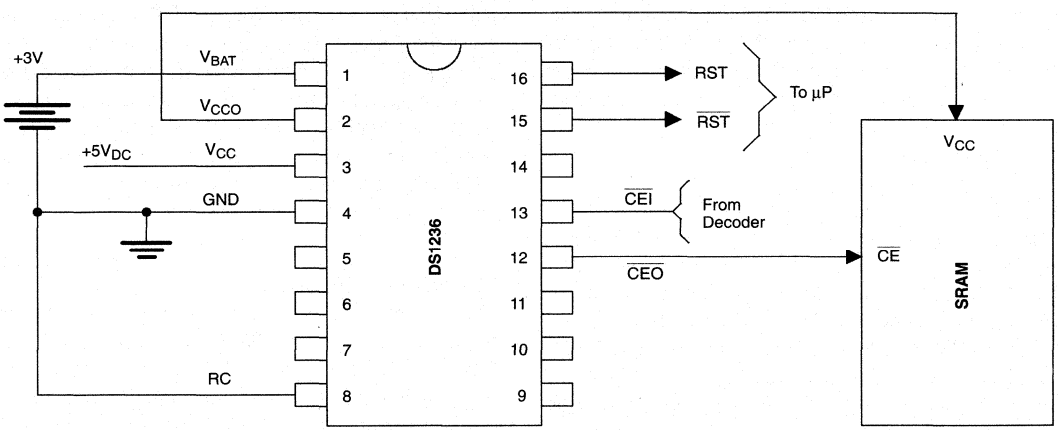
$$\therefore 4.80 = \frac{R1 + 10K}{10K} \times 2.54 \qquad R1 = 8.9K \text{ OHM}$$

EXAMPLE 2: 12 VOLT SUPPLY, R2 = 10K OHM, V_{SENSE} = 9.00 VOLTS

$$\therefore 9.00 = \frac{R1 + 10K}{10K} \times 2.54 \qquad R1 = 25.4K \text{ OHM}$$

$$V_{MAX} = \frac{9.00}{2.54} \times 5.00 = 17.7 \text{ VOLTS}$$

NONVOLATILE SRAM Figure 7



When the RC pin is tied to ground, the DS1236 is designed to interface with NMOS processors which do not have the microamp currents required during a battery backed mode. Grounding the RC pin does, however, continue to support nonvolatile backup of system SRAM memory. Nonvolatile systems incorporating NMOS processors generally require that only the SRAM memory and/or timekeeping functions be battery backed. When the processor is not battery backed (RC = 0), all signals connected from the processor to the DS1236 are disconnected from the backup battery supply, or grounded when system V_{CC} decays below V_{BAT}. In the NMOS processor system, the principal emphasis is placed on giving early warnings with $\overline{NMI}$, then providing a continuously active RST and $\overline{RST}$ signal during power-down while isolating the backup battery from the processor during a loss of V_{CC}.

During power-down, $\overline{NMI}$ will pulse low for a minimum of 200 µs, and then return high. If RC is tied low (NMOS mode), the voltage on $\overline{NMI}$ will follow V_{CC} until V_{CC} supply decays to V_{BAT}, at which point $\overline{NMI}$ will enter tri-state (see timing diagram). Also, upon V_{CC} out-of-tolerance at V_{CCTP}, the RST and $\overline{RST}$ outputs are driven active and RST will follow V_{CC} as the supply decays. On power-up, RST follows V_{CC} up, $\overline{RST}$ is held low, and both remain active for t_{RST} after valid V_{CC}. During a power-up from a V_{CC} voltage below V_{BAT}, any detected IN pin levels below V_{TP} are disabled from reaching the $\overline{NMI}$ pin until V_{CC} rises to V_{CCTP}. As a result, any potential $\overline{NMI}$ pulse will not be initiated until V_{CC} reaches V_{CCTP}. Removal of an active low level on the $\overline{NMI}$ pin is controlled by either an internal time-out (when the IN pin is less than V_{TP}), or by the subsequent rise of the IN pin above V_{TP}. The initiation and removal of the $\overline{NMI}$ signal results in an $\overline{NMI}$ pulse of 0 µs minimum to 500 µs maximum during power-up, depending on the relative voltage relationship between V_{CC} and the IN pin. As an example, when the IN pin is tied to ground, the internal time-out will result in a pulse of 200 µs minimum to 500 µs maximum. In contrast, if the IN pin is tied to V_{CCO}, $\overline{NMI}$ will not produce a pulse on power-up.

Connecting the RC pin to a high (V_{CCO}) invokes CMOS mode and provides nonvolatile support to both the system SRAM as well as a low power CMOS processor. When using CMOS microprocessors, it is possible to place the microprocessor into a very low- power mode termed the "stop" or "halt" mode. In this state the CMOS processor requires only microamp currents and is fully capable of being battery backed. This mode generally allows the CMOS microprocessor to maintain the contents of internal RAM as well as state control of I/O ports during battery backup. The processor can subsequently be restarted by any of several different signals. To maintain this low-power state, the DS1236 issues no $\overline{NMI}$ and/or reset signals to the processor until it is time to bring the processor back into full operation. To support the low-power processor battery backed mode (RC = 1), the DS1236 provides a pulsed $\overline{NMI}$ for early power failure warning. Waiting to initiate a Stop mode until after the $\overline{NMI}$ pin has returned high will guarantee the processor that no other active $\overline{NMI}$ or RST/$\overline{RST}$ will be issued by the DS1236 until one of two conditions occurs: 1) Voltage on the pin rises above V_{TP}, which activates the watchdog, or 2) V_{CC} cycles below then above V_{BAT}, which also results in an active RST and $\overline{RST}$. If V_{CC} does not fall below V_{CCTP}, the processor will be restarted by the reset derived from the watchdog timer as the IN pin rises above V_{TP}.

With the RC pin tied to V_{CCO}, RST and $\overline{RST}$ are not forced active as V_{CC} collapses to V_{CCTP}. The $\overline{RST}$ is held at a high level via the external battery as V_{CC} falls below battery potential. This mode of operation is intended for applications in which the processor is made nonvolatile with an external source, and allows the processor to power down into a Stop mode as signaled from $\overline{NMI}$ at an earlier voltage level. The $\overline{NMI}$ output pin will pulse low for t_{NMI} following a low voltage detect at the IN pin of V_{TP}. Following t_{NMI}, however, $\overline{NMI}$ will also be held at a high level (V_{BAT}) by the battery as V_{CC} decays below V_{BAT}. On power-up, RST and $\overline{RST}$ are held inactive until V_{CC} reaches V_{BAT}, then RST and $\overline{RST}$ are driven active for t_{RST}. If the IN pin falls below V_{TP} during an active reset, the reset outputs will be forced inactive by the $\overline{NMI}$ output. In addition, as long as the IN pin is less than V_{TP}, stimulation of the ST pin will result in additional $\overline{NMI}$ pulses. In this way, the $\overline{ST}$ pin can be used to allow the CMOS processor to determine if the supply voltage, as monitored by the IN pin, is above or below a selected operating value. This is illustrated in Figure 3. As discussed above, the RC pin determines the timing relationships and levels of several signals. The following section describes the power-up and power-down timing diagrams in more detail.

TIMING DIAGRAMS

This section provides a description of the timing diagrams shown in Figure 10, Figure 11, Figure 12, and Figure 13. These diagrams show the relative timing and levels in both the NMOS and the CMOS mode for power-up and down. Figure 10 illustrates the relationship for

power-down in CMOS mode. As V_{CC} falls, the IN pin voltage drops below V_{TP}. As a result, the processor is notified of an impending power failure via an active $\overline{NMI}$, which allows it to enter a sleep mode. As the power falls further, V_{CC} crosses V_{CCTP}, the power monitor trip point. Since the DS1236 is in CMOS mode, no reset is generated. The $\overline{RST}$ voltage will follow V_{CC} down, but will fall no further than V_{BAT}. At this time, $\overline{CEO}$ is brought high to write protect the RAM. When the V_{CC} reaches V_{BAT}, a power fail is issued via the PF and $\overline{PF}$ pins.

Figure 11 illustrates operation of the power-down sequence in NMOS mode. Once again, as power falls, an $\overline{NMI}$ is issued. This gives the processor time to save critical data in nonvolatile SRAM. When V_{CC} reaches V_{CCTP}, an active RST and $\overline{RST}$ are given. The RST voltage will follow V_{CC} as it falls. $\overline{CEO}$, PF, and $\overline{PF}$ will operate in a similar manner to CMOS mode. Notice that the $\overline{NMI}$ will tri-state to prevent a loss of battery power.

Figure 12 shows the power-up sequence for the NMOS mode. As V_{CC} slews above V_{BAT}, the PF and $\overline{PF}$ pins are deactivated. An active reset occurs as well as an $\overline{NMI}$. Although the $\overline{NMI}$ may be short due to slew rates, reset will be maintained for the standard t_{RST} time-out period. At a later time, if the IN pin falls below V_{TP}, a new $\overline{NMI}$ will occur. If the processor does not issue a $\overline{ST}$, a watchdog reset will also occur. The second $\overline{NMI}$ and RST are provided to illustrate these possibilities.

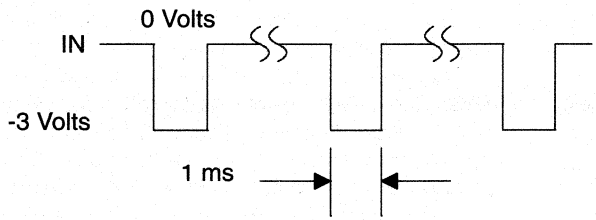
Figure 13 illustrates the power-up timing for CMOS mode. The principal difference is that the DS1236 issues a reset immediately in the NMOS mode. In CMOS mode, a reset is issued when IN rises above V_{TP}. Depending on the processor type, the $\overline{NMI}$ may terminate the Stop mode in the processor.

WAKE CONTROL/SLEEP CONTROL

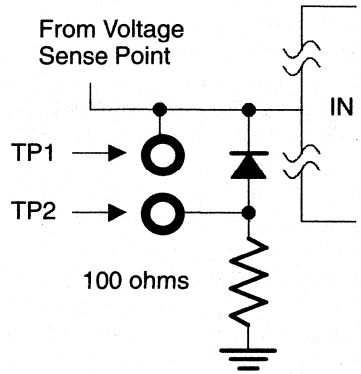
The Wake/Sleep Control input (WC/$\overline{SC}$) allows the processor to disable all comparators on the DS1236 before entering the Stop mode. This feature allows the DS1236, processor, and static RAM to maintain nonvolatility in the lowest power mode possible. The processor may invoke the sleep mode in battery-operated applications to conserve battery capacity when an absence of activity is detected. The operation of this signal is shown in Figure 14. The DS1236 may subsequently be restarted by a high-to-low transition on the $\overline{PBRST}$ input through human interface via a keyboard, touchpad, etc. The processor will then be restarted as the watchdog times out and drives RST and $\overline{RST}$ active. The DS1236 can also be started up by forcing the WC/$\overline{SC}$ pin high from an external source. Also, if the DS1236 is placed in a sleep mode by the processor and system power is lost, the DS1236 will wake up the next time V_{CC} rises above V_{BAT}. These possibilities are illustrated in Figure 15.

When the sleep mode is invoked during normal power-valid conditions, all operation on the DS1236 is disabled, thus leaving the $\overline{NMI}$, RST, and $\overline{RST}$ outputs disabled as well as the $\overline{ST}$ and IN inputs. However, a loss of power during a sleep mode will result in an active RST and $\overline{RST}$ when the RC pin is grounded (NMOS mode). If the RC pin is tied high, the RST and $\overline{RST}$ pins will remain inactive during power-down in a sleep mode. Removal of the sleep mode by the $\overline{PBRST}$ input is not affected by the IN pin threshold at V_{TP} when the RC pin is tied high (CMOS mode). Subsequent power-up of the V_{CC} supply with the RC pin tied high will activate the RST and $\overline{RST}$ outputs as the main supply rises above V_{BAT}. A high-to-low transition on the WC/$\overline{SC}$ pin must follow a high-to-low transition on the ST pin by t_{WC} to invoke a Sleep mode for the DS1236.

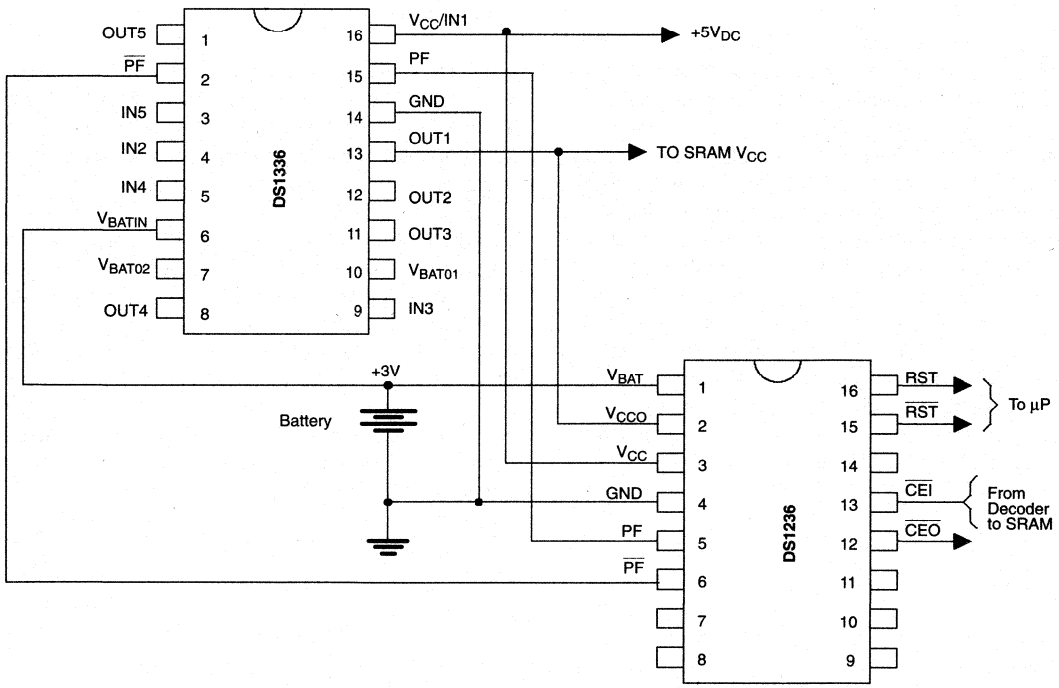
FRESHNESS SEAL Figure 8



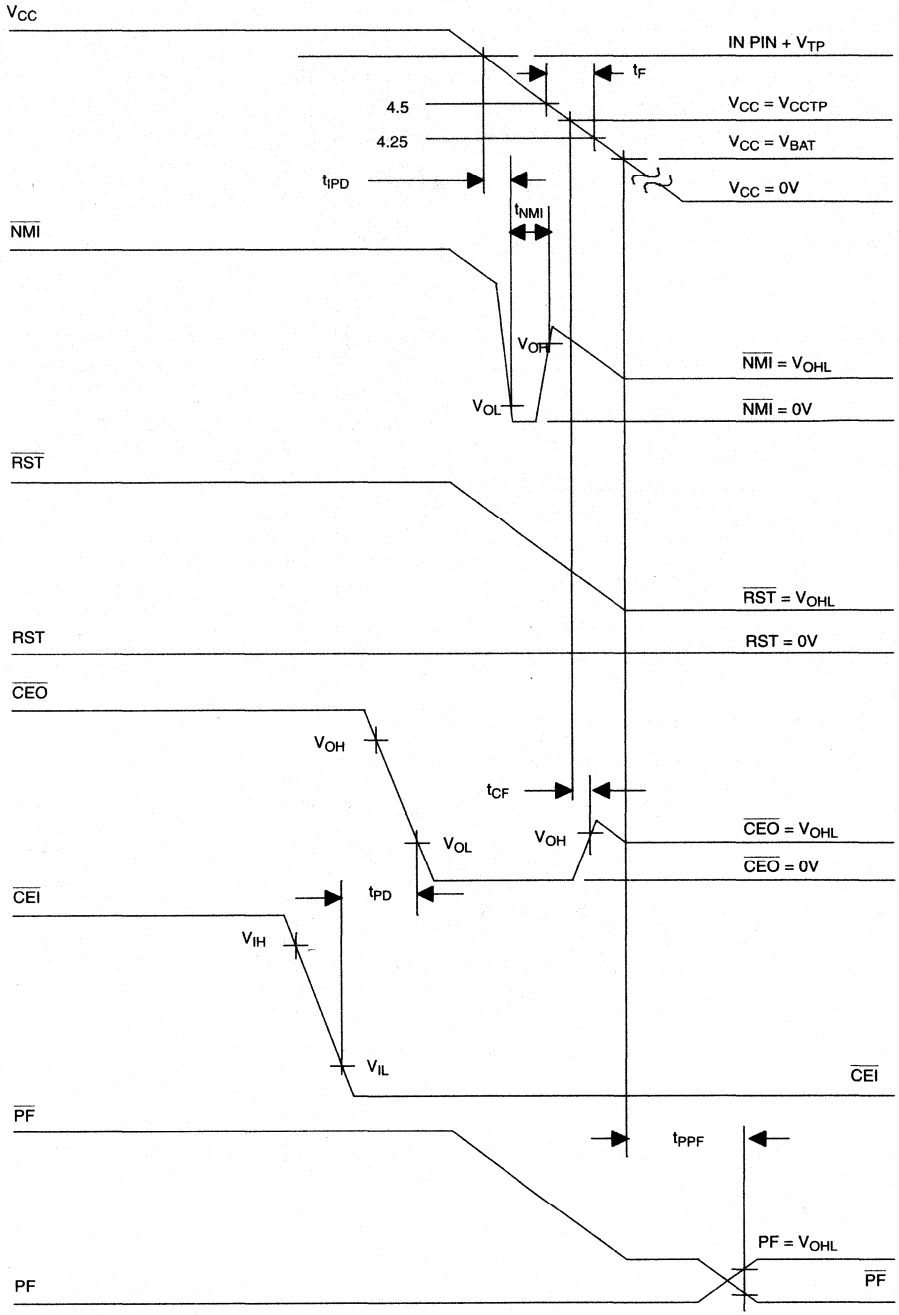
Note: This series of pulses must be applied during normal +5 volt operation.



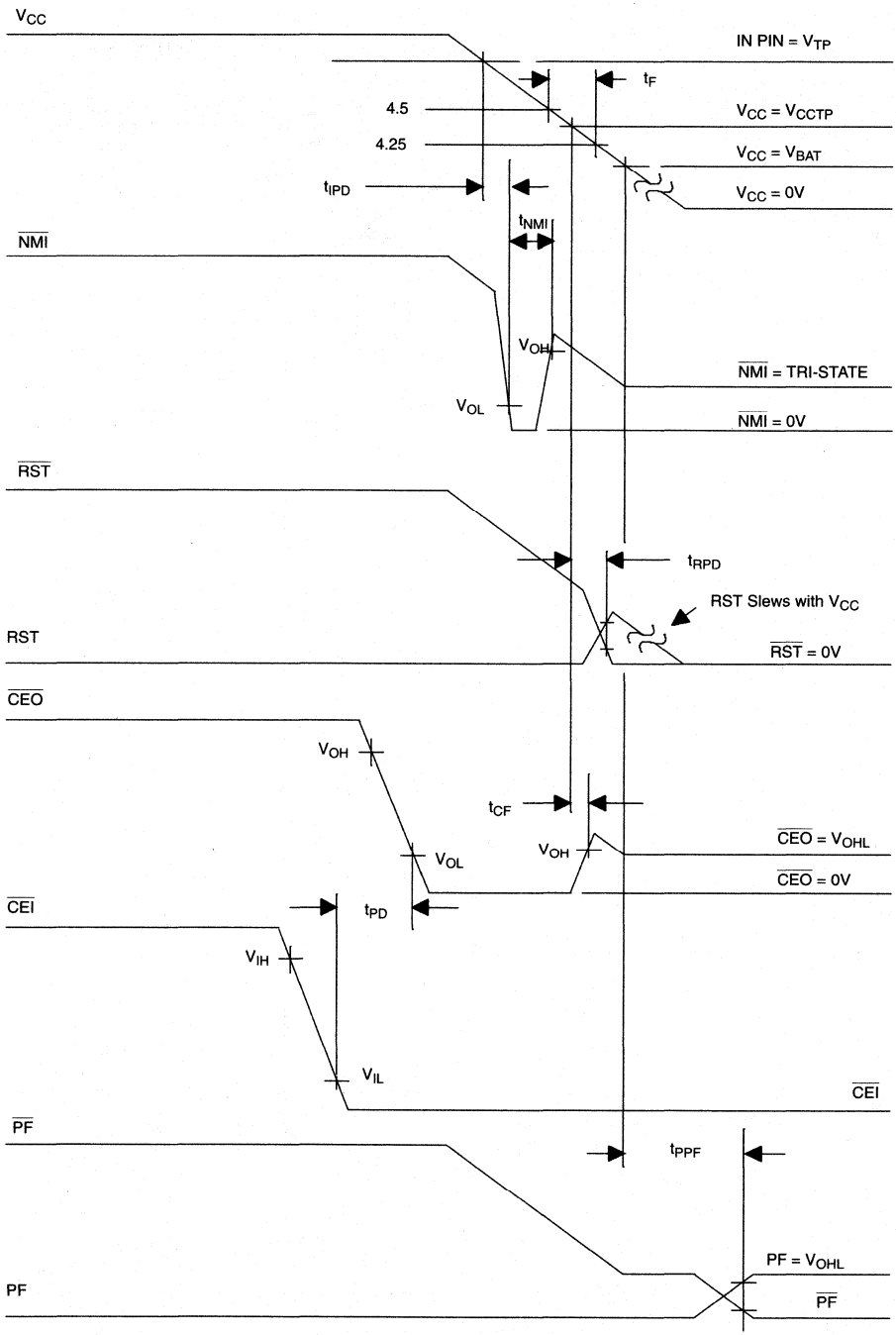
POWER SWITCHING Figure 9



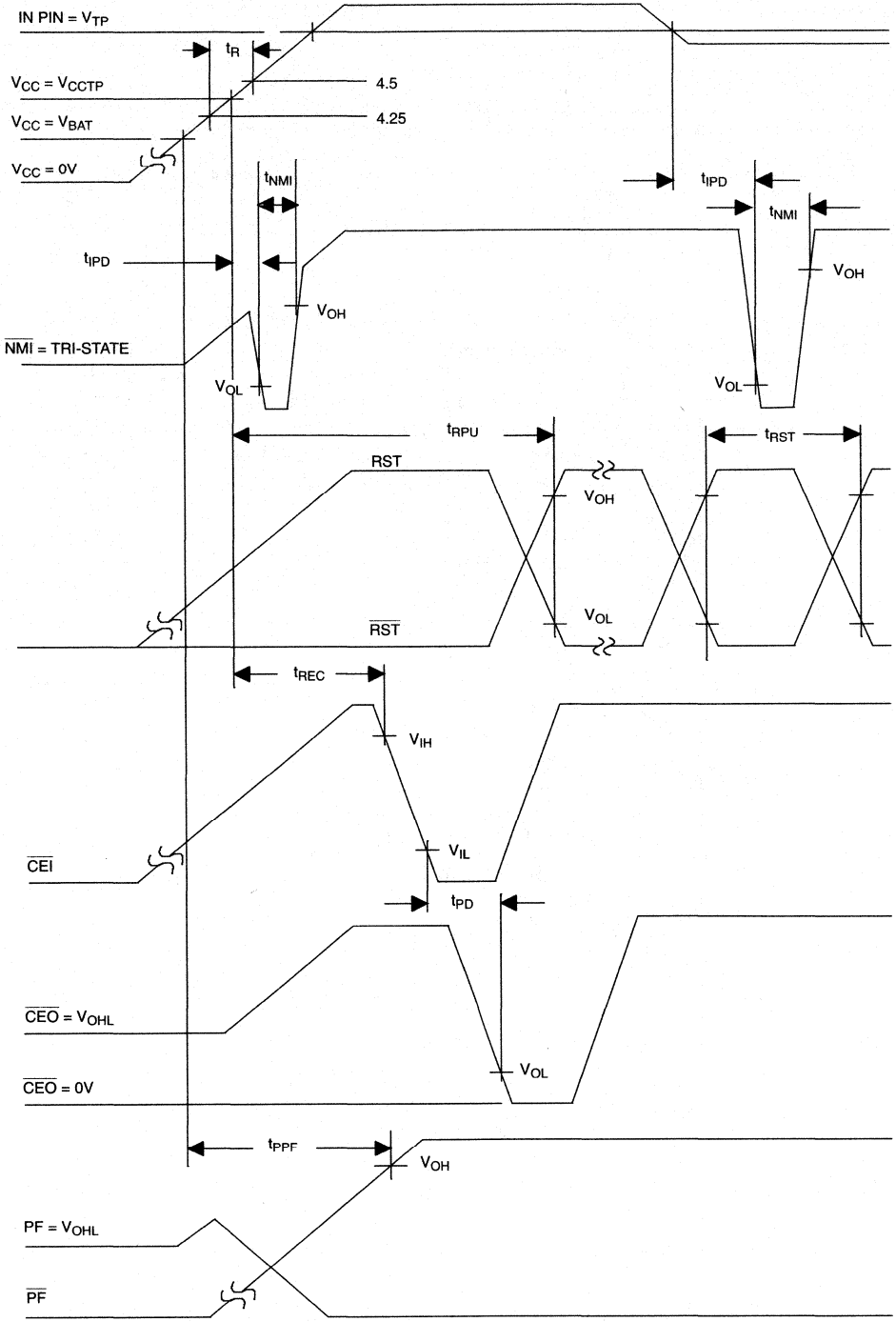
CMOS MODE POWER-DOWN (RC = V_{CCO}) Figure 10



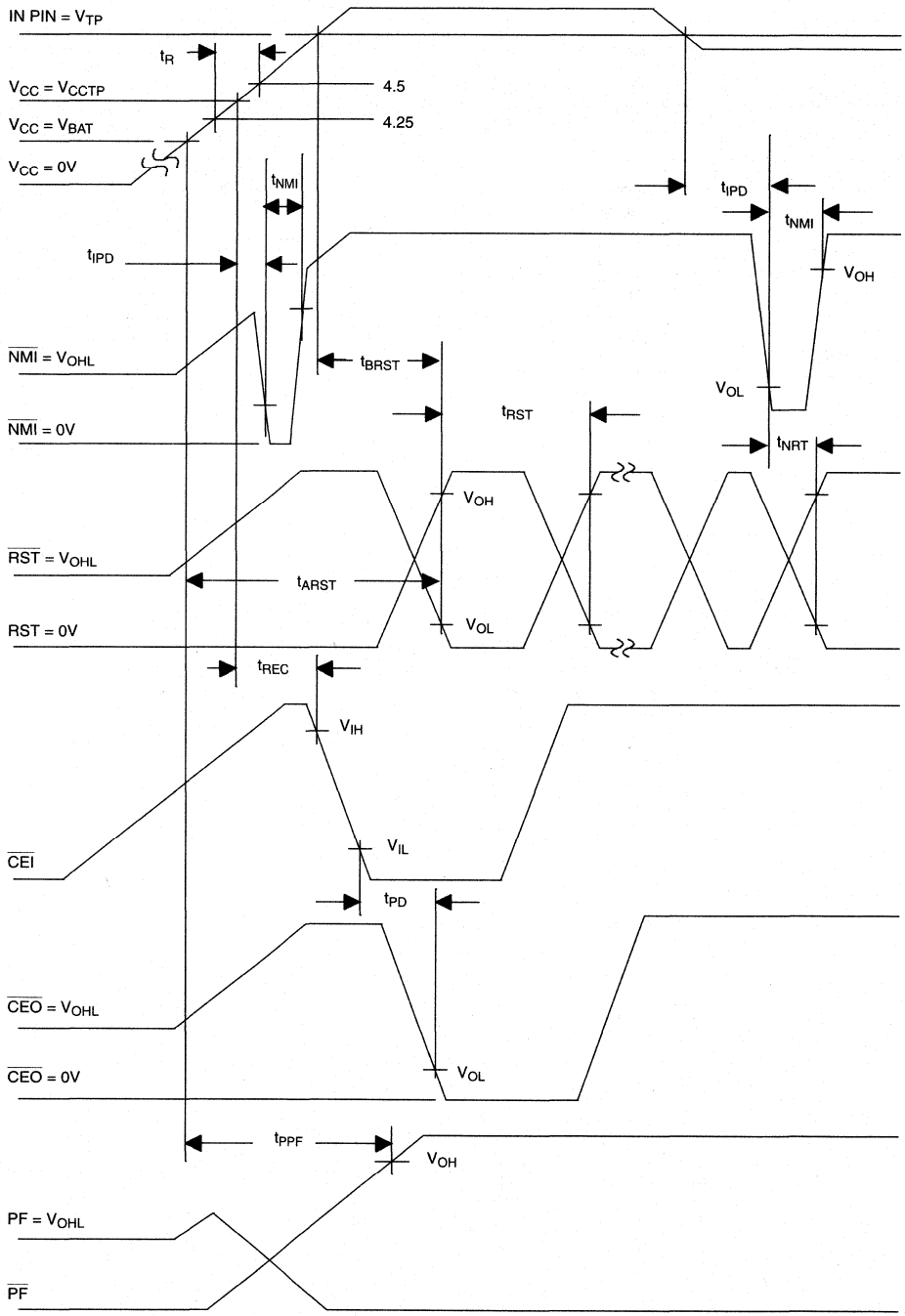
NMOS MODE POWER-DOWN (RC = GND) Figure 11



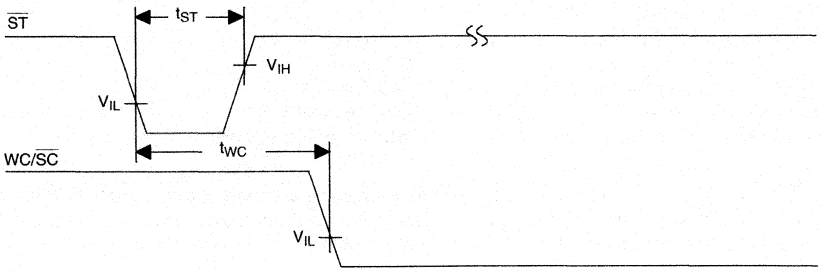
NMOS MODE POWER-UP (RC = GND) Figure 12



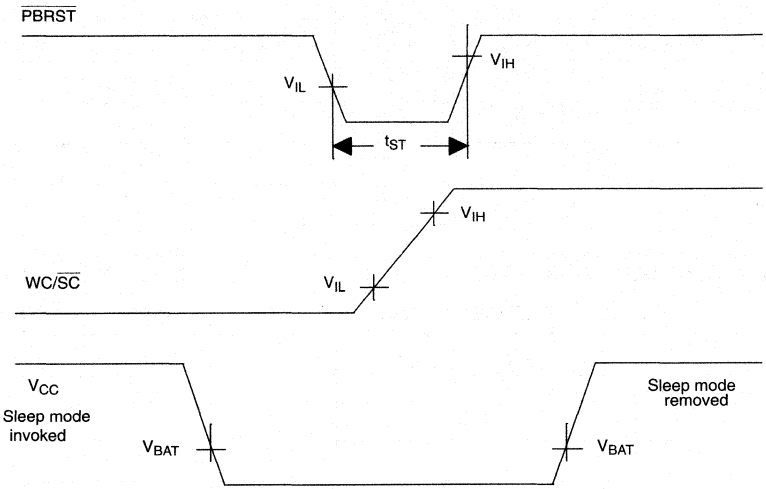
CMOS MODE POWER-UP (RC = V_{CCO}) Figure 13



WAKE/SLEEP CONTROL Figure 14



OPTIONS FOR INVOKING WAKEUP Figure 15



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	-0.5V to +7.0V
Voltage on I/O Relative to Ground	–0.5V to V_{CC} + 0.5V
Voltage on IN Pin Relative to Ground	–3.5V to V_{CC} + 0.5V
Operating Temperature	0°C to 70°C
Operating Temperature (Industrial Version)	–40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Supply Voltage (5% Option)	V_{CC}	4.75	5.0	5.5	V	1
Input High Level	V_{IH}	2.0		V_{CC}+0.3	V	1
Input Low Level	V_{IL}	-0.3		+0.8	V	1
IN Input Pin	V_{IN}	-0.3		V_{CC} +0.3	V	1
Battery Input	V_{BAT}	2.7		4.0	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.5 V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}			4	mA	2
Sleep Supply Current in Sleep mode	I_{CC}			20	µA	
Battery Current	I_{BAT}			0.1	µA	2
Supply Output Current (V_{CCO}=V_{CC} - 0.3V)	I_{CC01}			100	mA	3
Supply Output Current in Data Retention (V_{CC} < V_{BAT})	I_{CC02}			1	mA	4
Supply Output Voltage	V_{CCO}		V_{CC}–0.3		V	1
Battery Backup Voltage	V_{CCO}		V_{BAT}–0.7		V	1,6
Low Level @ RST	V_{OL}			0.4	V	1
Output Voltage @ –500 µA	V_{OH}	V_{CC}–0.5V	V_{CC}–0.1V		V	1
$\overline{CEO}$ and PF Output	V_{OHL}		V_{BAT}–0.7		V	1,6
$\overline{PBRST}$ Pull Up Resist	R_{PBRST}	10K			Ohms	
Input Leakage Current	I_{LI}	-1.0		+1.0	µA	18
Output Leakage	I_{LO}	-1.0		+1.0	µA	18
Output Current @0.4V	I_{OL}			4.0	mA	12

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Current @2.4V	I_{OH}	-1.0			mA	13
Power Sup. Trip Point	V_{CCTP}	4.25	4.37	4.50	V	1
Power Supply Trip (5% Option)	V_{CCTP}	4.50	4.62	4.75	V	1
IN Input Pin Current	I_{CCIN}	-1.0		+1.0	µA	
IN Input Trip Point	V_{TP}	2.5	2.54	2.6	V	1

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} Fail Detect to RST, $\overline{RST}$	t_{RPD}	40	100	175	µs	
V_{TP} to $\overline{NMI}$	t_{IPD}	40	100	175	µs	
RESET Active Time	t_{RST}	25	100	150	ms	
$\overline{NMI}$ Pulse Width	t_{NMI}	200	300	500	µs	14
$\overline{ST}$ Pulse Width	t_{ST}	20			ns	19
$\overline{PBRST}$ @ V_{IL}	t_{PB}	30			ms	
V_{CC} Slew Rate 4.75 to 4.25	t_F	300			µs	
Chip Enable Propagation Delay	t_{PD}			20	ns	
V_{CC} Fail to Chip Enable High	t_{CF}	7	12	44	µs	17
V_{CC} Valid to RST, $\overline{RST}$ (RC=1)	t_{FPU}			100	ns	
V_{CC} Valid to RST & $\overline{RST}$	t_{RPU}	25	100	150	ms	5
V_{CC} Slew to 4.24 to V_{BAT}	t_{FB1}	10			µs	7
V_{CC} Slew 4.25 to 4.75 V_{BAT}	t_{FB2}	100			µs	8
Chip Enable Output Recovery Time	t_{REC}	.1			µs	9
V_{CC} Slew 4.25 to 4.75	t_R	0			µs	
Chip Enable Pulse Width	t_{CE}			5	s	10
Watchdog Time Delay	t_{TD}	100	400	600	ms	
$\overline{ST}$ to WC/$\overline{SC}$	t_{WC}	0.1		50	µs	
V_{BAT} Detect to PF, $\overline{PF}$	t_{PPF}			2	µs	7
$\overline{ST}$ to $\overline{NMI}$	t_{STN}			30	ns	11
$\overline{NMI}$ to RST & $\overline{RST}$	t_{NRT}			30	ns	
V_{BAT} Detect to RST & $\overline{RST}$	t_{ARST}			200	µs	15
V_{CC} Valid to RST, $\overline{RST}$	t_{BRST}	30	100	150	µs	16

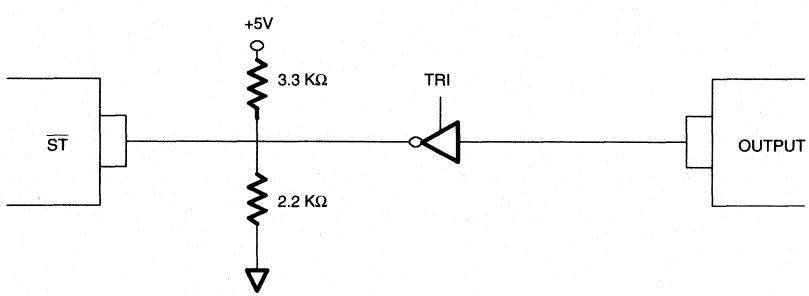
CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

NOTES:

1. All voltages referenced to ground. A 0.1 µF capacitor is recommended between V_{CC} and GND.
2. Measured with V_{CCO}, $\overline{CEO}$, PF, $\overline{ST}$, $\overline{PBRST}$, RST, $\overline{RST}$, and $\overline{NMI}$ pin open. I_{BAT} specified at 25°C.
3. I_{CCO1} is the maximum average load which the DS1236 can supply at V_{CC}-0.3V through the V_{CCO} pin during normal 5-volt operation.
4. I_{CCO2} is the maximum average load which the DS1236 can supply through the V_{CCO} pin during data retention battery supply operation, with a maximum drop of 0.8 volts.
5. With t_R = 5 µs.
6. V_{CCO} is approximately V_{BAT}-0.5V at 1 µA load.
7. Sleep mode is not invoked.
8. Sleep mode is invoked.
9. t_{REC} is the minimum time required before $\overline{CEI}$/$\overline{CEO}$ memory access is allowed.
10. t_{CE} maximum must be met to ensure data integrity on power loss.
11. IN input is less than V_{TP} but V_{CC} greater than V_{CCTP}.
12. All outputs except RST which is 25 µA maximum.
13. All outputs except $\overline{RST}$ and $\overline{NMI}$ which is 25 µA minimum.
14. Pulse width of $\overline{NMI}$ requires that the IN pin remain below V_{TP}. If the IN pin returns to a level above V_{TP} for a period longer than t_{IPD} and before the t_{NMI} period has elapsed, the $\overline{NMI}$ pin will immediately return to a high.
15. IN pin greater than V_{TP} when V_{CC} supply rises to V_{BAT}. Example: IN tied to GND.
16. IN pin less than V_{TP} when V_{CC} supply rises to V_{BAT}.
17. $\overline{CEI}$ low.
18. The WC/$\overline{SC}$ pin contains an internal latch which drives back on to the pin. This latch requires ±200 µamps to switch states. The $\overline{ST}$ pin will sink ±50 uamps in normal operation and ±1 µamp in the sleep mode.
19. $\overline{ST}$ should be active low before the watchdog is disabled (i.e., before the $\overline{ST}$ input is tristated).



DALLAS SEMICONDUCTOR

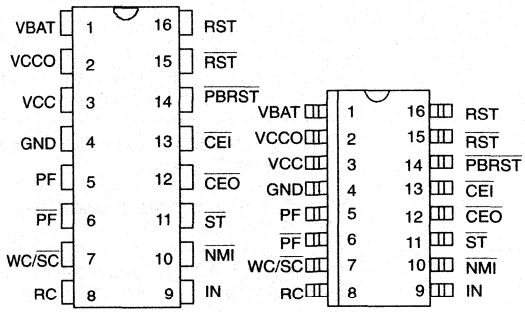
DS1236A
MicroManager Chip

3

FEATURES

- Holds microprocessor in check during power transients
- Halts and restarts an out-of-control microprocessor
- Monitors pushbutton for external override
- Warns microprocessor of an impending power failure
- Converts CMOS SRAM into nonvolatile memory
- Unconditionally write protects memory when power supply is out of tolerance
- Consumes less than 100 nA of battery current at 25°C
- Controls external power switch for high current applications
- Accurate 10% power supply monitoring
- Optional 5% power supply monitoring designated DS1236A-5
- Provides orderly shutdown in nonvolatile microprocessor applications
- Supplies necessary control for low-power "stop mode" in battery operated hand-held applications
- Standard 16-pin DIP or space-saving 16-pin SOIC
- Optional industrial temperature range -40°C to +85°C

PIN ASSIGNMENT



16-Pin DIP (300 Mil.) See Mech. Drawings Section

16-Pin SOIC (300 Mil.) See Mech. Drawings Section

PIN DESCRIPTION

V_{BAT}	–	+3 Volt Battery Input
V_{CCO}	–	Switched SRAM Supply Output
V_{CC}	–	+5 Volt Power Supply Input
GND	–	Ground
PF	–	Power Fail (Active High)
$\overline{PF}$	–	Power Fail (Active Low)
WC/$\overline{SC}$	–	Wake-Up Control (Sleep)
RC	–	Reset Control
IN	–	Early Warning Input
$\overline{NMI}$	–	Non-Maskable Interrupt
$\overline{ST}$	–	Strobe Input
$\overline{CEO}$	–	Chip Enable Output
$\overline{CEI}$	–	Chip Enable Input
$\overline{PBRST}$	–	Pushbutton Reset Input
$\overline{RST}$	–	Reset Output (Active Low)
RST	–	Reset Output (Active High)

DESCRIPTION

The DS1236A MicroManager Chip provides all the necessary functions for power supply monitoring, reset control, and memory backup in microprocessor-based systems. A precise internal voltage reference and comparator circuit monitor power supply status. When an out-of-tolerance condition occurs, the microprocessor reset and power fail outputs are forced active, and static RAM control unconditionally write protects external memory. The DS1236A also provides early warning detection of a user-defined threshold by driving a non-maskable interrupt. External reset control is provided by a pushbutton reset input which is debounced and activates reset outputs. An internal watchdog timer can also force the reset outputs to the active state if the strobe input is not driven low prior to watchdog time-out. Reset control and wake-up/sleep control inputs also provide the necessary signals for orderly shutdown and start-up in battery backup and battery operated applications. A block diagram of the DS1236A is shown in Figure 1.

PIN DESCRIPTION

PIN NAME	DESCRIPTION
V_{BAT}	+3V battery input provides nonvolatile operation of control functions.
V_{CCO}	V_{CC} output for nonvolatile SRAM applications.
V_{CC}	+5V primary power input.
PF	Power fail indicator, active high, used for external power switching as shown in Figure 9.
$\overline{PF}$	Power fail indicator, active low.
WC/$\overline{SC}$	Wake-up and Sleep control. Invokes low-power mode.
RC	Reset control input. Determines reset output . Normally low for NMOS processors and high for battery-backed CMOS processors.
IN	Early warning power fail input. This voltage sense point can be tied (via resistor divider) to a user-selected voltage.
$\overline{NMI}$	Non-maskable interrupt. Used in conjunction with the IN pin to indicate an impending power failure.
$\overline{ST}$	Strobe input. A high-to-low transition will reset the watchdog timer, indicating that software is still in control.
$\overline{CEO}$	Chip enable output. Used with nonvolatile SRAM applications.
$\overline{CEI}$	Chip enable input.
$\overline{PBRST}$	Pushbutton reset input.
$\overline{RST}$	Active low reset output.
RST	Active high reset output.

PROCESSOR MODE

A distinction is often made between CMOS and NMOS processor systems. In a CMOS system, power consumption may be a concern, and nonvolatile operation is possible by battery backing both the SRAM and the CMOS processor. All resources would be maintained in the absence of V_{CC}. A power-down reset is not issued since the low-power mode of most CMOS processors (Stop) is terminated with a Reset. A pulsed interrupt ($\overline{NMI}$) is issued to allow the CMOS processor to invoke a sleep mode to save power. For this case, a power-on reset is desirable to wake up and initialize the processor. The CMOS mode is invoked by connecting RC to V_{CCO}.

An NMOS processor consumes more power, and consequently may not be battery backed. In this case, it is desirable to notify the processor of a power fail, then keep it in reset during the loss of V_{CC}. This avoids intermittent or aberrant operation. On power-up, the processor will continue to be reset until V_{CC} reaches an operational level to provide an orderly start. The NMOS mode is invoked by connecting RC to ground.

POWER MONITOR

The DS1236A employs a band gap voltage reference and a precision comparator to monitor the 5-volt supply (V_{CC}) in microprocessor-based systems. When an out-of-tolerance condition occurs, the RST and $\overline{RST}$ outputs are driven to the active state. Th e V_{CC} trip point (V_{CCTP}) is set for 10% operation so that the RST and $\overline{RST}$ outputs will become active as V_{CC} falls below 4.5 volts (4.37 typical). The V_{CCTP} for the 5% operation option (DS1236A–5) is set for 4.75 volts (4.62 typical). The RST and $\overline{RST}$ signals are excellent for microprocessor reset control, as processing is stopped at the last possible moment of in-tolerance V_{CC}. On power-up, the RST and $\overline{RST}$ signals are held active for a minimum of 25 ms (100 ms typical) after V_{CCTP} is reached to allow the power supply and microprocessor to stabilize. Note: The operation described above is obtained with the reset control pin (RC) connected to GND (NMOS mode). Please review the reset control section for more information.

WATCHDOG TIMER

The DS1236A provides a watchdog timer function which forces the RST and $\overline{RST}$ signals to the active state when the strobe input ($\overline{ST}$) is not stimulated for a predetermined time period. This time period is 400 ms typically with a maximum time-out of 600 ms. The watchdog time-out period begins as soon as RST and $\overline{RST}$ are inactive. If a high-to-low transition occurs at the $\overline{ST}$ input prior to time-out, the watchdog timer is reset and begins to time out again. The $\overline{ST}$ input timing is shown in Figure 2. To guarantee the watchdog timer does not time out, a high-to-low transition on $\overline{ST}$ must occur at or less than 100 ms (minimum time-out) from a reset. If the watchdog timer is allowed to time out, the RST and $\overline{RST}$ outputs are driven to the active state for 25 ms minimum. The $\overline{ST}$ input can be derived from microprocessor address, data, and/or control signals. Under normal operating conditions, these signals would routinely reset the watchdog timer prior to time-out. If the watchdog timer is not required, two methods have been provided to disable it.

Permanently grounding the IN pin in the CMOS mode (RC=1) will disable the watchdog. In normal operation with RC=1, the watchdog is disabled as soon as the IN pin is below V_{TP}. With IN grounded, an $\overline{NMI}$ output will occur only at power-up, or when the $\overline{ST}$ pin is strobed. As shown in the Figure 3, a falling edge on $\overline{ST}$ will generate an $\overline{NMI}$ when IN is below V_{TP}. This allows the processor to verify that power is between V_{TP} and V_{CCTP}, as an $\overline{NMI}$ will be returned immediately after the $\overline{ST}$ strobe. The watchdog timer is not affected by the IN pin when in NMOS mode (RC=0).

If the $\overline{NMI}$ signal is required to monitor supply voltages, the watchdog may also be disabled by leaving the $\overline{ST}$ input open. Independent of the state of the RC pin, the watchdog is also disabled as soon as V_{CC} falls to V_{CCTP}.

PUSHBUTTON RESET

An input pin is provided on the DS1236A for direct connection to a pushbutton. The pushbutton reset input requires an active low signal. Internally, this input is pulled high by a 10K resistor whenever V_{CC} is greater than V_{BAT}. The $\overline{PBRST}$ pin is also debounced and timed such that the RST and $\overline{RST}$ outputs are driven to the active state for 25 ms minimum. This 25 ms delay begins as the pushbutton is released from a low level. A typical example of the power monitor, watchdog timer, and pushbutton reset connections are shown in Figure 4. The $\overline{PBRST}$ input is disabled whenever the IN pin voltage level is less than V_{TP} and the reset control (RC) is tied high (CMOS mode). The $\overline{PBRST}$ input is also disabled whenever V_{CC} is below V_{BAT}. Timing of the $\overline{PBRST}$-generated RST is illustrated in Figure 5.

NON-MASKABLE INTERRUPT

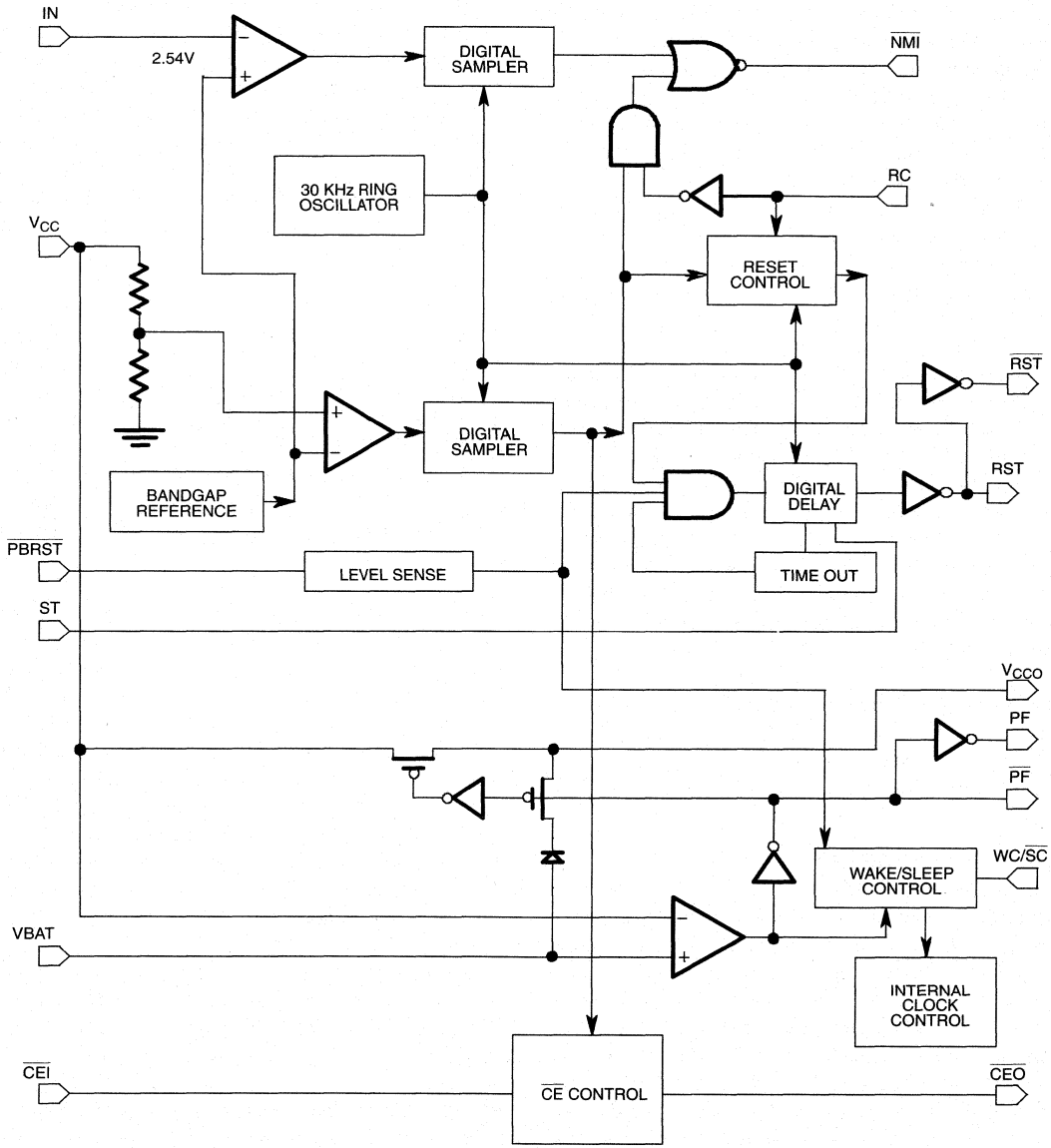
The DS1236A generates a non-maskable interrupt $\overline{NMI}$ for early warning of power failure to a microprocessor. A precision comparator monitors the voltage level at the IN pin relative to a reference generated by the internal band gap. The IN pin is a high impedance input allowing for a user-defined sense point. An external resistor voltage divider network (Figure 6) is used to interface with high voltage signals. This sense point may be derived from the regulated 5-volt supply or from a higher DC voltage level closer to the main system power input. Since the IN trip point V_{TP} is 2.54 volts, the proper values for R1 and R2 can be determined by the equation as shown in Figure 6. Proper operation of the DS1236A requires that the voltage at the IN pin be limited to V_{IN}. Therefore, the maximum allowable voltage at the supply being monitored (V_{MAX}) can also be derived as shown in Figure 6. A simple approach to solving this equation is to select a value for R2 high enough to keep power consumption low, and solve for R1. The flexibility of the IN input pin allows for detection of power loss at the earliest point in a power supply system, maximizing the amount of time for microprocessor shut-down between $\overline{NMI}$ and RST or $\overline{RST}$.

When the supply being monitored decays to the voltage sense point, the DS1236A pulses the $\overline{NMI}$ output to the active state for a minimum of 200 µs. The $\overline{NMI}$ power fail detection circuitry also has built-in time domain hysteresis. That is, the monitored supply is sampled periodically at a rate determined by an internal ring oscillator running at approximately 30 KHz (33 µs/cycle). Three consecutive samplings of out-of-tolerance supply (below V_{SENSE}) must occur at the IN pin to active $\overline{NMI}$. Therefore, the supply must be below the voltage sense point for approximately 100 µs or the comparator will reset. In this way, power supply noise is removed from the monitoring function, preventing false trips. During a power-up , any detected IN pin levels be low V_{TP} by the comparator are disabled from reaching the $\overline{NMI}$ pin until V_{CC} rises to V_{CCTP}. As a result, any potential $\overline{NMI}$ pulse will not be initiated until V_{CC} reaches V_{CCTP}.

Removal of an active low level on the $\overline{NMI}$ pin is controlled by either an internal time-out (when IN pin is less than V_{TP}) or by the subsequent rise of the IN pin above

V_{TP}. The initiation and removal of the $\overline{NMI}$ signal during power-up results in an $\overline{NMI}$ pulse of from 0 µs minimum to 500 µs maximum, depending on the relative voltage relationship between V_{CC} and the IN pin voltage. As an example, when the IN pin is tied to ground during power-up, the internal time-out will result in a pulse of 200 µs minimum to 500 µs maximum. In contrast, if the IN pin is tied to V_{CCO} during power-up, $\overline{NMI}$ will not produce a pulse on power-up. Note that a fast slewing power supply may cause the $\overline{NMI}$ to be virtually non-existent on power-up. This is of no consequence, however, since a $\overline{RST}$ will be active.

DS1236A FUNCTIONAL BLOCK DIAGRAM Figure 1



If the IN pin is connected to V_{CCO}, the $\overline{NMI}$ output will pulse low as V_{CC} decays to V_{CCTP} in the NMOS mode (RC=0). In the CMOS mode (RC=V_{CCO}) the power-down of V_{CC} out-of-tolerance at V_{CCTP} will not produce a pulse on the $\overline{NMI}$ pin. Given that any $\overline{NMI}$ pulse has been completed by the time V_{CC} decays to V_{CCTP}, the $\overline{NMI}$ pin will remain high. The $\overline{NMI}$ voltage will follow V_{CC} down until V_{CC} decays to V_{BAT}. Once V_{CC} decays to V_{BAT}, the $\overline{NMI}$ pin will either remain at V_{OHL} or enter tri-state mode as determined by the RC pin (see "Reset Control" section).

MEMORY BACKUP

The DS1236A provides all of the necessary functions required to battery back a static RAM. First, a switch is provided to direct SRAM power from the incoming 5 volt supply (V_{CC}) or from an external battery (V_{BAT}), whichever is greater. This switched supply (V_{CCO}) can also be used to battery back a CMOS microprocessor. For more information about nonvolatile processor applications, review the "Reset Control" and "Wake Control" sections. Second, the same power fail detection described in the power monitor section is used to hold the chip enable output ($\overline{CEO}$) to within 0.3 volts of V_{CC} or to within 0.7 volts of V_{BAT}. This write protection mechanism occurs as V_{CC} falls below V_{CCTP} as specified. If $\overline{CEI}$ is low at the time power fail detection occurs, $\overline{CEO}$ is held in its present state until $\overline{CEI}$ is returned high, or the period t_{CE} expires. This delay of write protection until the current memory cycle is completed prevents the corruption of data. If $\overline{CEO}$ is in an inactive state at the time of V_{CC} fail detection, $\overline{CEO}$ will be unconditionally disabled within t_{CF}. During nominal supply conditions $\overline{CEO}$ will follow $\overline{CEI}$ with a maximum propagation delay of 20 ns. Figure 7 shows a typical nonvolatile SRAM application. The DS1236A unlike the DS1236 can be operated without a battery. In this method of operation the V_{BAT}, pin 1, must be grounded. In general, it would also be expected to have the RC, pin 8, grounded (NMOS mode) since no battery backup is available.

FRESHNESS SEAL

In order to conserve battery capacity during initial construction of an end system, the DS1236A provides a freshness seal that electrically disconnects the battery. This means that upon battery attach, the V_{CCO} output will remain inactive until V_{CC} is applied. This prevents V_{CCO} from powering other devices when the battery is first attached, and V_{CC} is not present. Once V_{CC} is applied, the freshness seal is broken and cannot be invoked again without subsequent removal and re–attachment of the battery.

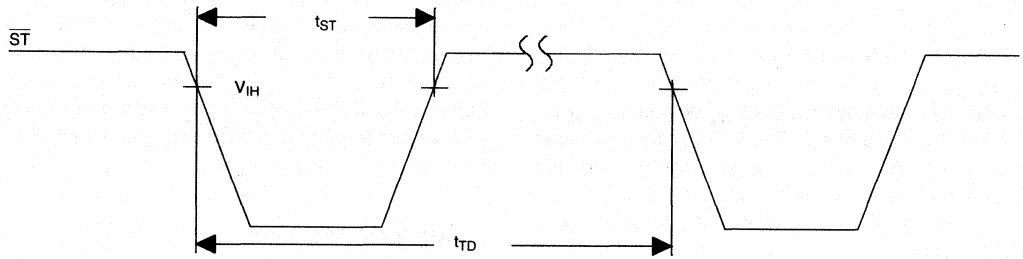
POWER SWITCHING

When larger operating currents are required in a battery-backed system, the 5-volt supply and battery supply switches internal to the DS1236A may not be large enough to support the required load through V_{CCO} with a reasonable voltage drop. For these applications, the PF and $\overline{PF}$ outputs are provided to gate external power switching devices. As shown in Figure 8, power to the load is switched from V_{CC} to battery on power-down, and from battery to V_{CC} on power- up. The DS1336 is designed to use the $\overline{PF}$ output to switch between V_{BAT} and V_{CC}. It provides better leakage and switchover performance than currently available discrete components. The transition threshold for PF and $\overline{PF}$ is set to the external battery voltage V_{BAT}, allowing a smooth transition between sources. The load applied to the PF pin from the external switch will be supplied by the battery. Therefore, if a discrete switch is used, this load should be taken into consideration when sizing the battery.

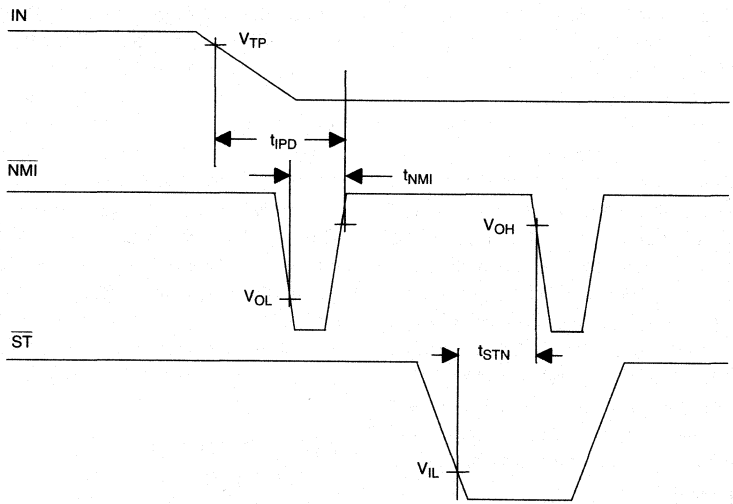
RESET CONTROL

As mentioned above, the DS1236A supports two modes of operation. The CMOS mode is used when the system incorporates a CMOS microprocessor which is battery backed. The NMOS mode is used when a non-battery backed processor is incorporated. The mode is selected by the RC (Reset Control) pin. The level of this pin distinguishes timing and level control on RST, $\overline{RST}$, and $\overline{NMI}$ outputs for volatile processor operation versus nonvolatile battery backup or battery-operated processor applications.

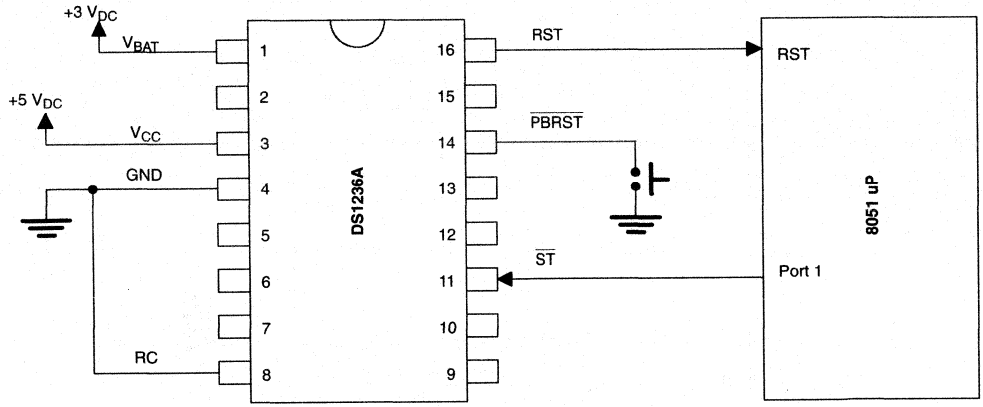
ST/INPUT TIMING Figure 2



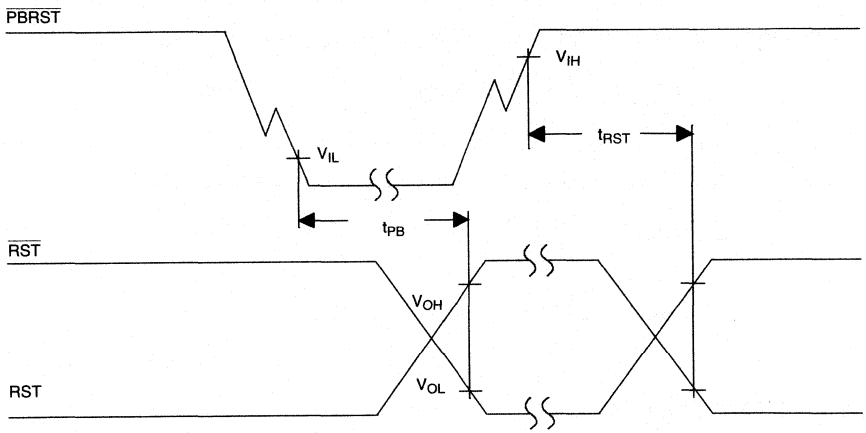
NMI/FROM ST/INPUT Figure 3



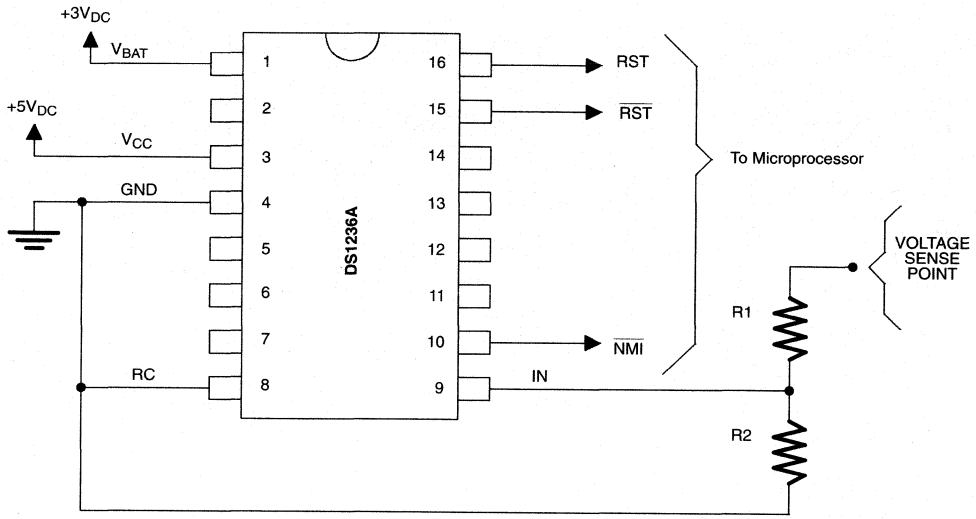
POWER MONITOR, WATCHDOG Figure 4



PUSH BUTTON RESET TIMING Figure 5



NON-MASKABLE INTERRUPT Figure 6



EXAMPLE 1: 5 VOLT SUPPLY, R2 = 10K OHM, V_{SENSE} = 4.80 VOLTS

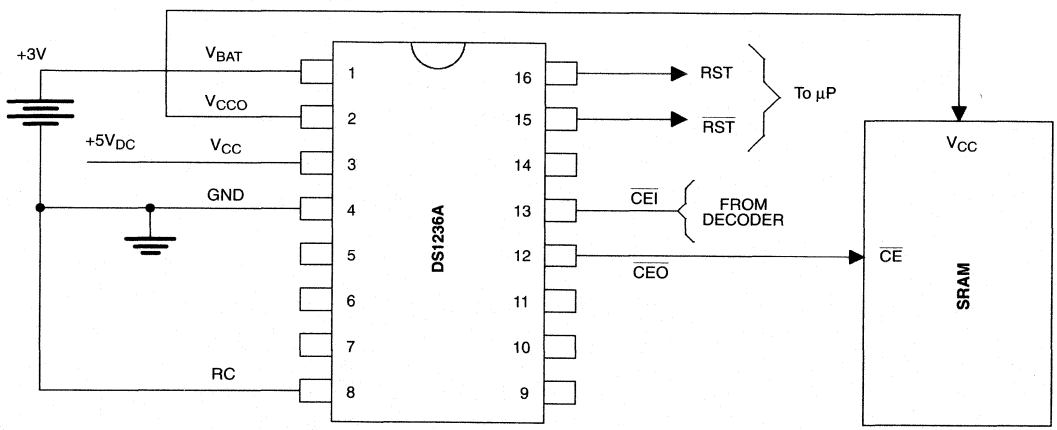
$$\therefore 4.80 = \frac{R1 + 10K}{10K} \times 2.54 \qquad R1 = 8.9K\ OHM$$

EXAMPLE 2: 12 VOLT SUPPLY, R2 = 10K OHM, V_{SENSE} = 9.00 VOLTS

$$\therefore 9.00 = \frac{R1 + 10K}{10K} \times 2.54 \qquad R1 = 25.4K\ OHM$$

$$V_{MAX} = \frac{9.00}{2.54} \times 5.00 = 17.7\ VOLTS$$

NONVOLATILE SRAM Figure 7



When the RC pin is tied to ground, the DS1236A is designed to interface with NMOS processors which do not have the microamp currents required during a battery backed mode. Grounding the RC pin does, however, continue to support nonvolatile backup of system SRAM memory. Nonvolatile systems incorporating NMOS processors generally require that only the SRAM memory and/or timekeeping functions be battery backed. When the processor is not battery backed (RC = 0), all signals connected from the processor to the DS1236A are disconnected from the backup battery supply, or grounded when system V_{CC} decays below V_{BAT}. In the NMOS processor system, the principal emphasis is placed on giving early warnings with $\overline{NMI}$, then providing a continuously active RST and $\overline{RST}$ signal during power-down while isolating the backup battery from the processor during a loss of V_{CC}.

During power-down, $\overline{NMI}$ will pulse low for a minimum of 200 µs, and then return high. If RC is tied low (NMOS mode), the voltage on $\overline{NMI}$ will follow V_{CC} until V_{CC} supply decays to V_{BAT}, at which point $\overline{NMI}$ will enter tri-state (see timing diagram). Also, upon V_{CC} out-of-tolerance at V_{CCTP}, the RST and $\overline{RST}$ outputs are driven active and RST will follow V_{CC} as the supply decays. On power-up, RST follows V_{CC} up, $\overline{RST}$ is held low, and both remain active for t_{RST} after valid V_{CC}. During a power-up from a V_{CC} voltage below V_{BAT}, any detected IN pin levels below V_{TP} are disabled from reaching the $\overline{NMI}$ pin until V_{CC} rises to V_{CCTP}. As a result, any potential $\overline{NMI}$ pulse will not be initiated until V_{CC} reaches V_{CCTP}. Removal of an active low level on the $\overline{NMI}$ pin is controlled by either an internal time-out (when the IN pin is less than V_{TP}), or by the subsequent rise of the IN pin above V_{TP}. The initiation and removal of the $\overline{NMI}$ signal results in an $\overline{NMI}$ pulse of 0 µs minimum to 500 µs maximum during power-up, depending on the relative voltage relationship between V_{CC} and the IN pin. As an example, when the IN pin is tied to ground, the internal time-out will result in a pulse of 200 µs minimum to 500 µs maximum. In contrast, if the IN pin is tied to V_{CCO}, $\overline{NMI}$ will not produce a pulse on power-up.

Connecting the RC pin to a high (V_{CCO}) invokes CMOS mode and provides nonvolatile support to both the system SRAM as well as a low power CMOS processor. When using CMOS microprocessors, it is possible to place the microprocessor into a very low- power mode termed the "stop" or "halt" mode. In this state the CMOS processor requires only microamp currents and is fully capable of being battery backed. This mode generally allows the CMOS microprocessor to maintain the contents of internal RAM as well as state control of I/O ports during battery backup. The processor can subsequently be restarted by any of several different signals. To maintain this low-power state, the DS1236A issues no $\overline{NMI}$ and/or reset signals to the processor until it is time to bring the processor back into full operation. To support the low-power processor battery backed mode (RC = 1), the DS1236A provides a pulsed $\overline{NMI}$ for early power failure warning. Waiting to initiate a Stop mode until after the $\overline{NMI}$ pin has returned high will guarantee the processor that no other active $\overline{NMI}$ or RST/$\overline{RST}$ will be issued by the DS1236A until one of two conditions occurs: 1) Voltage on the pin rises above V_{TP}, which activates the watchdog, or 2) V_{CC} cycles below then above V_{BAT}, which also results in an active RST and $\overline{RST}$. If V_{CC} does not fall below V_{CCTP}, the processor will be restarted by the reset derived from the watchdog timer as the IN pin rises above V_{TP}.

With the RC pin tied to V_{CCO}, RST and $\overline{RST}$ are not forced active as V_{CC} collapses to V_{CCTP}. The $\overline{RST}$ is held at a high level via the external battery as V_{CC} falls below battery potential. This mode of operation is intended for applications in which the processor is made nonvolatile with an external source, and allows the processor to power down into a Stop mode as signaled from $\overline{NMI}$ at an earlier voltage level. The $\overline{NMI}$ output pin will pulse low for t_{NMI} following a low voltage detect at the IN pin of V_{TP}. Following t_{NMI}, however, $\overline{NMI}$ will also be held at a high level (V_{BAT}) by the battery as V_{CC} decays below V_{BAT}. On power-up, RST and $\overline{RST}$ are held inactive until V_{CC} reaches V_{BAT}, then RST and $\overline{RST}$ are driven active for t_{RST}. If the IN pin falls below V_{TP} during an active reset, the reset outputs will be forced inactive by the $\overline{NMI}$ output. In addition, as long as the IN pin is less than V_{TP}, stimulation of the ST pin will result in additional $\overline{NMI}$ pulses. In this way, the $\overline{ST}$ pin can be used to allow the CMOS processor to determine if the supply voltage, as monitored by the IN pin, is above or below a selected operating value. This is illustrated in Figure 3. As discussed above, the RC pin determines the timing relationships and levels of several signals. The following section describes the power-up and power-down timing diagrams in more detail.

TIMING DIAGRAMS

This section provides a description of the timing diagrams shown in Figure 9, Figure 10, Figure 11, and Figure 12. These diagrams show the relative timing and levels in both the NMOS and the CMOS mode for power-up and down. Figure 9 illustrates the relationship for

power-down in CMOS mode. As V_{CC} falls, the IN pin voltage drops below V_{TP}. As a result, the processor is notified of an impending power failure via an active $\overline{NMI}$, which allows it to enter a sleep mode. As the power falls further, V_{CC} crosses V_{CCTP}, the power monitor trip point. Since the DS1236A is in CMOS mode, no reset is generated. The $\overline{RST}$ voltage will follow V_{CC} down, but will fall no further than V_{BAT}. At this time, $\overline{CEO}$ is brought high to write protect the RAM. When the V_{CC} reaches V_{BAT}, a power fail is issued via the PF and $\overline{PF}$ pins.

Figure 10 illustrates operation of the power-down sequence in NMOS mode. Once again, as power falls, an $\overline{NMI}$ is issued. This gives the processor time to save critical data in nonvolatile SRAM. When V_{CC} reaches V_{CCTP}, an active RST and $\overline{RST}$ are given. The RST voltage will follow V_{CC} as it falls. $\overline{CEO}$, PF, and $\overline{PF}$ will operate in a similar manner to CMOS mode. Notice that the $\overline{NMI}$ will tri-state to prevent a loss of battery power.

Figure 11 shows the power-up sequence for the NMOS mode. As V_{CC} slews above V_{BAT}, the PF and $\overline{PF}$ pins are deactivated. An active reset occurs as well as an $\overline{NMI}$. Although the $\overline{NMI}$ may be short due to slew rates, reset will be maintained for the standard t_{RST} time-out period. At a later time, if the IN pin falls below V_{TP}, a new $\overline{NMI}$ will occur. If the processor does not issue a $\overline{ST}$, a watchdog reset will also occur. The second $\overline{NMI}$ and RST are provided to illustrate these possibilities.

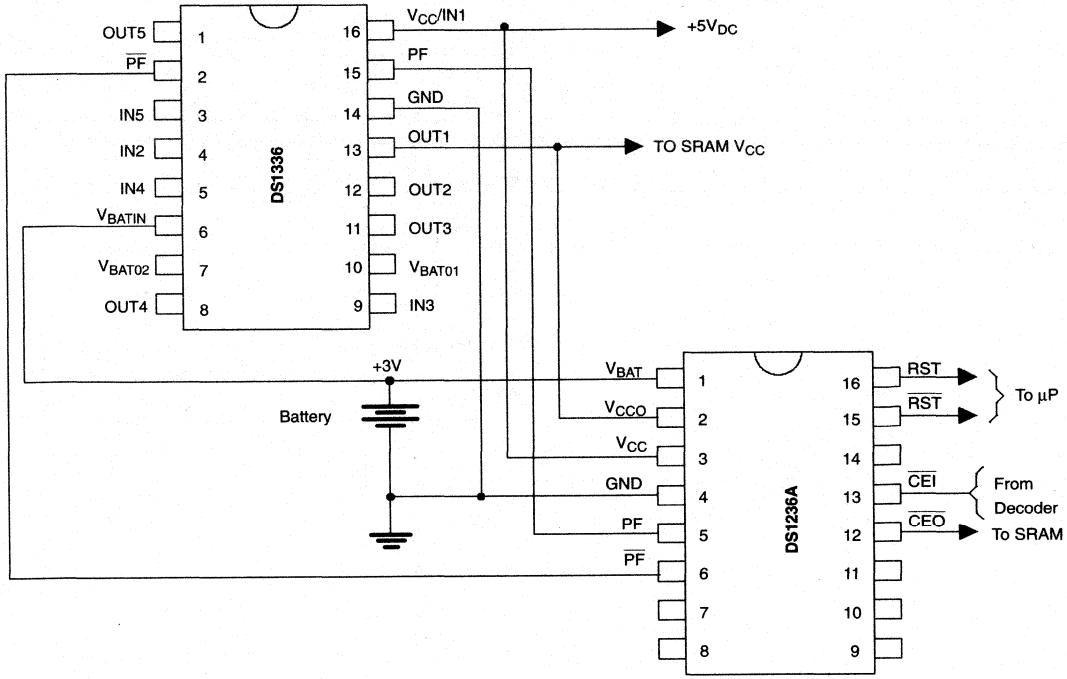
Figure 12 illustrates the power-up timing for CMOS mode. The principal difference is that the DS1236A issues a reset immediately in the NMOS mode. In CMOS mode, a reset is issued when IN rises above V_{TP}. Depending on the processor type, the $\overline{NMI}$ may terminate the Stop mode in the processor.

WAKE CONTROL/SLEEP CONTROL

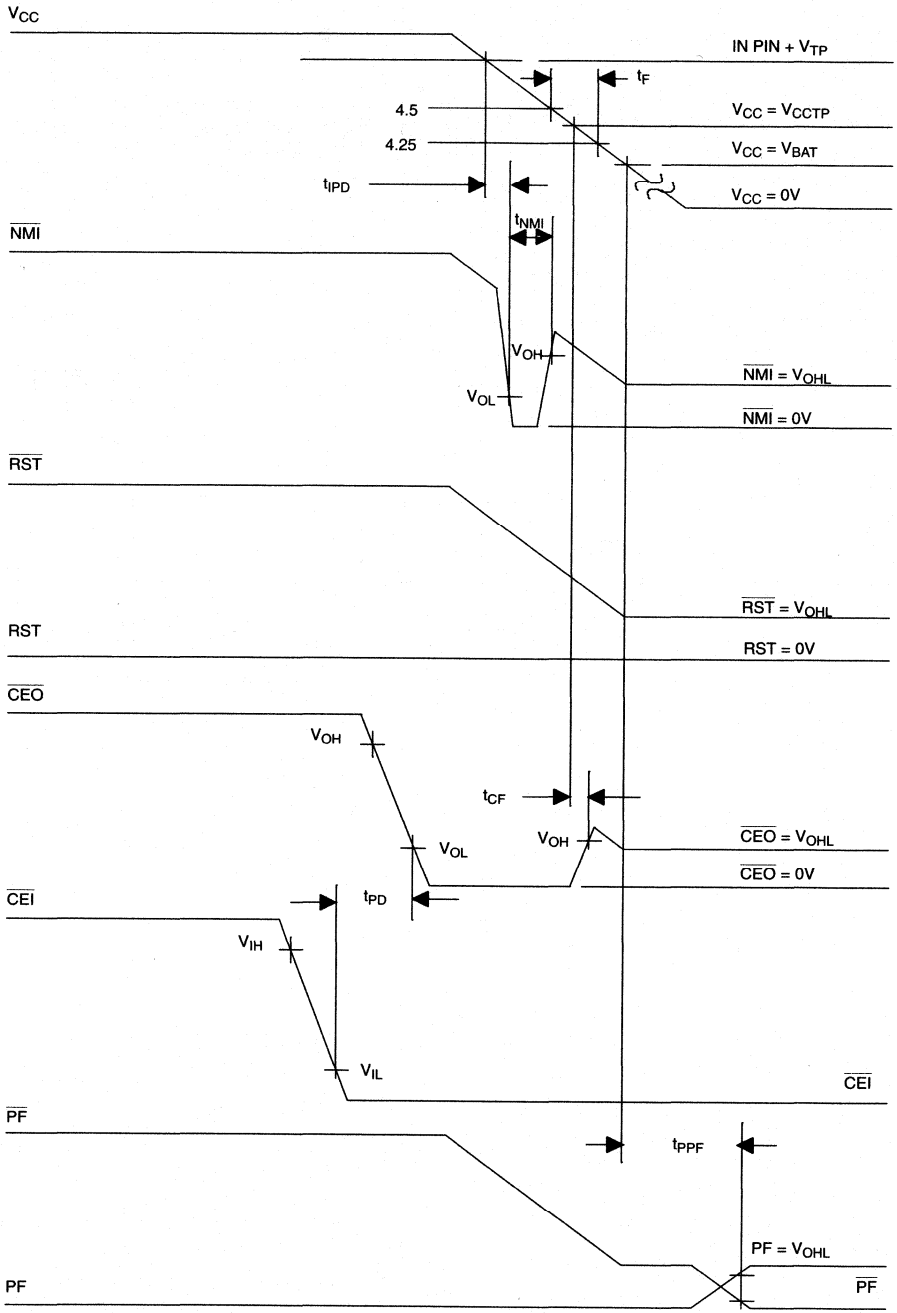
The Wake/Sleep Control input (WC/$\overline{SC}$) allows the processor to disable all comparators on the DS1236A before entering the Stop mode. This feature allows the DS1236A, processor, and static RAM to maintain nonvolatility in the lowest power mode possible. The processor may invoke the sleep mode in battery-operated applications to conserve battery capacity when an absence of activity is detected. The operation of this signal is shown in Figure 13. The DS1236A may subsequently be restarted by a high-to-low transition on the $\overline{PBRST}$ input through human interface via a keyboard, touchpad, etc. The processor will then be restarted as the watchdog times out and drives RST and $\overline{RST}$ active. The DS1236A can also be started up by forcing the WC/$\overline{SC}$ pin high from an external source. Also, if the DS1236A is placed in a sleep mode by the processor and system power is lost, the DS1236A will wake up the next time V_{CC} rises above V_{BAT}. These possibilities are illustrated in Figure 14.

When the sleep mode is invoked during normal power-valid conditions, all operation on the DS1236A is disabled, thus leaving the $\overline{NMI}$, RST, and $\overline{RST}$ outputs disabled as well as the $\overline{ST}$ and IN inputs. However, a loss of power during a sleep mode will result in an active RST and $\overline{RST}$ when the RC pin is grounded (NMOS mode). If the RC pin is tied high, the RST and $\overline{RST}$ pins will remain inactive during power-down in a sleep mode. Removal of the sleep mode by the $\overline{PBRST}$ input is not affected by the IN pin threshold at V_{TP} when the RC pin is tied high (CMOS mode). Subsequent power-up of the V_{CC} supply with the RC pin tied high will activate the RST and $\overline{RST}$ outputs as the main supply rises above V_{BAT}. A high-to-low transition on the WC/$\overline{SC}$ pin must follow a high-to-low transition on the ST pin by t_{WC} to invoke a Sleep mode for the DS1236A.

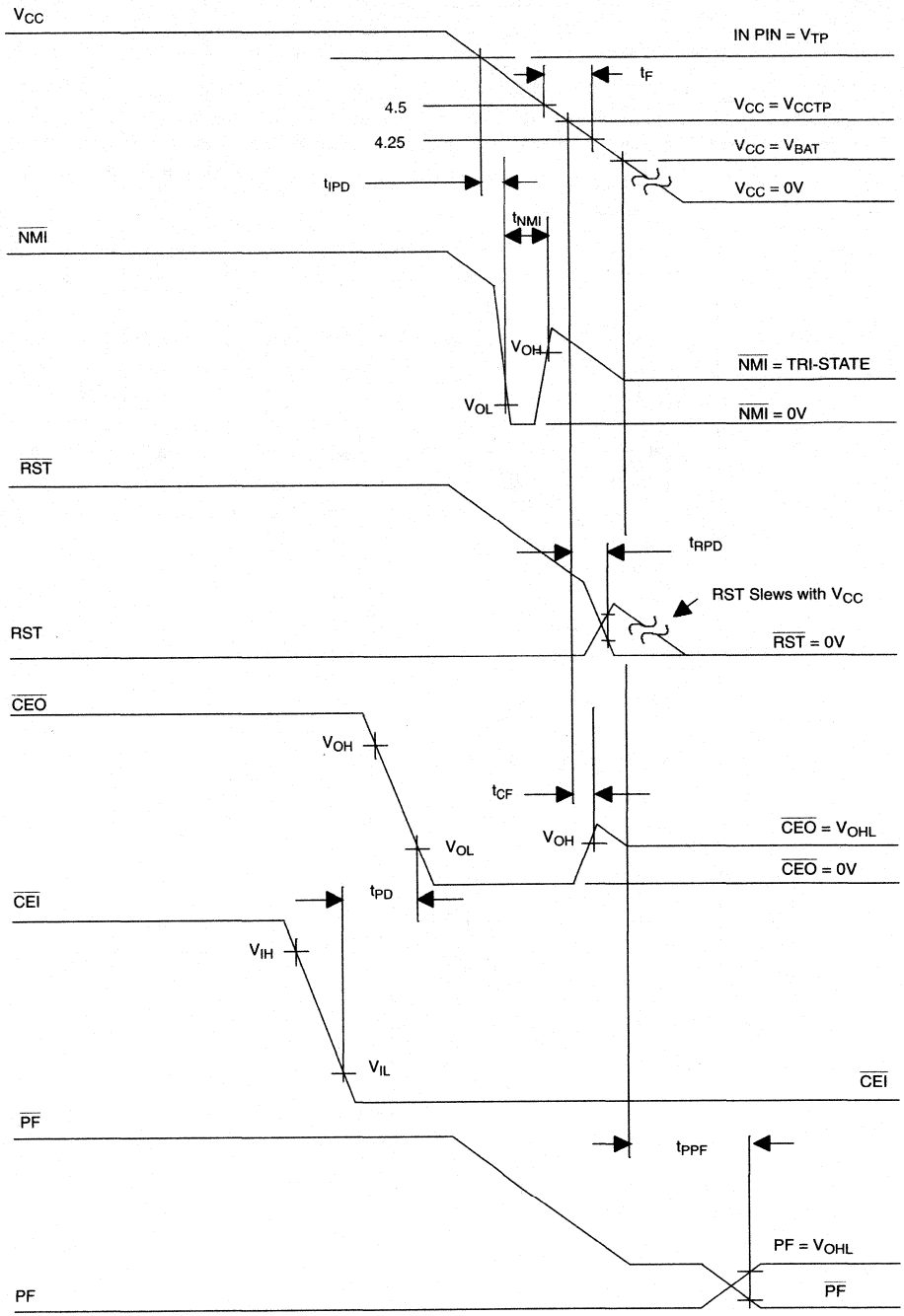
POWER SWITCHING



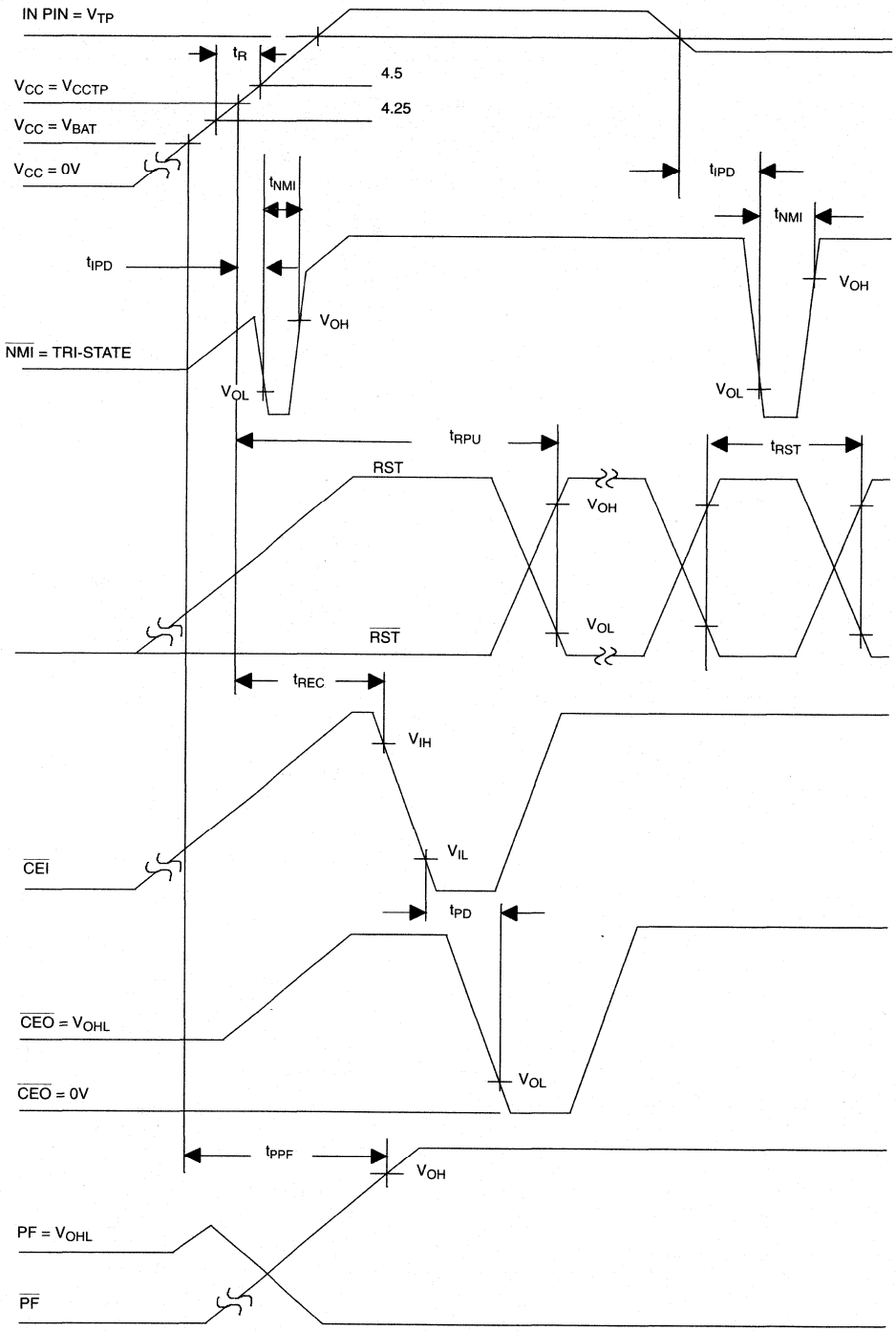
CMOS MODE POWER-DOWN (RC = V_{CCO}) Figure 9



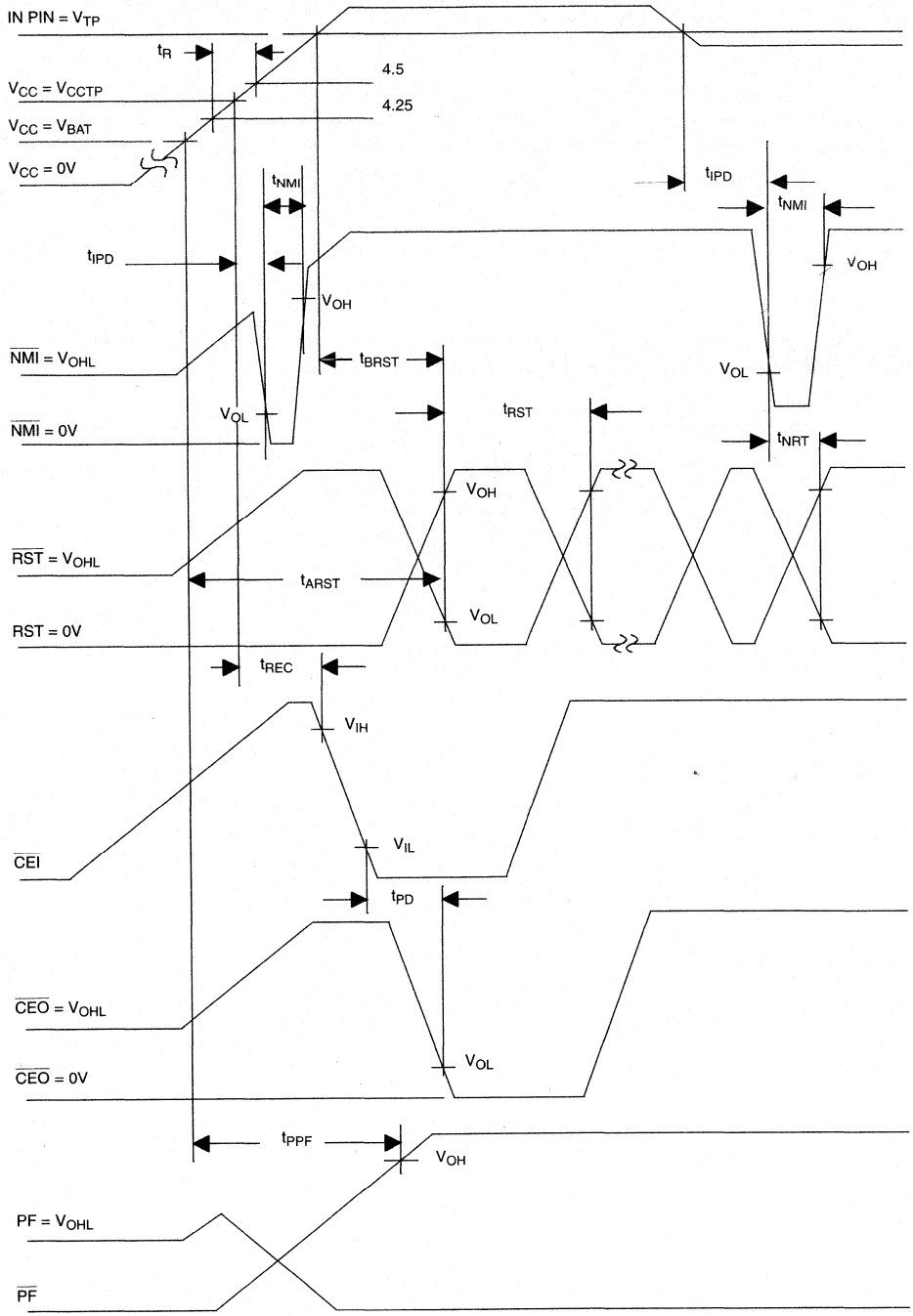
NMOS MODE POWER-DOWN (RC = GND) Figure 10



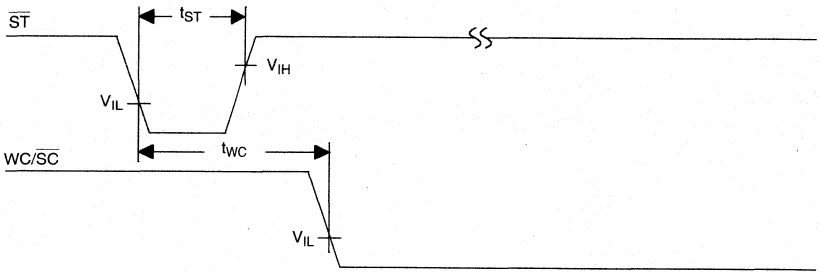
NMOS MODE POWER-UP (RC = GND) Figure 11



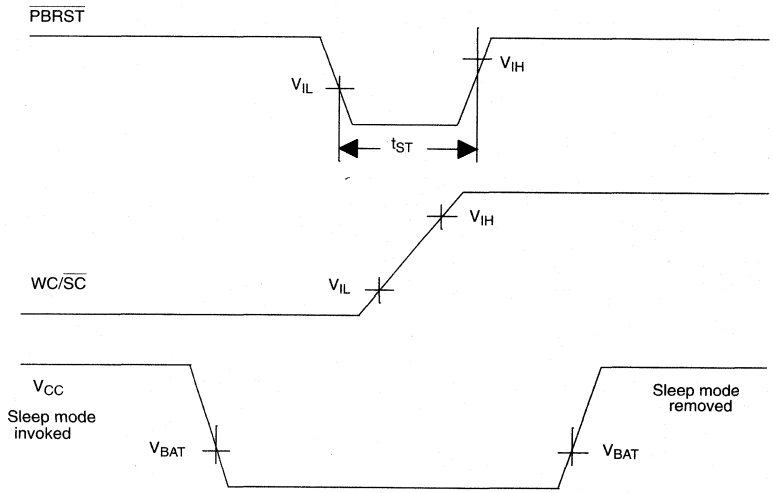
CMOS MODE POWER-UP (RC = V_{CCO}) Figure 12



WAKE/SLEEP CONTROL Figure 13



OPTIONS FOR INVOKING WAKEUP Figure 14



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	–0.5V to +7.0V
Voltage on I/O Relative to Ground	–0.5V to V_{CC} + 0.5V
Operating Temperature	0°C to 70°C
Operating Temperature (Industrial Version)	–40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Supply Voltage (5% Option)	V_{CC}	4.75	5.0	5.5	V	1
Input High Level	V_{IH}	2.0		V_{CC}+0.3	V	1
Input Low Level	V_{IL}	-0.3		+0.8	V	1
IN Input Pin	V_{IN}	-0.3		V_{CC} +0.3	V	1
Battery Input	V_{BAT}	0		4.0	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=4.5 V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}			4	mA	2
Sleep Supply Current in Sleep Mode	I_{CC}			20	µA	
Battery Current	I_{BAT}			0.1	µA	2
Supply Output Current (V_{CCO}=V_{CC} - 0.3V)	I_{CC01}			100	mA	3
Supply Output Current in Data Retention (V_{CC} < V_{BAT})	I_{CC02}			1	mA	4
Supply Output Voltage	V_{CCO}		V_{CC} -0.3		V	1
Battery Backup Voltage	V_{CCO}		V_{BAT} -0.7		V	1,6
Low Level @ RST	V_{OL}			0.4	V	1
Output Voltage @ –500 µA	V_{OH}	V_{CC}–0.5V	V_{CC}–0.1V		V	1
$\overline{CEO}$ and PF Output	V_{OHL}		V_{BAT} -0.7		V	1,6,19
$\overline{PBRST}$ Pull Up Resistor	R_{PBRST}	10K			Ω	
Input Leakage Current	I_{LI}	-1.0		+1.0	µA	18
Output Leakage	I_{LO}	-1.0		+1.0	µA	18
Output Current @0.4V	I_{OL}			4.0	mA	12
Output Current @2.4V	I_{OH}	-1.0			mA	13
Power Sup. Trip Point	V_{CCTP}	4.25	4.37	4.50	V	1
Power Supply Trip (5% Option)	V_{CCTP}	4.50	4.62	4.75	V	1
IN Input Pin Current	I_{CCIN}	-1.0		+1.0	µA	
IN Input Trip Point	V_{TP}	2.5	2.54	2.6	V	1

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} Fail Detect to RST, $\overline{RST}$	t_{RPD}	40	100	175	µs	
V_{TP} to $\overline{NMI}$	t_{IPD}	40	100	175	µs	
RESET Active Time	t_{RST}	25	100	150	ms	
$\overline{NMI}$ Pulse Width	t_{NMI}	200	300	500	µs	14
$\overline{ST}$ Pulse Width	t_{ST}	20			ns	20
$\overline{PBRST}$ @ V_{IL}	t_{PB}	30			ms	
V_{CC} Slew Rate 4.75 to 4.25	t_F	300			µs	
Chip Enable Propagation Delay	t_{PD}			20	ns	
V_{CC} Fail to Chip Enable High	t_{CF}	7	12	44	µs	17
V_{CC} Valid to RST, $\overline{RST}$ (RC=1)	t_{FPU}			100	ns	
V_{CC} Valid to RST & $\overline{RST}$	t_{RPU}	25	100	150	ms	5
V_{CC} Slew to 4.24 to V_{BAT}	t_{FB1}	10			µs	7
V_{CC} Slew 4.25 to 4.75 V_{BAT}	t_{FB2}	100			µs	8
Chip Enable Output Recovery Time	t_{REC}	.1			µs	9
V_{CC} Slew 4.25 to 4.75	t_R	0			µs	
Chip Enable Pulse Width	t_{CE}			5	s	10
Watchdog Time Delay	t_{TD}	100	400	600	ms	
$\overline{ST}$ to WC/$\overline{SC}$	t_{WC}	0.1		50	µs	
V_{BAT} Detect to PF, $\overline{PF}$	t_{PPF}			2	µs	7
$\overline{ST}$ to $\overline{NMI}$	t_{STN}			30	ns	11
$\overline{NMI}$ to RST & $\overline{RST}$	t_{NRT}			30	ns	
V_{BAT} Detect to RST & $\overline{RST}$	t_{ARST}			200	µs	15
V_{CC} Valid to RST, $\overline{RST}$	t_{BRST}	30	100	150	µs	16

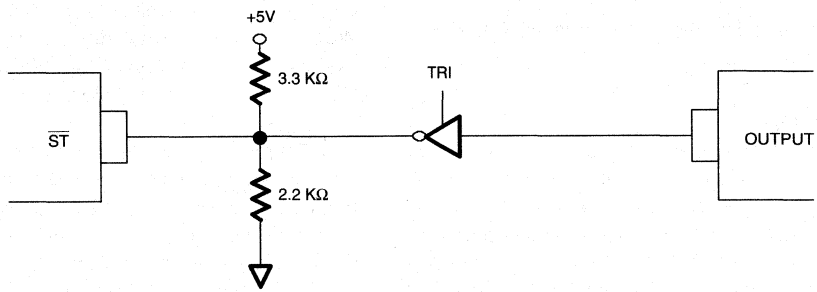
CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

NOTES:

1. All voltages referenced to ground. A 0.1 µF capacitor is recommended between V_{CC} and GND.
2. Measured with V_{CCO}, $\overline{CEO}$, $\overline{PF}$, PF, $\overline{ST}$, $\overline{PBRST}$, RST, $\overline{RST}$, and $\overline{NMI}$ pin open. I_{BAT} specified at 25°C.
3. I_{CCO1} is the maximum average load which the DS1236A can supply at V_{CC}-0.3V through the V_{CCO} pin during normal 5-volt operation.
4. I_{CCO2} is the maximum average load which the DS1236A can supply through the V_{CCO} pin during data retention battery supply operation, with a maximum drop of 0.8 volts.
5. With t_R = 5 µs.
6. V_{CCO} is approximately V_{BAT}-0.5V at 1 µA load.
7. Sleep mode is not invoked.
8. Sleep mode is invoked.
9. t_{REC} is the minimum time required before $\overline{CEI}$/$\overline{CEO}$ memory access is allowed.
10. t_{CE} maximum must be met to ensure data integrity on power loss.
11. IN input is less than V_{TP} but V_{CC} greater than V_{CCTP}.
12. All outputs except RST which is 25 µA maximum.
13. All outputs except $\overline{RST}$ and $\overline{NMI}$, which is 25 µA minimum.
14. Pulse width of $\overline{NMI}$ requires that the IN pin remain below V_{TP}. If the IN pin returns to a level above V_{TP} for a period longer than t_{IPD} and before the t_{NMI} period has elapsed, the $\overline{NMI}$ pin will immediately return to a high.
15. IN pin greater than V_{TP} when V_{CC} supply rises to V_{BAT}. Example: IN tied to GND.
16. IN pin less than V_{TP} when V_{CC} supply rises to V_{BAT}.
17. $\overline{CEI}$ low.
18. The WC/$\overline{SC}$ pin contains an internal latch which drives back on to the pin. This latch requires ±200 µamps to switch states. The $\overline{ST}$ pin will sink ±50 uamps in normal operation and ±1 µamp in the sleep mode.
19. If no battery is attached (i.e., V_{BAT}=GND) then V_{OHL} will track V_{CC}.
20. $\overline{ST}$ should be active low before the watchdog is disabled (i.e., before the $\overline{ST}$ input is tristated).



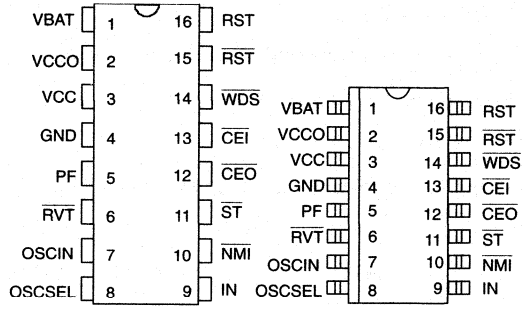
DALLAS SEMICONDUCTOR

DS1238 MicroManager

FEATURES

- Holds microprocessor in check during power transients
- Halts and restarts an out-of-control microprocessor
- Warns microprocessor of an impending power failure
- Converts CMOS SRAM into nonvolatile memory
- Unconditionally write protects memory when power supply is out of tolerance
- Delays write protection until completion of the current memory cycle
- Consumes less than 200 nA of battery current
- Controls external power switch for high current applications
- Debounces pushbutton reset
- Accurate 10% power supply monitoring
- Optional 5% power supply monitoring designated DS1238-5
- Provides orderly shutdown ini mcroprocessor applications
- Pin-for-pin compatible with MAX691
- Standard 16-pin DIP or space-saving 16-pin SOIC
- Optional industrial temperature range -40°C to +85°C

PIN ASSIGNMENT



16-Pin DIP (300 Mil.) See Mech. Drawings Section

16-Pin SOIC (300 Mil.) See Mech. Drawings Section

PIN DESCRIPTION

V_{BAT}	–	+3 Volt Battery Input
V_{CCO}	–	Switched SRAM Supply Output
V_{CC}	–	+5 Volt Power Supply Input
GND	–	Ground
PF	–	Power Fail
$\overline{RVT}$	–	Reset Voltage Threshold
OSCIN	–	Oscillator In
OSCSEL	–	Oscillator Select
IN	–	Early Warning Input
$\overline{NMI}$	–	Non–Maskable Interrupt
$\overline{ST}$	–	Strobe Input
$\overline{CEO}$	–	Chip Enable Output
$\overline{CEI}$	–	Chip Enable Input
$\overline{WDS}$	–	Watchdog Status
$\overline{RST}$	–	Reset Output (active low)
RST	–	Reset Output (active high)

DESCRIPTION

The DS1238 MicroManager provides all the necessary functions for power supply monitoring, reset control, and memory backup in microprocessor-based systems. A precise internal voltage reference and comparator circuit monitor power supply status. When an out-of-tolerance condition occurs, the microprocessor reset and power fail outputs are forced active, and static RAM control unconditionally write protects external memory. The DS1238 also provides early warning detection of a user-defined threshold by driving a non-maskable interrupt. External reset control is provided by a pushbutton reset debounce circuit connected to the $\overline{RST}$ pin. An internal watchdog timer can also force the reset outputs to the active state if the strobe input is not driven low prior to watchdog timeout. Oscillator control pins OSCSEL and OSCIN provide either external or internal clock timing for both the reset pulse width and the watchdog timeout period. The Watchdog Status and Reset Voltage Threshold are provided via $\overline{WDS}$ and $\overline{RVT}$, respectively. A block diagram of the DS1238 is shown in Figure 1.

PIN DESCRIPTION

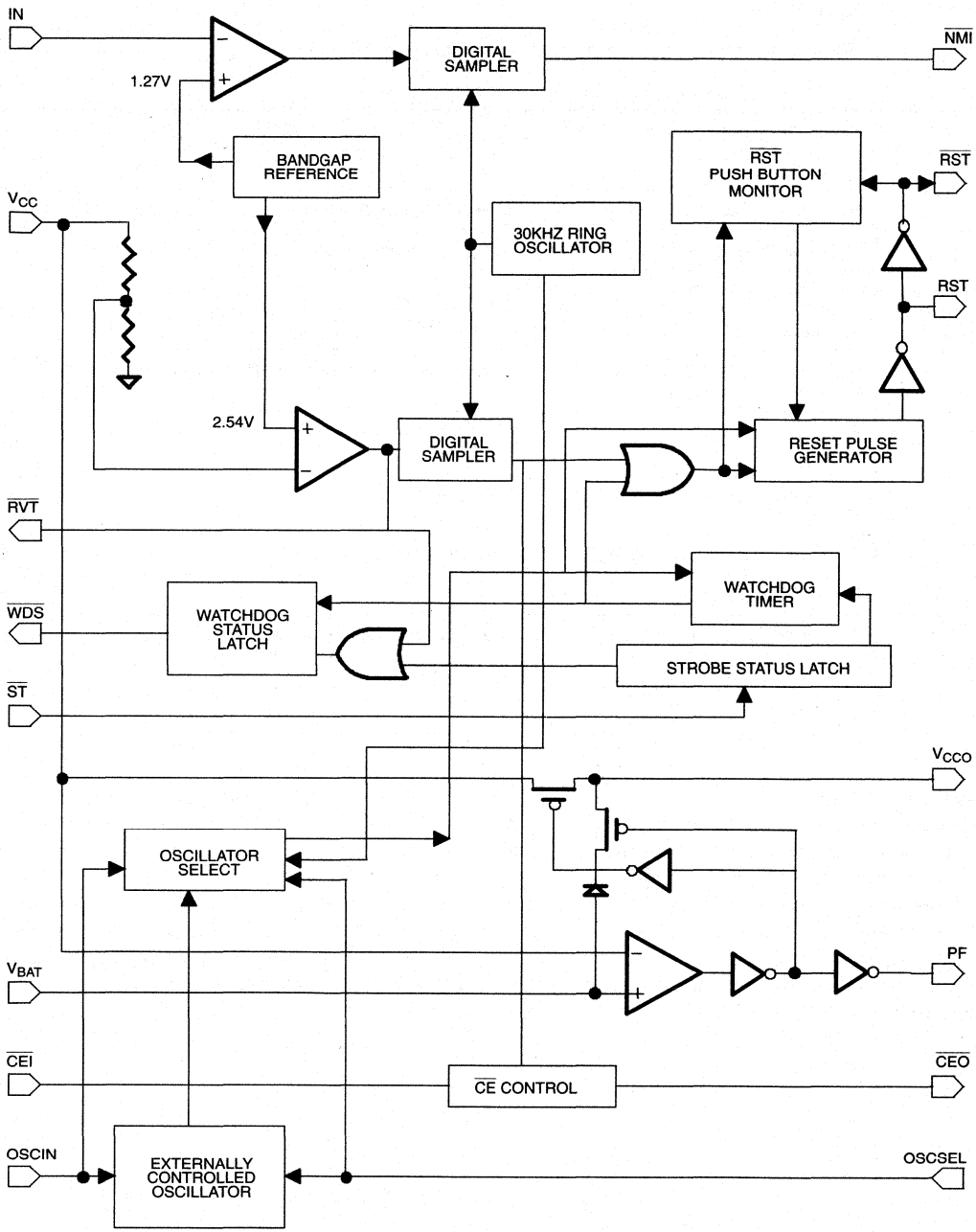
PIN NAME	DESCRIPTION
V_{BAT}	+3V Battery Input provides nonvolatile operation of control functions.
V_{CCO}	V_{CC} output for nonvolatile SRAM applications.
V_{CC}	+5V primary power input.
GND	System ground.
PF	Power fail indicator, active high, used for external power switching as shown in Figure 9.
$\overline{RVT}$	Reset Voltage Threshold. Indicates that V_{CC} is below the reset voltage threshold.
OSCIN	Oscillator input or timing capacitor. See Table 1.
OSCSEL	Oscillator Select. Selects internal or external clock functions. See Table 1.
IN	Early warning power fail input. This voltage sense point may be tied (via resistor divider) to a user-selected voltage.
$\overline{NMI}$	Non-maskable interrupt. Output used in conjunction with the IN pin to indicate an impending power failure.
$\overline{ST}$	Strobe input. A high–to–low transition will reset the watchdog timer, indicating that software is still in control.
$\overline{CEO}$	Chip enable output. Write protected. Used with nonvolatile SRAM applications.
$\overline{CEI}$	Chip enable input.
$\overline{WDS}$	Watchdog Status. Indicates that a watchdog timeout has occurred.
$\overline{RST}$	Active low reset output.
RST	Active high reset output.

3

POWER MONITOR

The DS1238 employs a band gap voltage reference and a precision comparator to monitor the 5–volt supply (V_{CC}) in microprocessor-based systems. When an out-of-tolerance condition occurs, the $\overline{RVT}$, RST, and $\overline{RST}$ outputs are driven to the active state. The V_{CC} trip point (V_{CCTP}) is set for 10% operation so that the $\overline{RVT}$, RST and $\overline{RST}$ outputs will become active as V_{CC} falls below 4.5 volts (4.37 typical). The V_{CCTP} for the 5% operation option (DS1238-5) is set for 4.75 volts (4.62 typical). The RST and $\overline{RST}$ signals are excellent for microprocessor reset control, as processing is stopped at the last possible moment of in-tolerance V_{CC}. On power up, $\overline{RVT}$ will become inactive as soon as V_{CC} rises above V_{CCTP}. However, the RST and $\overline{RST}$ signals remain active for a minimum of 50 ms (100 ms typical) after V_{CCTP} is reached to allow the power supply and microprocessor to stabilize.

DS1238 FUNCTIONAL BLOCK DIAGRAM Figure 1



WATCHDOG TIMER

The DS1238 provides a watchdog timer function which forces the $\overline{WDS}$, RST, and $\overline{RST}$ signals to the active state when the strobe input ($\overline{ST}$) is not stimulated for a predetermined time period. This time period is described below in Table 1. The watchdog timeout period begins as soon as RST and $\overline{RST}$ are inactive. If a high-to-low transition occurs at the $\overline{ST}$ input prior to time out, the watchdog timer is reset and begins to time out again. The $\overline{ST}$ input timing is shown in Figure 2. In order to guarantee that the watchdog timer does not timeout, a high-to-low transition on $\overline{ST}$ must occur at or less than the minimum timeout of the watchdog as described in the AC Electrical Characteristics. If the watchdog timer is allowed to time out, the $\overline{WDS}$, RST, and $\overline{RST}$ outputs are driven to the active state. $\overline{WDS}$ is a latched signal which indicates the watchdog status, and is activated as soon as the watchdog timer completes a full period as outlined in Table 1. The $\overline{WDS}$ pin will remain low until one of three operations occurs. The first is to strobe the $\overline{ST}$ pin with a falling edge, which will both set the $\overline{WDS}$ as well as the watchdog timer count. The second is to leave the $\overline{ST}$ pin open, which disables the watchdog. Lastly, the $\overline{WDS}$ pin is active low whenever V_{CC} falls below V_{CCTP} and activates the $\overline{RVT}$ signal. The $\overline{ST}$ input can be derived from microprocessor address, data, or control signals, as well as microcontroller port pins. Under normal operating conditions, these signals would routinely reset the watchdog timer prior to time out. The watchdog is disabled by leaving the $\overline{ST}$ input open, or as soon as V_{CC} falls to V_{CCTP}.

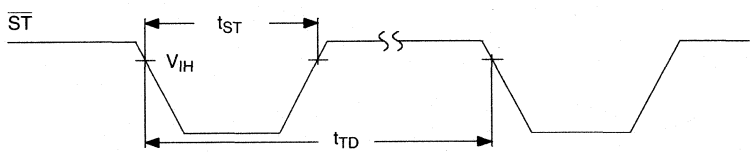
NON–MASKABLE INTERRUPT

The DS1238 generates a non-maskable interrupt ($\overline{NMI}$) for early warning of a power failure to the microprocessor. A precision comparator monitors the voltage level at the IN pin relative to an on-chip reference generated by an internal band gap. The IN pin is a high impedance input allowing for a user-defined sense point. An external resistor voltage divider network (Figure 5) is used to interface with high voltage signals. This sense point may be derived from the regulated 5-volt supply, or from a higher DC voltage level closer to the main system power input. Since the IN trip point V_{TP} is 1.27 volts, the proper values for R1 and R2 can be determined by the equation as shown in Figure 5. Proper operation of the DS1238 requires that the voltage at the IN pin be limited to V_{IH}. Therefore, the maximum allowable voltage at the supply being monitored (V_{MAX}) can also be derived as shown in Figure 5. A simple approach to solving this equation is to select a value for R2 of high enough value to keep power consumption low, and solve for R1. The flexibility of the IN input pin allows for detection of power loss at the earliest point in a power supply system, maximizing the amount of time for microprocessor shut-down between $\overline{NMI}$ and RST or $\overline{RST}$.

When the supply being monitored decays to the voltage sense point, the DS1238 will force the $\overline{NMI}$ output to an active state. Noise is removed from the $\overline{NMI}$ power fail detection circuitry using built-in time domain hysteresis. That is, the monitored supply is sampled periodically at a rate determined by an internal ring oscillator running at approximately 30 KHz (33 µs/cycle). Three consecutive samplings of out-of-tolerance supply (below V_{SENSE}) must occur at the IN pin to active $\overline{NMI}$. Therefore, the supply must be below the voltage sense point for approximately 100 µs or the comparator will reset. In this way, power supply noise is removed from the monitoring function preventing false trips. During a power–up, any IN pin levels below V_{TP} detected by the comparator are disabled from reaching the $\overline{NMI}$ pin until V_{CC} rises to V_{CCTP}. As a result, any potential active $\overline{NMI}$ will not be initiated until V_{CC} reaches V_{CCTP}.

Removal of an active low level on the $\overline{NMI}$ pin is controlled by the subsequent rise of the IN pin above V_{TP}. The initiation and removal of the $\overline{NMI}$ signal during power up depends on the relative voltage relationship between V_{CC} and the IN pin voltage. Note that a fast slewing power supply may cause the $\overline{NMI}$ to be virtually non-existent on power up. This is of no consequence however, since an RST will be active. The $\overline{NMI}$ voltage will follow V_{CC} down until V_{CC} decays to V_{BAT}. Once V_{CC} decays to $V\overline{BAT}$, the $\overline{NMI}$ pin will enter a tri-state mode.

$\overline{ST}$ INPUT TIMING Figure 2

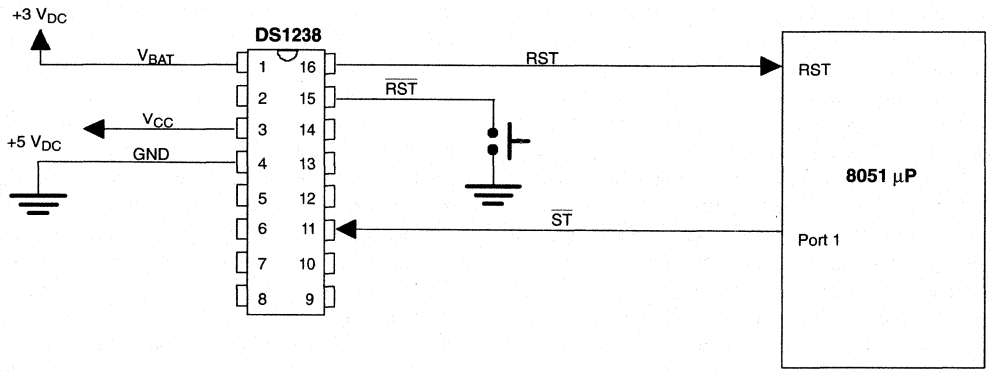


OSCILLATOR CONTROLS Table 1

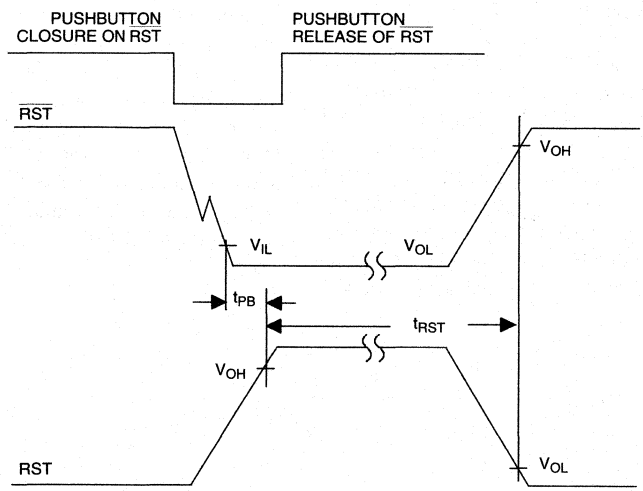
	OSCIN	OSCSEL	Watchdog Timeout Period (typ)		
			First Period Following a Reset	Other Timeout	Reset Active Duration
External	Ext Clk	Low	20480 Clks	5120 Clocks	641 Clks
	Ext Cap	Low	$\cong \frac{2.2\ sec}{47\ pf}$ X Cpf	$\cong \frac{550\ ms}{47\ pf}$ X Cpf	$\cong \frac{69\ ms}{47\ pf}$ X Cpf
Internal	Low	Hi/Open	2.7 sec	170 ms	85 ms
	Hi/Open	Hi/Open	2.7 sec	2.7 sec	85 ms

Note that the OSCIN and OSCSEL pins are tri-stated when V_{CC} is below V_{BAT}.

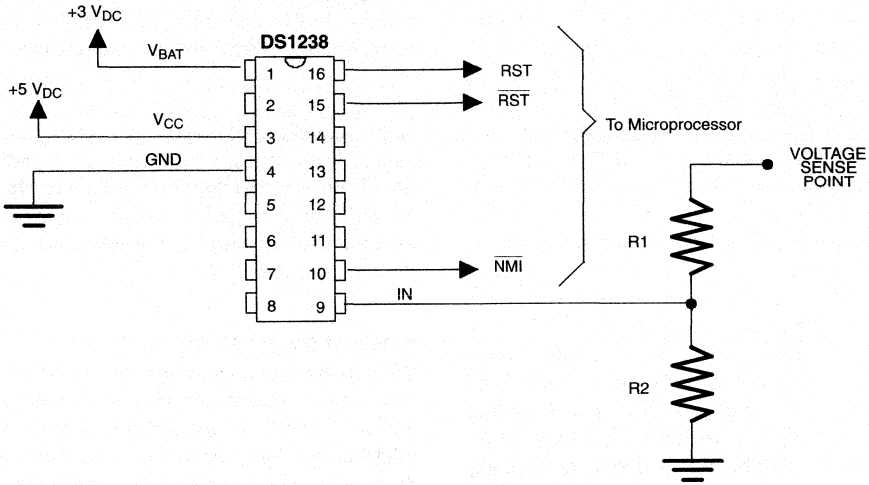
POWER MONITOR, WATCHDOG TIMER, AND PUSHBUTTON RESET Figure 3



PUSHBUTTON RESET TIMING Figure 4



NON-MASKABLE INTERRUPT Figure 5



$$V_{SENSE} = \frac{R1 + R2}{R2} \times 1.27$$

$$MAXVOLTAGE = \frac{V_{SENSE}}{1.27} \times 5.0 = VMAX$$

Example 1: 5 Volt Supply, R2 = 10K Ohms, V_{SENSE} = 4.8 Volts

$$4.8 = \frac{R1 + 10K}{10K} \times 1.27 \geq R1$$

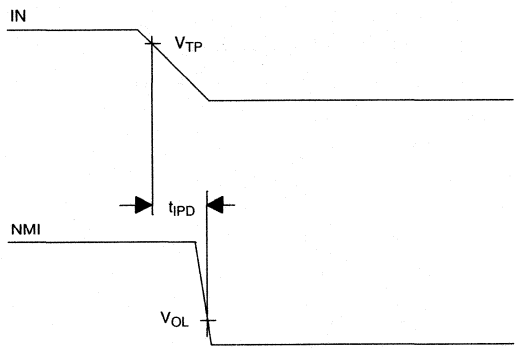
$$= 27.8K \text{ Ohm}$$

Example 2: 12 Volt Supply, R2 = 10K Ohms, V_{SENSE} = 9.0 Volts

$$9.0 = \frac{R1 + 10K}{10K} \times 1.27 \geq R1 = 60.9K \text{ Ohm}$$

$$V_{MAX} = \frac{9.00}{1.27} \times 5.0 = 35.4 \text{ Volts}$$

$\overline{NMI}$ FROM IN INPUT Figure 6



MEMORY BACKUP

The DS1238 provides all of the necessary functions required to battery back a static RAM. First, an internal switch is provided to supply SRAM power from the primary 5-volt supply (V_{CC}) or from an external battery (V_{BAT}), whichever is greater. Second, the same power fail detection described in the power monitor section is used to hold the chip enable output ($\overline{CEO}$) to within 0.3 volts of V_{CC} or to within 0.7 volts of V_{BAT}. The output voltage diode drop from V_{BAT} (0.7 V) is necessary to prevent charging of the battery in violation of UL standards. Write protection occurs as V_{CC} falls below V_{CCTP} as specified. If $\overline{CEI}$ is low at the time power fail detection occurs, $\overline{CEO}$ is held in its present state until $\overline{CEI}$ is returned high, or the period t_{CE} expires. This delay of write protection until the current memory cycle is completed prevents the corruption of data. If $\overline{CEO}$ is in an inactive state at the time of V_{CC} fail detection, $\overline{CEO}$ will be unconditionally disabled within t_{CF}. During nominal supply conditions $\overline{CEO}$ will follow $\overline{CEI}$ with a maximum propagation delay of 20 ns. Figure 7 shows a typical nonvolatile SRAM application.

FRESHNESS SEAL

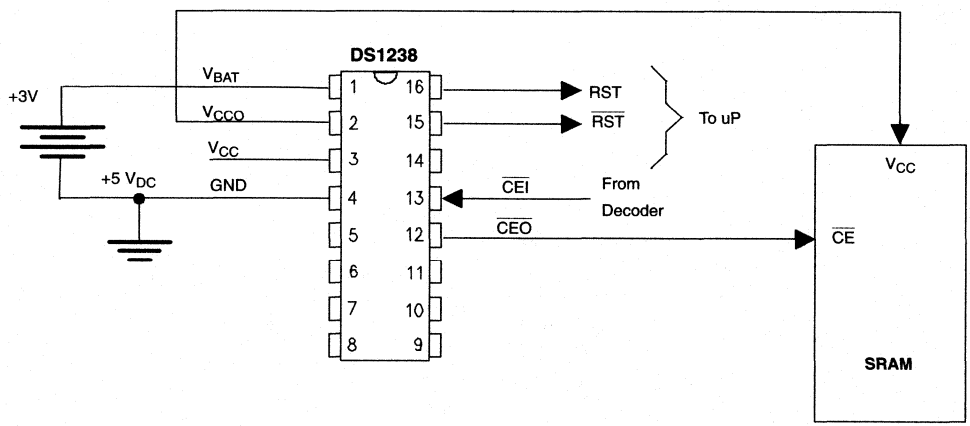
In order to conserve battery capacity during storage and/or shipment of an end system, the DS1238 provides an internal freshness seal to electrically disconnect the battery. Figure 8 depicts the three pulses below ground on the IN pin required to invoke the freshness seal. The freshness seal will result in the tri-state of outputs V_{CCO}, RST, $\overline{RST}$, and $\overline{CEO}$. The $\overline{WDS}$ output will be driven active low. The PF pin is not disabled by the freshness mode and will continue to source power from the V_{BAT} pin whenever V_{CC} is below V_{BAT}. The freshness seal will be disconnected and normal operation will begin when V_{CC} is cycled and reapplied to a level above V_{BAT}.

To prevent negative pulses associated with noise from setting the freshness mode in system applications, a series diode and resistor can be used to shunt noise to ground. During manufacturing, the freshness seal can still be set by holding TP2 at -3 volts while applying the 0 to -3-volt clock to TP1.

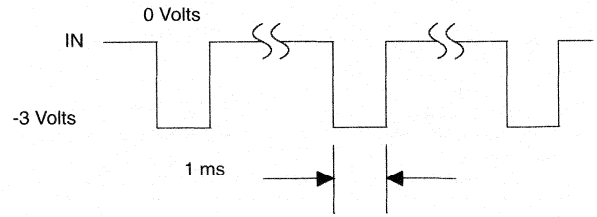
POWER SWITCHING

When larger operating currents are required in a battery-backed system, the internal switching devices of the DS1238 may be too small to support the required load through V_{CCO} with a reasonable voltage drop. For these applications, the PF output is provided to gate external power switching devices. As shown in Figure 9, power to the load is switched from V_{CC} to battery on power down, and from battery to V_{CC} on power up. The DS1336 is designed to use the PF output to switch between V_{BAT} and V_{CC}. It provides better leakage and switchover performance than currently available discrete components. The transition threshold for PF is set to the external battery voltage V_{BAT}, allowing a smooth transition between sources. Any load applied to the PF pin by an external switch will be supplied by the battery. Therefore, if a discrete switch is used, this load should be taken into consideration when sizing the battery.

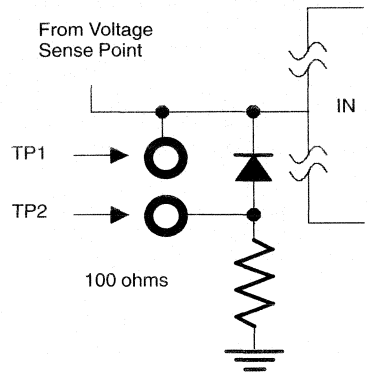
NONVOLATILE SRAM Figure 7



FRESHNESS SEAL Figure 8

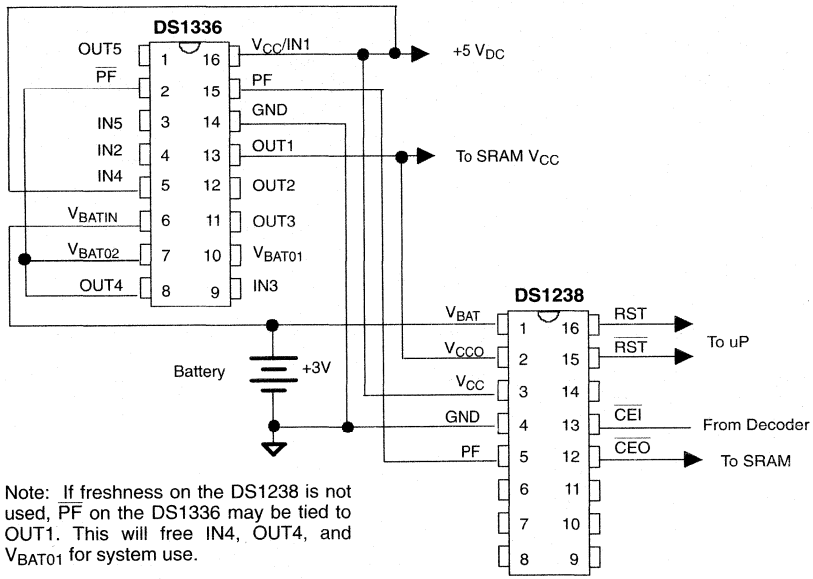


Note: This series of pulses must be applied during normal +5 volt operation.



3

POWER SWITCHING Figure 9



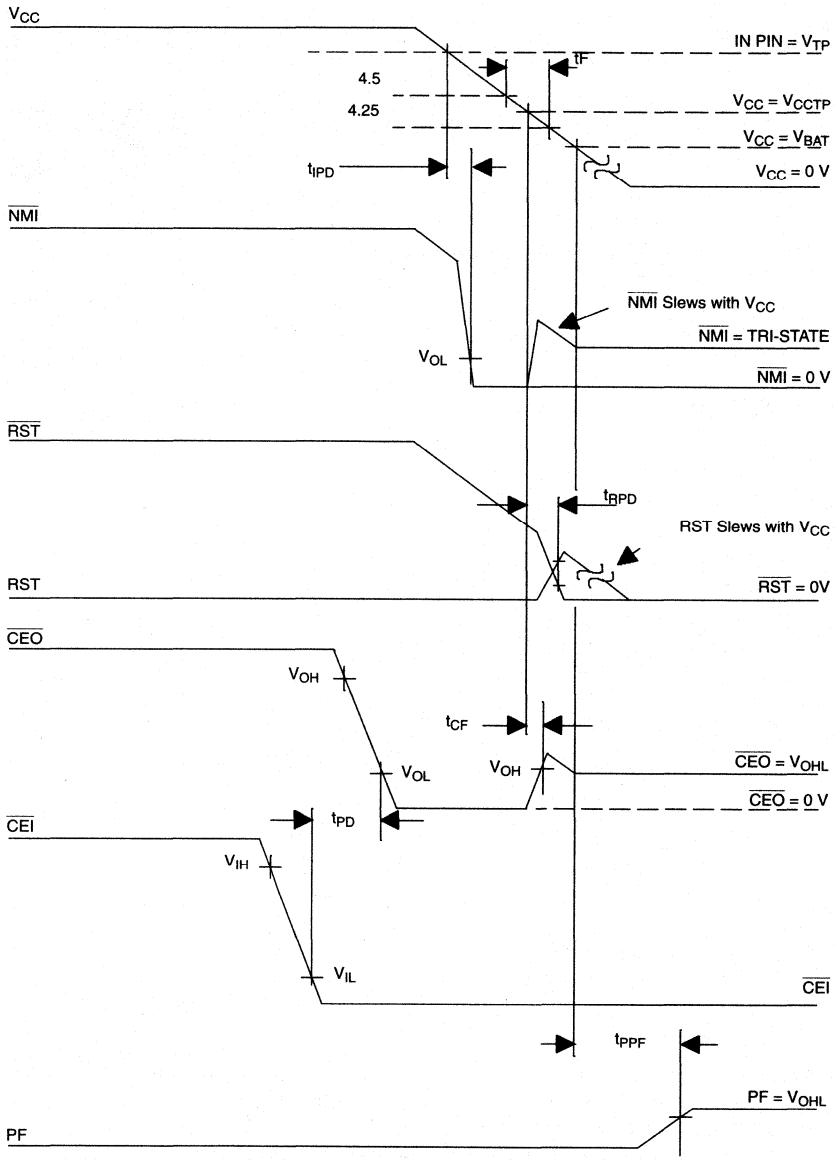
Note: If freshness on the DS1238 is not used, $\overline{PF}$ on the DS1336 may be tied to OUT1. This will free IN4, OUT4, and V_{BAT01} for system use.

TIMING DIAGRAMS

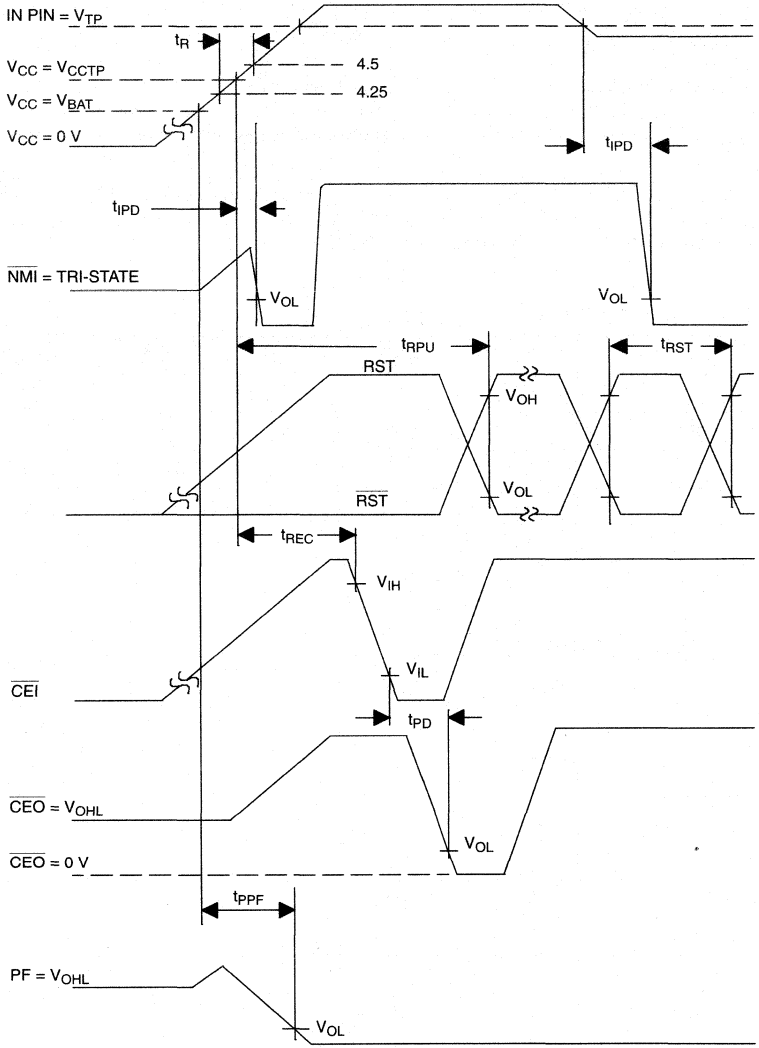
This section provides a description of the timing diagrams shown in Figure 10 and Figure 11. Figure 10 illustrates the relationship for power down. As V_{CC} falls, the IN pin voltage drops below V_{TP}. As a result, the processor is notified of an impending power failure via an active $\overline{NMI}$. This gives the processor time to save critical data in nonvolatile SRAM. As the power falls further, V_{CC} crosses V_{CCTP}, the power monitor trip point. When V_{CC} reaches V_{CCTP}, and active RST and $\overline{RST}$ are given. At this time, $\overline{CEO}$ is brought high to write protect the RAM. When the V_{CC} reaches V_{BAT}, a power fail is issued via the PF pin.

Figure 11 shows the power up sequence. As V_{CC} slews above V_{BAT}, the PF pin is deactivated. An active reset occurs as well as an $\overline{NMI}$. Although the $\overline{NMI}$ may be short due to slew rates, reset will be maintained for the standard t_{RPU} timeout period. At a later time, if the IN pin falls below V_{TP}, a new $\overline{NMI}$ will occur. If the processor does not issue an $\overline{ST}$, a watchdog reset will also occur. The second $\overline{NMI}$ and RST are provided to illustrate these possibilities.

POWER DOWN TIMING Figure 10



POWER UP TIMING Figure 11



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	–0.5V to +7.0V
Voltage on I/O Relative to Ground	–0.5V to V_{CC} + 0.5V
Voltage on IN Pin Relative to Ground	–3.5V to V_{CC} + 0.5V
Operating Temperature	0°C to 70°C
Operating Temperature (Industrial Version)	–40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Supply Voltage (5% Option)	V_{CC}	4.75	5.0	5.5	V	1
Input High Level	V_{IH}	2.0		V_{CC}+0.3	V	1
Input Low Level	V_{IL}	-0.3		+0.8	V	1
IN Input Pin	V_{IN}	0		V_{CC}	V	1
Battery Input	V_{BAT}	2.7		4.0	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}			4	mA	2
Battery Current	I_{BAT}	0		200	nA	2 , 12
Supply Output Current (V_{CCO} = V_{CC} - 0.3V)	I_{CC01}			100	mA	3
Supply Out Current (V_{CC} < V_{BAT})	I_{CC02}			1	mA	4
Supply Output Voltage	V_{CCO}	V_{CC} -0.3			V	1
Battery Back Voltage	V_{CCO}		V_{BAT} -0.8		V	6
Low Level @ RST	V_{OL}			0.4	V	1
Output Voltage @ –500 µA	V_{OH}	V_{CC}–0.5V	V_{CC}–0.1V		V	1
$\overline{CEO}$ and PF Output	V_{OHL}		V_{BAT} -0.8		V	6
Input Leakage Current	I_{LI}	-1.0		+1.0	µA	121
Output Leakage	I_{LO}	-1.0		+1.0	µA	
Output Current @0.4V	I_{OL}			4.0	mA	9
Output Current @2.4V	I_{OH}	-1.0			mA	10
Power Sup. Trip Point	V_{CCTP}	4.25	4.37	4.50	V	1
Power Supply Trip (5% Option)	V_{CCTP}	4.50	4.62	4.75	V	
IN Input Pin Current	I_{CCIN}	-1.0		+1.0	µA	
IN Input Trip Point	V_{TP}	1.15	1.27	1.35	V	1

AC ELECTRICAL CHARACTERISTIC

(0°C to 70°C; V_{CC} = 5V± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} Fall Detect to RST, $\overline{RST}$	t_{RPD}	40	100	175	µs	
V_{TP} to $\overline{NMI}$	t_{IPD}	40	100	175	µs	
RESET Active OSCSEL=high	t_{RST}	40	85	150	ms	
$\overline{ST}$ Pulse Width	t_{ST}	20			ns	13
PBRST @ V_{IL}	t_{PB}	30			ms	
V_{CC} Slew Rate 4.75 to 4.25	t_F	300			µs	
Chip Enable Prop Delay	t_{PD}			20	ns	
V_{CC} Fail to Chip Enable High	t_{CF}	7	12	144	µs	11
V_{CC} Valid to RST (RC = 1)	t_{FPU}			100	ns	
V_{CC} Valid to RST	t_{RPU}	40	100	150	ms	5
V_{CC} Slew to 4.25 to V_{BAT}	t_{FB1}	10			µs	
Chip Enable Output Recovery Time	t_{REC}	0.1			µs	7
V_{CC} Slew 4.25 to 4.75	t_R	0			µs	
Chip Enable Pulse Width	t_{CE}			5	µs	8
Watchdog Time Delay int clock Long period	t_{TD}	1.7	2.7		s	
Short period		110	170		ms	
Watchdog Time Delay, ext clock, After reset	t_{TD}		20480		clocks	
Normal			5120		clocks	
V_{BAT} Detect to PF	t_{PPF}			2	µs	
OSC IN Frequency	f_{OSC}	0		250	KHz	

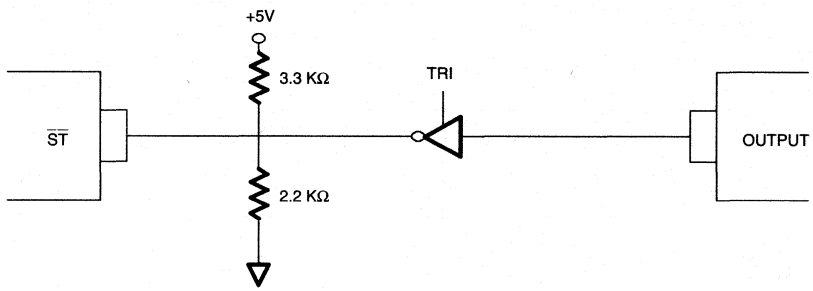
CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

NOTES:

1. All voltages referenced to ground.
2. Measured with V_{CCO}, $\overline{CEO}$, PF, $\overline{ST}$, RST, $\overline{RST}$, and $\overline{NMI}$ pin open.
3. I_{CCO1} is the maximum average load which the DS1238 can supply at V_{CC}-.3V through the V_{CCO} pin during normal 5-volt operation.
4. I_{CCO2} is the maximum average load which the DS1238 can supply through the V_{CCO} pin during data retention battery supply operation, with a maximum drop of 0.8 volts for commercial, 1.0V for industrial.
5. With t_R = 5 µs.
6. V_{CCO} is approximately V_{BAT}-0.5V at 1 µA load.
7. t_{REC} is the minimum time required before $\overline{CEI}/\overline{CEO}$ memory access is allowed.
8. t_{CE} maximum must be met to insure data integrity on power loss.
9. All outputs except RST which is 25 µA max.
10. All outputs except $\overline{RST}$, $\overline{RVT}$, and $\overline{NMI}$ which is 25 µA min.
11. The $\overline{ST}$ pin will sink ±50 µA in normal operation. The OSCIN pin will sink ±5 µA in normal operation. The OSCSEL pin will sink ±10 µA in normal operation.
12. I_{BAT} is measured with V_{BAT}=3.0V.
13. $\overline{ST}$ should be active low before the watchdog is disabled (i.e., before the $\overline{ST}$ input is tristated).



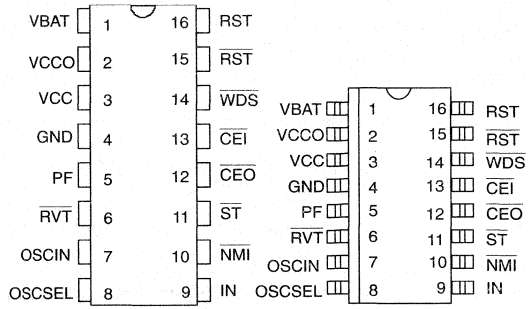
DALLAS SEMICONDUCTOR

DS1238A MicroManager

FEATURES

- Holds microprocessor in check during power transients
- Halts and restarts an out-of-control microprocessor
- Warns microprocessor of an impending power failure
- Converts CMOS SRAM into nonvolatile memory
- Unconditionally write protects memory when power supply is out of tolerance
- Delays write protection until completion of the current memory cycle
- Consumes less than 200 nA of battery current
- Controls external power switch for high current applications
- Debounces pushbutton reset
- Accurate 10% power supply monitoring
- Optional 5% power supply monitoring designated DS1238A-5
- Provides orderly shutdown in microprocessor applications
- Pin-for-pin compatible with MAX691
- Standard 16-pin DIP or space-saving 16-pin SOIC
- Optional industrial temperature range -40°C to +85°C

PIN ASSIGNMENT



16-Pin DIP (300 Mil.)
See Mech. Drawings Section

16-Pin SOIC (300 Mil.)
See Mech. Drawings Section

PIN DESCRIPTION

V_{BAT}	–	+3 Volt Battery Input
V_{CCO}	–	Switched SRAM Supply Output
V_{CC}	–	+5 Volt Power Supply Input
GND	–	Ground
PF	–	Power Fail
$\overline{RVT}$	–	Reset Voltage Threshold
OSCIN	–	Oscillator In
OSCSEL	–	Oscillator Select
IN	–	Early Warning Input
$\overline{NMI}$	–	Non–Maskable Interrupt
$\overline{ST}$	–	Strobe Input
$\overline{CEO}$	–	Chip Enable Output
$\overline{CEI}$	–	Chip Enable Input
$\overline{WDS}$	–	Watchdog Status
$\overline{RST}$	–	Reset Output (active low)
RST	–	Reset Output (active high)

DESCRIPTION

The DS1238A MicroManager provides all the necessary functions for power supply monitoring, reset control, and memory backup in microprocessor-based systems. A precise internal voltage reference and comparator circuit monitor power supply status. When an out-of-tolerance condition occurs, the microprocessor reset and power fail outputs are forced active, and static RAM control unconditionally write protects external memory. The DS1238A also provides early warning detection of a user-defined threshold by driving a nonmaskable interrupt. External reset control is provided by a pushbutton reset debounce circuit connected to the $\overline{RST}$ pin. An internal watchdog timer can also force the reset outputs to the active state if the strobe input is not driven low prior to watchdog timeout. Oscillator control pins OSCSEL and OSCIN provide either external or internal clock timing for both the reset pulse width and the watchdog timeout period. The Watchdog Status and Reset Voltage Threshold are provided via $\overline{WDS}$ and $\overline{RVT}$, respectively. A block diagram of the DS1238A is shown in Figure 1.

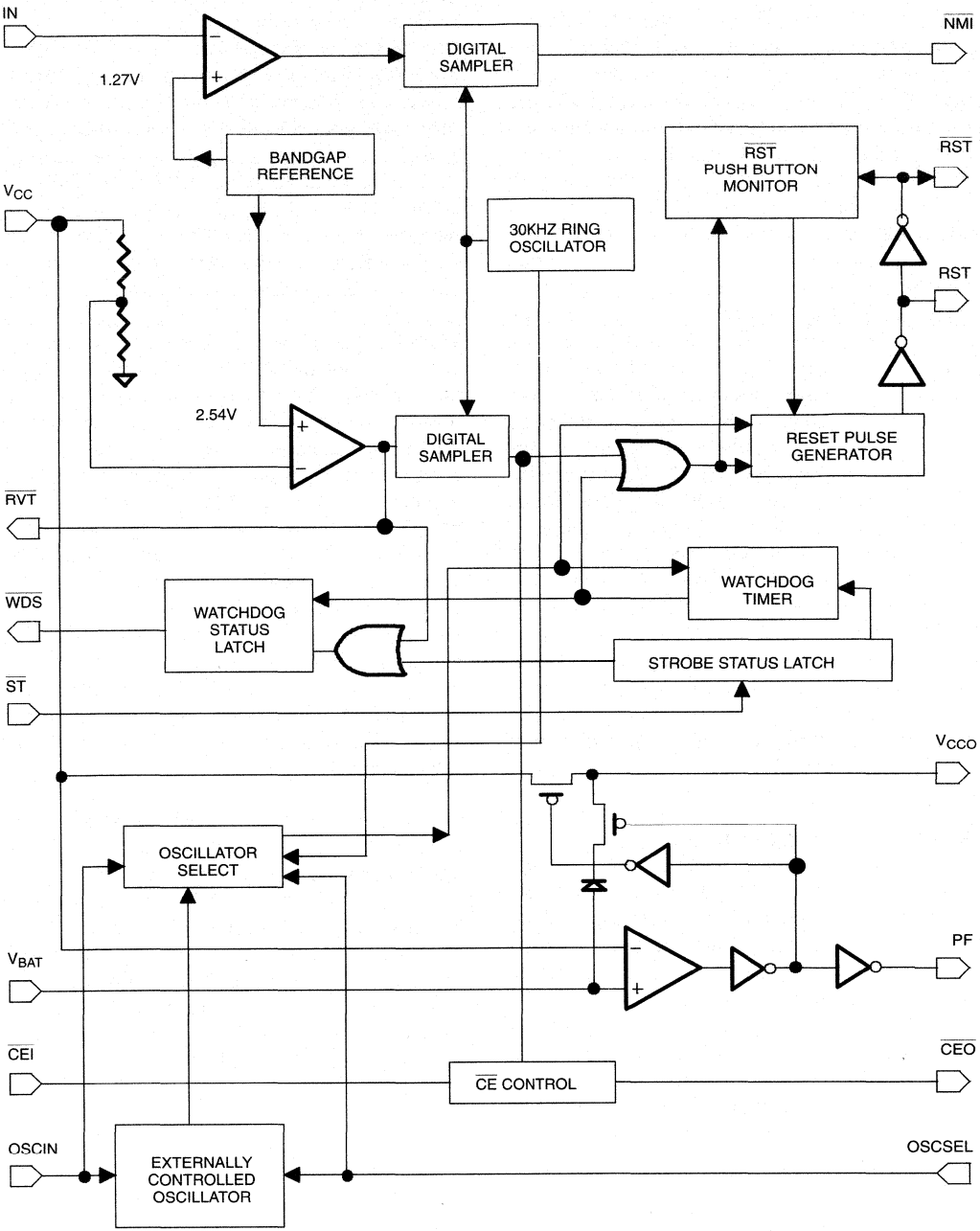
PIN DESCRIPTION

PIN NAME	DESCRIPTION
V_{BAT}	+3V Battery Input provides nonvolatile operation of control functions.
V_{CCO}	V_{CC} output for nonvolatile SRAM applications.
V_{CC}	+5V primary power input.
GND	System ground.
PF	Power fail indicator, active high, used for external power switching as shown in Figure 9.
$\overline{RVT}$	Reset Voltage Threshold. Indicates that V_{CC} is below the reset voltage threshold.
OSCIN	Oscillator input or timing capacitor. See Table 1.
OSCSEL	Oscillator Select. Selects internal or external clock functions. See Table 1.
IN	Early warning power fail input. This voltage sense point may be tied (via resistor divider) to a user-selected voltage.
$\overline{NMI}$	Non-maskable interrupt. Output used in conjunction with the IN pin to indicate an impending power failure.
$\overline{ST}$	Strobe input. A high–to–low transition will reset the watchdog timer, indicating that software is still in control.
$\overline{CEO}$	Chip enable output. Write protected. Used with nonvolatile SRAM applications.
$\overline{CEI}$	Chip enable input.
$\overline{WDS}$	Watchdog Status. Indicates that a watchdog timeout has occurred.
$\overline{RST}$	Active low reset output.
RST	Active high reset output.

POWER MONITOR

The DS1238A employs a band gap voltage reference and a precision comparator to monitor the 5–volt supply (V_{CC}) in microprocessor-based systems. When an out-of-tolerance condition occurs, the $\overline{RVT}$, RST, and $\overline{RST}$ outputs are driven to the active state. The V_{CC} trip point (V_{CCTP}) is set for 10% operation so that the $\overline{RVT}$, RST and $\overline{RST}$ outputs will become active as V_{CC} falls below 4.5 volts (4.37 typical). The V_{CCTP} for the 5% operation option (DS1238A-5) is set for 4.75 volts (4.62 typical). The RST and $\overline{RST}$ signals are excellent for microprocessor reset control, as processing is stopped at the last possible moment of in-tolerance V_{CC}. On power up, $\overline{RVT}$ will become inactive as soon as V_{CC} rises above V_{CCTP}. However, the RST and $\overline{RST}$ signals remain active for a minimum of 50 ms (100 ms typical) after V_{CCTP} is reached to allow the power supply and microprocessor to stabilize.

DS1238A FUNCTIONAL BLOCK DIAGRAM Figure 1



3

WATCHDOG TIMER

The DS1238A provides a watchdog timer function which forces the $\overline{WDS}$, RST, and $\overline{RST}$ signals to the active state when the strobe input ($\overline{ST}$) is not stimulated for a predetermined time period. This time period is described below in Table 1. The watchdog timeout period begins as soon as RST and $\overline{RST}$ are inactive. If a high-to-low transition occurs at the $\overline{ST}$ input prior to time out, the watchdog timer is reset and begins to time out again. The $\overline{ST}$ input timing is shown in Figure 2. In order to guarantee that the watchdog timer does not timeout, a high-to-low transition on $\overline{ST}$ must occur at or less than the minimum timeout of the watchdog as described in the AC Electrical Characteristics. If the watchdog timer is allowed to time out, the $\overline{WDS}$, RST, and $\overline{RST}$ outputs are driven to the active state. $\overline{WDS}$ is a latched signal which indicates the watchdog status, and is activated as soon as the watchdog timer completes a full period as outlined in Table 1. The $\overline{WDS}$ pin will remain low until one of three operations occurs. The first is to strobe the $\overline{ST}$ pin with a falling edge, which will both set the $\overline{WDS}$ as well as the watchdog timer count. The second is to leave the $\overline{ST}$ pin open, which disables the watchdog. Lastly, the $\overline{WDS}$ pin is active low whenever V_{CC} falls below V_{CCTP} and activates the $\overline{RVT}$ signal. The $\overline{ST}$ input can be derived from microprocessor address, data, or control signals, as well as microcontroller port pins. Under normal operating conditions, these signals would routinely reset the watchdog timer prior to time out. The watchdog is disabled by leaving the $\overline{ST}$ input open, or as soon as V_{CC} falls to V_{CCTP}.

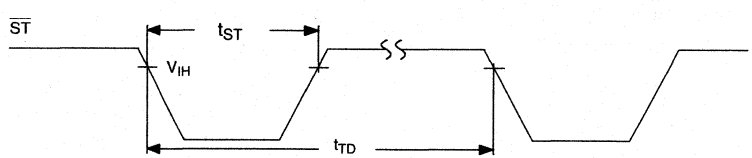
NON–MASKABLE INTERRUPT

The DS1238A generates a non-maskable interrupt ($\overline{NMI}$) for early warning of a power failure to the microprocessor. A precision comparator monitors the voltage level at the IN pin relative to an on-chip reference generated by an internal band gap. The IN pin is a high impedance input allowing for a user-defined sense point. An external resistor voltage divider network (Figure 5) is used to interface with high voltage signals. This sense point may be derived from the regulated 5-volt supply, or from a higher DC voltage level closer to the main system power input. Since the IN trip point V_{TP} is 1.27 volts, the proper values for R1 and R2 can be determined by the equation as shown in Figure 5. Proper operation of the DS1238A requires that the voltage at the IN pin be limited to V_{IH}. Therefore, the maximum allowable voltage at the supply being monitored (V_{MAX}) can also be derived as shown in Figure 5. A simple approach to solving this equation is to select a value for R2 of high enough value to keep power consumption low, and solve for R1. The flexibility of the IN input pin allows for detection of power loss at the earliest point in a power supply system, maximizing the amount of time for microprocessor shut-down between $\overline{NMI}$ and RST or $\overline{RST}$.

When the supply being monitored decays to the voltage sense point, the DS1238A will force the $\overline{NMI}$ output to an active state. Noise is removed from the $\overline{NMI}$ power fail detection circuitry using built-in time domain hysteresis. That is, the monitored supply is sampled periodically at a rate determined by an internal ring oscillator running at approximately 30 KHz (33 µs/cycle). Three consecutive samplings of out-of-tolerance supply (below V_{SENSE}) must occur at the IN pin to active $\overline{NMI}$. Therefore, the supply must be below the voltage sense point for approximately 100 µs or the comparator will reset. In this way, power supply noise is removed from the monitoring function preventing false trips. During a power–up, any IN pin levels below V_{TP} detected by the comparator are disabled from reaching the $\overline{NMI}$ pin until V_{CC} rises to V_{CCTP}. As a result, any potential active $\overline{NMI}$ will not be initiated until V_{CC} reaches V_{CCTP}.

Removal of an active low level on the $\overline{NMI}$ pin is controlled by the subsequent rise of the IN pin above V_{TP}. The initiation and removal of the $\overline{NMI}$ signal during power up depends on the relative voltage relationship between V_{CC} and the IN pin voltage. Note that a fast slewing power supply may cause the $\overline{NMI}$ to be virtually non-existent on power up. This is of no consequence however, since an RST will be active. The $\overline{NMI}$ voltage will follow V_{CC} down until V_{CC} decays to V_{BAT}. Once V_{CC} decays to $\overline{VBAT}$, the $\overline{NMI}$ pin will enter a tri-state mode.

$\overline{ST}$ INPUT TIMING Figure 2



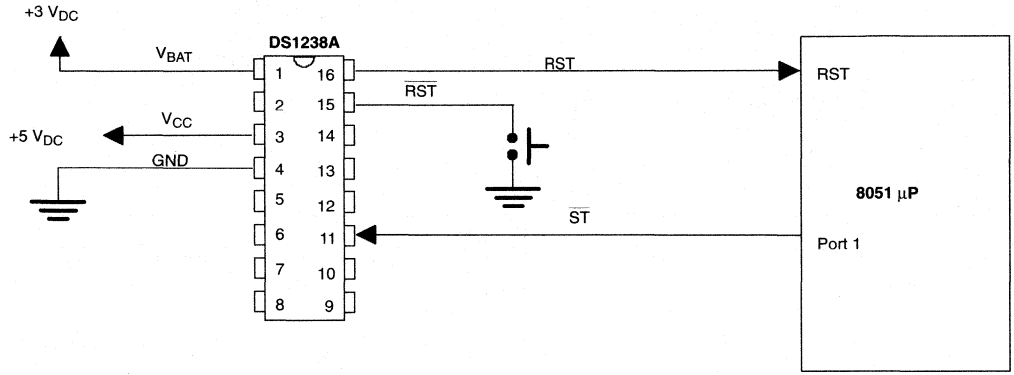
OSCILLATOR CONTROLS Table 1

	OSCIN	OSCSEL	Watchdog Timeout Period (typ)		
			First Period Following a Reset	Other Timeout	Reset Active Duration
External	Ext Clk	Low	20480 Clks	5120 Clocks	641 Clks
	Ext Cap	Low	$\cong \frac{2.2\ \text{sec}}{47\ \text{pf}} \times \text{Cpf}$	$\cong \frac{550\ \text{ms}}{47\ \text{pf}} \times \text{Cpf}$	$\cong \frac{69\ \text{ms}}{47\ \text{pf}} \times \text{Cpf}$
Internal	Low	Hi/Open	2.7 sec	170 ms	85 ms
	Hi/Open	Hi/Open	2.7 sec	2.7 sec	85 ms

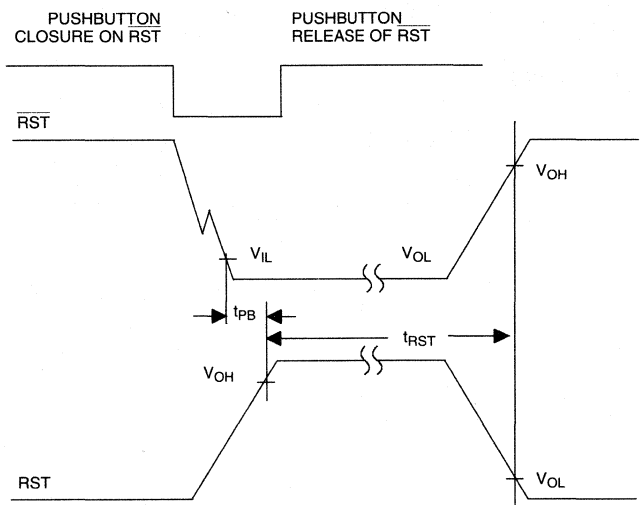
Note that the OSCIN and OSCSEL pins are tri-stated when V_{CC} is below V_{BAT}.

3

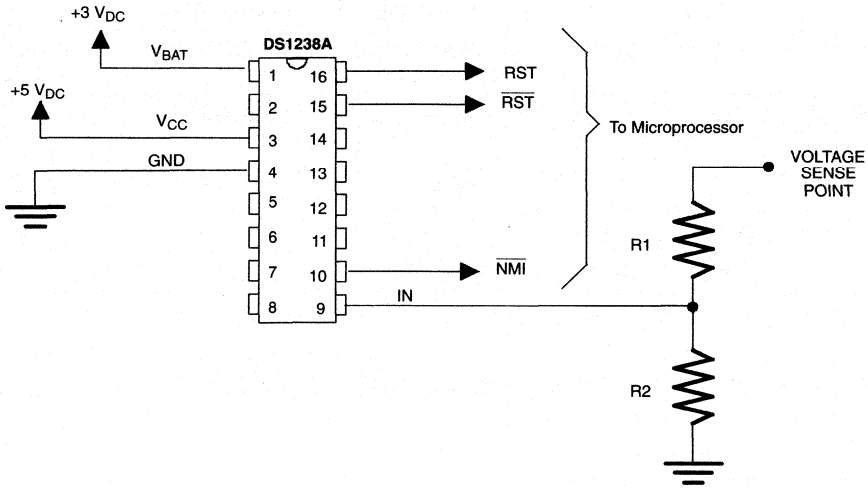
POWER MONITOR, WATCHDOG TIMER, AND PUSHBUTTON RESET Figure 3



PUSHBUTTON RESET TIMING Figure 4



NON-MASKABLE INTERRUPT Figure 5



$$V_{SENSE} = \frac{R1 + R2}{R2} \times 1.27$$

$$MAXVOLTAGE = \frac{V_{SENSE}}{1.27} \times 5.0 = VMAX$$

Example 1: 5 Volt Supply, R2 = 10K Ohms, V_{SENSE} = 4.8 Volts

$$4.8 = \frac{R1 + 10K}{10K} \times 1.27 \geq R1$$

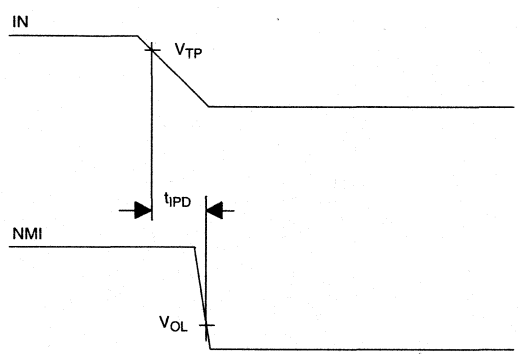
$$= 27.8K \text{ Ohm}$$

Example 2: 12 Volt Supply, R2 = 10K Ohms, V_{SENSE} = 9.0 Volts

$$9.0 = \frac{R1 + 10K}{10K} \times 1.27 \geq R1 = 60.9K \text{ Ohm}$$

$$V_{MAX} = \frac{9.00}{1.27} \times 5.0 = 35.4 \text{ Volts}$$

$\overline{NMI}$ FROM IN INPUT Figure 6



MEMORY BACKUP

The DS1238A provides all of the necessary functions required to battery back a static RAM. First, an internal switch is provided to supply SRAM power from the primary 5-volt supply (V_{CC}) or from an external battery (V_{BAT}), whichever is greater. Second, the same power fail detection described in the power monitor section is used to hold the chip enable output ($\overline{CEO}$) to within 0.3 volts of V_{CC} or to within 0.7 volts of V_{BAT}. The output voltage diode drop from V_{BAT} (0.7V) is necessary to prevent charging of the battery in violation of UL standards. Write protection occurs as V_{CC} falls below V_{CCTP} as specified. If $\overline{CEI}$ is low at the time power fail detection occurs, $\overline{CEO}$ is held in its present state until $\overline{CEI}$ is returned high, or the period t_{CE} expires. This delay of write protection until the current memory cycle is completed prevents the corruption of data. If $\overline{CEO}$ is in an inactive state at the time of V_{CC} fail detection, $\overline{CEO}$ will be unconditionally disabled within t_{CF}. During nominal supply conditions $\overline{CEO}$ will follow $\overline{CEI}$ with a maximum propagation delay of 20 ns. Figure 7 shows a typical nonvolatile SRAM application.

FRESHNESS SEAL

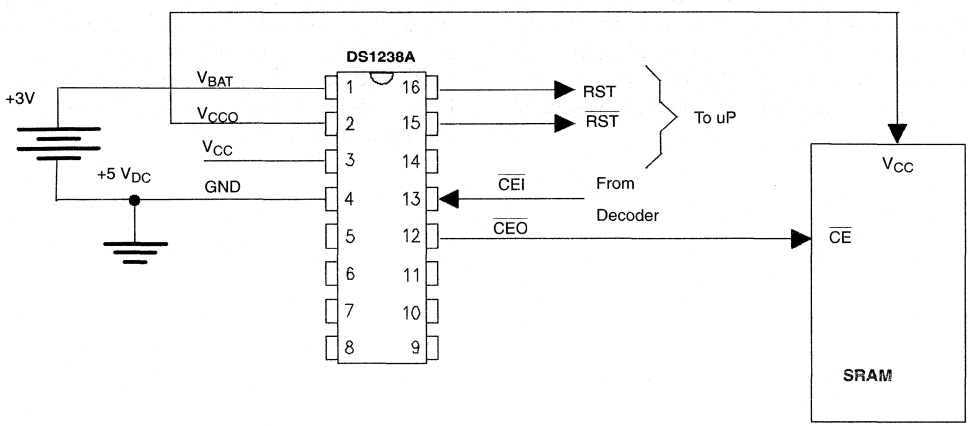
In order to conserve battery capacity during initial construction of an end system, the DS1238A provides a freshness seal that electrically disconnects the battery. This means that upon battery attach, the V_{CCO} output will remain inactive until V_{CC} is applied. This prevents V_{CCO} from powering other devices when the battery is first attached, and V_{CC} is not present. Once V_{CC} is applied, the freshness seal is broken and cannot be invoked again without subsequent removal and re–attachment of the battery.

POWER SWITCHING

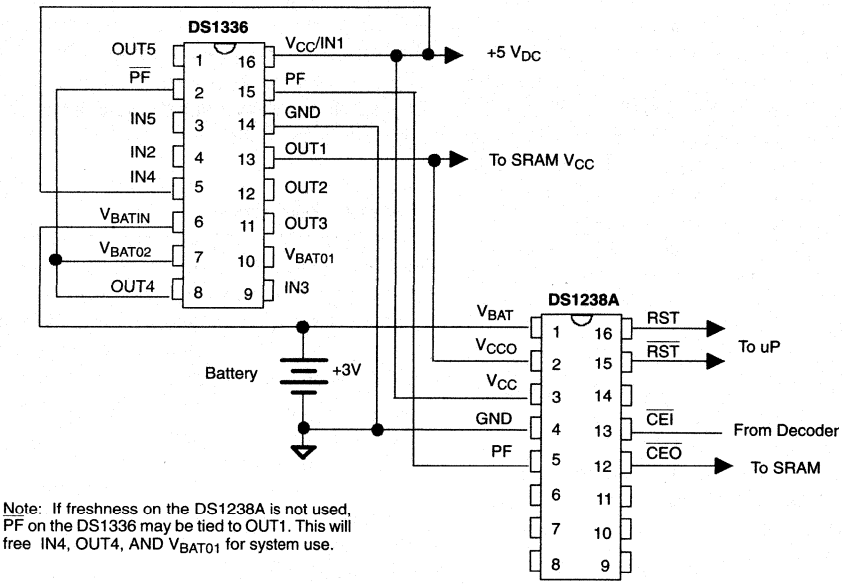
When larger operating currents are required in a battery-backed system, the internal switching devices of the DS1238A may be too small to support the required load through V_{CCO} with a reasonable voltage drop. For these applications, the PF output is provided to gate external power switching devices. As shown in Figure 8, power to the load is switched from V_{CC} to battery on power down, and from battery to V_{CC} on power up. The DS1336 is designed to use the PF output to switch between V_{BAT} and V_{CC}. It provides better leakage and switchover performance than currently available discrete components. The transition threshold for PF is set to the external battery voltage V_{BAT}, allowing a smooth transition between sources. Any load applied to the PF pin by an external switch will be supplied by the battery. Therefore, if a discrete switch is used, this load should be taken into consideration when sizing the battery.

3

NONVOLATILE SRAM Figure 7



POWER SWITCHING Figure 8



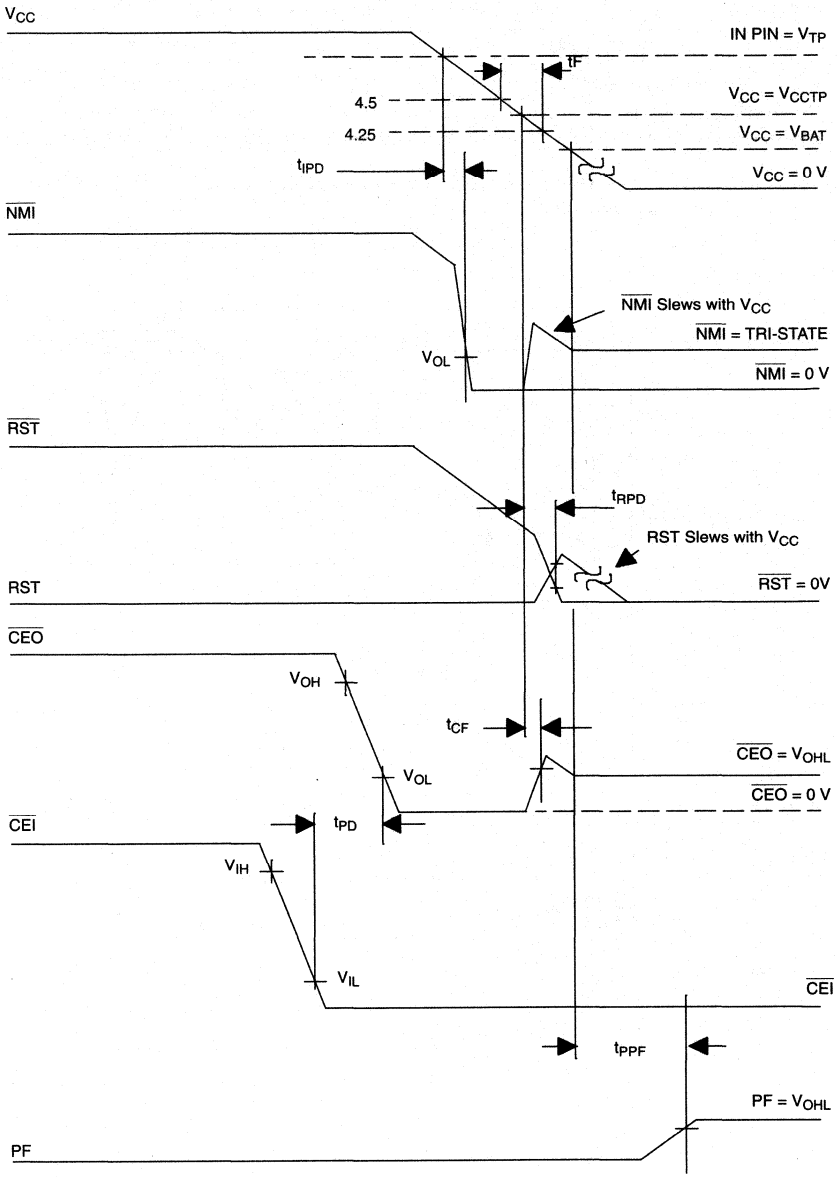
Note: If freshness on the DS1238A is not used, PF on the DS1336 may be tied to OUT1. This will free IN4, OUT4, AND V_{BAT01} for system use.

TIMING DIAGRAMS

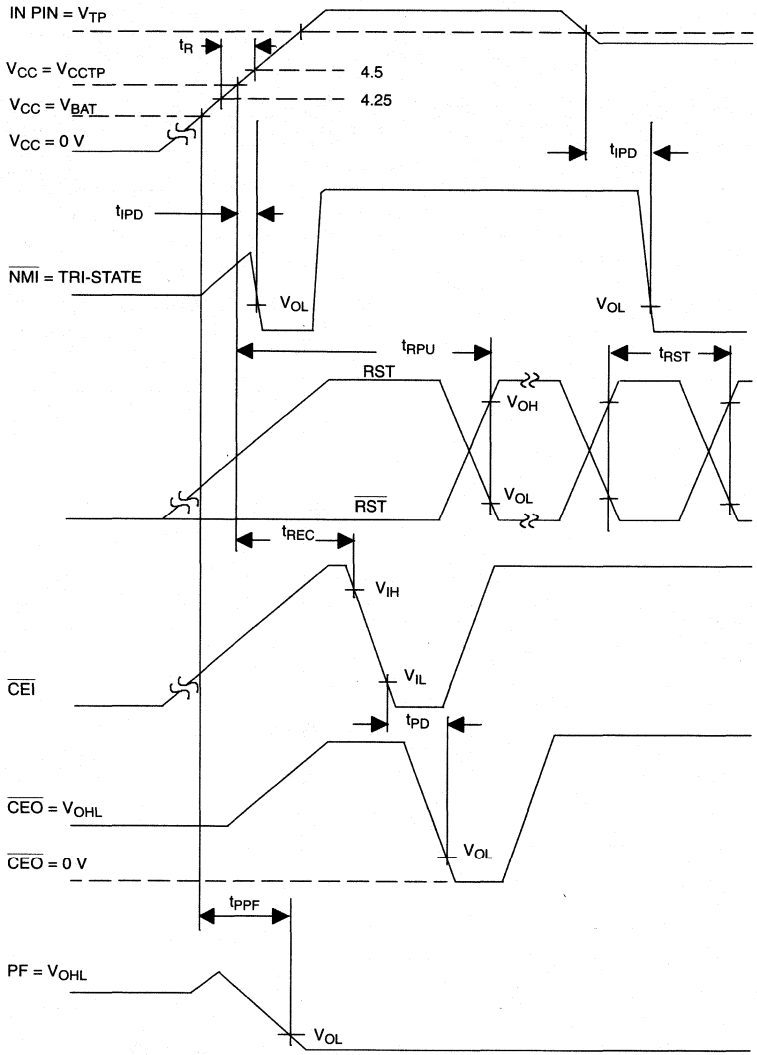
This section provides a description of the timing diagrams shown in Figure 9 and Figure 10. Figure 9 illustrates the relationship for power down. As V_{CC} falls, the IN pin voltage drops below V_{TP}. As a result, the processor is notified of an impending power failure via an active $\overline{NMI}$. This gives the processor time to save critical data in nonvolatile SRAM. As the power falls further, V_{CC} crosses V_{CCTP}, the power monitor trip point. When V_{CC} reaches V_{CCTP}, and active RST and $\overline{RST}$ are given. At this time, $\overline{CEO}$ is brought high to write protect the RAM. When the V_{CC} reaches V_{BAT}, a power fail is issued via the PF pin.

Figure 10 shows the power up sequence. As V_{CC} slews above V_{BAT}, the PF pin is deactivated. An active reset occurs as well as an $\overline{NMI}$. Although the $\overline{NMI}$ may be short due to slew rates, reset will be maintained for the standard t_{RPU} timeout period. At a later time, if the IN pin falls below V_{TP}, a new $\overline{NMI}$ will occur. If the processor does not issue an $\overline{ST}$, a watchdog reset will also occur. The second $\overline{NMI}$ and RST are provided to illustrate these possibilities.

POWER DOWN TIMING Figure 9



POWER UP TIMING Figure 10



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	–0.5V to +7.0V
Voltage on I/O Relative to Ground	–0.5V to V_{CC} + 0.5V
Operating Temperature	0°C to 70°C
Operating Temperature (Industrial Version)	–40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Supply Voltage (5% Option)	V_{CC}	4.75	5.0	5.5	V	1
Input High Level	V_{IH}	2.0		V_{CC}+0.3	V	1
Input Low Level	V_{IL}	-0.3		+0.8	V	1
IN Input Pin	V_{IN}	0		V_{CC}	V	1
Battery Input	V_{BAT}	0		4.0	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}			4	mA	2
Battery Current	I_{BAT}	0		200	nA	2, 12
Supply Output Current (V_{CCO} = V_{CC} - 0.3V)	I_{CC01}			100	mA	3
Supply Out Current (V_{CC} < V_{BAT})	I_{CC02}			1	mA	4
Supply Output Voltage	V_{CCO}	V_{CC} -0.3			V	1
Battery Back Voltage	V_{CCO}		V_{BAT} -0.8		V	6
Low Level @ RST	V_{OL}			0.4	V	1
Output Voltage @ –500 µA	V_{OH}	V_{CC}–0.5V	V_{CC}–0.1V		V	1
$\overline{CEO}$ and PF Output	V_{OHL}		V_{BAT} -0.8		V	6
Input Leakage Current	I_{LI}	-1.0		+1.0	µA	2
Output Leakage	I_{LO}	-1.0		+1.0	µA	11
Output Current @0.4V	I_{OL}			4.0	mA	9
Output Current @2.4V	I_{OH}	-1.0			mA	10
Power Sup. Trip Point	V_{CCTP}	4.25	4.37	4.50	V	1
Power Supply Trip (5% Option)	V_{CCTP}	4.50	4.62	4.75	V	
IN Input Pin Current	I_{CCIN}	-1.0		+1.0	µA	
IN Input Trip Point	V_{TP}	1.15	1.27	1.35	V	1

AC ELECTRICAL CHARACTERISTIC

(0°C to 70°C; V_{CC} = 5V± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} Fall Detect to RST, $\overline{RST}$	t_{RPD}	40	100	175	µs	
V_{TP} to $\overline{NMI}$	t_{IPD}	40	100	175	µs	
RESET Active OSCSEL=high	t_{RST}	40	85	150	ms	
$\overline{ST}$ Pulse Width	t_{ST}	20			ns	13
PBRST @ V_{IL}	t_{PB}	30			ms	
V_{CC} Slew Rate 4.75 to 4.25	t_F	300			µs	
Chip Enable Prop Delay	t_{PD}			20	ns	
V_{CC} Fail to Chip Enable High	t_{CF}	7	12	144	µs	11
V_{CC} Valid to RST (RC = 1)	t_{FPU}			100	ns	
V_{CC} Valid to RST	t_{RPU}	40	100	150	ms	5
V_{CC} Slew to 4.25 to V_{BAT}	t_{FB1}	10			µs	
Chip Enable Output Recovery Time	t_{REC}	0.1			µs	7
V_{CC} Slew 4.25 to 4.75	t_R	0			µs	
Chip Enable Pulse Width	t_{CE}			5	µs	8
Watchdog Time Delay int clock Long period	t_{TD}	1.7	2.7		s	
Short period		110	170		ms	
Watchdog Time Delay, ext clock, After reset	t_{TD}		20480		clocks	
Normal			5120		clocks	
V_{BAT} Detect to PF	t_{PPF}			2	µs	
OSC IN Frequency	f_{OSC}	0		250	KHz	

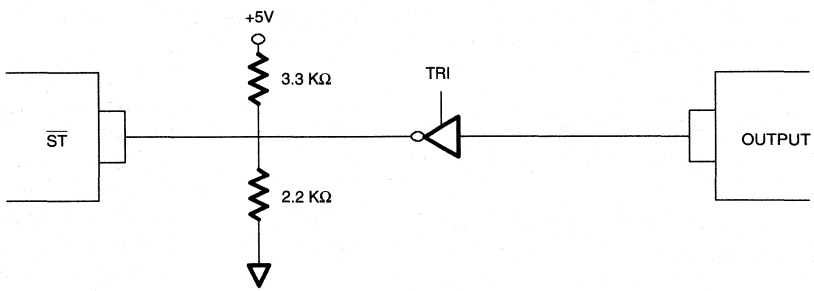
CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

NOTES:

1. All voltages referenced to ground.
2. Measured with V_{CCO}, $\overline{CEO}$, PF, $\overline{ST}$, RST, $\overline{RST}$, and $\overline{NMI}$ pin open.
3. I_{CCO1} is the maximum average load which the DS1238A can supply at V_{CC}-.3V through the V_{CCO} pin during normal 5-volt operation.
4. I_{CCO2} is the maximum average load which the DS1238A can supply through the V_{CCO} pin during data retention battery supply operation, with a maximum drop of 0.8 volts for commercial, 1.0V for industrial.
5. With t_R = 5 µs.
6. V_{CCO} is approximately V_{BAT}-0.5V at 1 µA load.
7. t_{REC} is the minimum time required before $\overline{CEI}/\overline{CEO}$ memory access is allowed.
8. t_{CE} maximum must be met to insure data integrity on power loss.
9. All outputs except RST which is 25 µA max.
10. All outputs except $\overline{RST}$, $\overline{RTV}$, and $\overline{NMI}$ which is 25 µA min.
11. The $\overline{ST}$ pin will sink ±50 µA in normal operation. The OSCIN pin will sink ±5 µA in normal operation. The OSCSEL pin will sink ±10 µA in normal operation.
12. I_{BAT} is measured with V_{BAT}=3.0V.
13. $\overline{ST}$ should be active low before the watchdog is disabled (i.e., before the $\overline{ST}$ input is tristated).



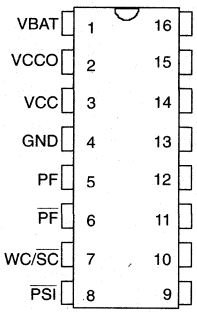
DALLAS SEMICONDUCTOR

DS1239
MicroManager Chip

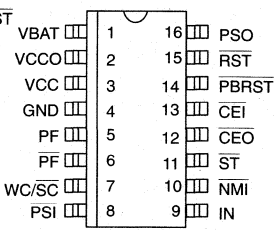
FEATURES

- Provides necessary control for start up and shutdown of power supply from keyboard
- Holds microprocessor in check during power transients
- Halts and restarts an out-of-control microprocessor
- Monitors push button for external override
- Warns microprocessor of an impending power failure
- Converts CMOS SRAM into nonvolatile memory
- Unconditionally write-protects memory when power supply is out of tolerance
- Consumes less than 100 nA of battery current
- Controls external power switch for high current applications
- Accurate 10% power supply monitoring
- Optional 5% power supply monitoring designated DS1239-5
- Provides orderly shutdown in nonvolatile microprocessor applications
- Supplies necessary control for low-power "stop mode" in battery operate hand-held applications
- Standard 16-pin DIP or space-saving 16-pin SOIC
- Optional industrial temperature range -40°C to +85°C

PIN ASSIGNMENT



DS1239 16-Pin DIP
(300 Mil)
See Mech Drawings Section



DS1239 16-Pin SOIC
(300 Mil)
See Mech. Drawings Section

PIN DESCRIPTION

V_{BAT}	–	+3 Volt Battery Input
V_{CCO}	–	Switched SRAM Supply Output
V_{CC}	–	+5 Volt Power Supply Input
GND	–	Ground
PF	–	Power Fail (Active High)
$\overline{PF}$	–	Power Fail (Active Low)
WC/$\overline{SC}$	–	Wake-Up Control (Sleep)
$\overline{PSI}$	–	Power Supply Control Input
IN	–	Early Warning Input
$\overline{NMI}$	–	Non-Maskable Interrupt
$\overline{ST}$	–	Strobe Input
$\overline{CEO}$	–	Chip Enable Output
$\overline{CEI}$	–	Chip Enable Input
$\overline{PBRST}$	–	Pushbutton Reset Input
$\overline{RST}$	–	Reset Output (Active low)
PSO	–	Power Supply Control Outputs

DESCRIPTION

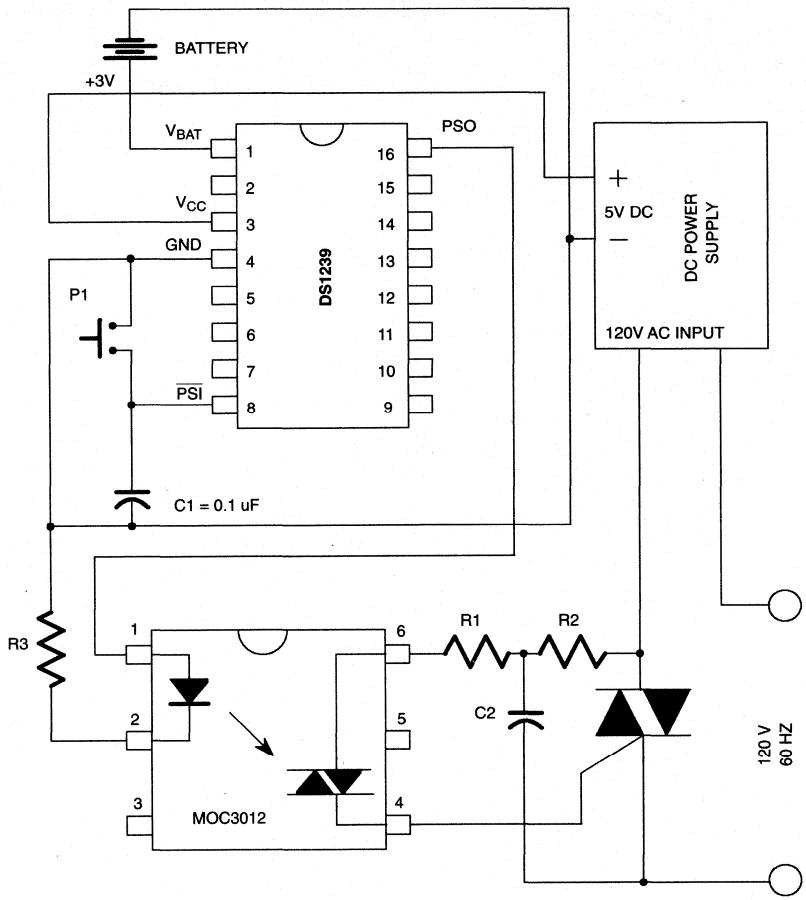
The DS1239 MicroManager provides all the necessary functions for power supply control and monitoring, reset control, and memory backup in microprocessor-based systems. Using the DS1239, an AC power switch is no longer required for microprocessor-based systems. A keyboard control system for power supply start up and shutdown is provided through the use of the Power Supply Control Input and Output. In other respects, the DS1239 is functionally identical to a DS1236 in the NMOS mode. For a complete description of the other DS1239 features, refer to the DS1236 data sheet. Pin-out of the DS1239 is identical to the DS1236 with two exceptions. The RC and RST pins have been replaced with $\overline{PSI}$ and PSO, respectively. Other pins and functions operate exactly as the DS1236 in NMOS mode.

POWER SUPPLY CONTROL

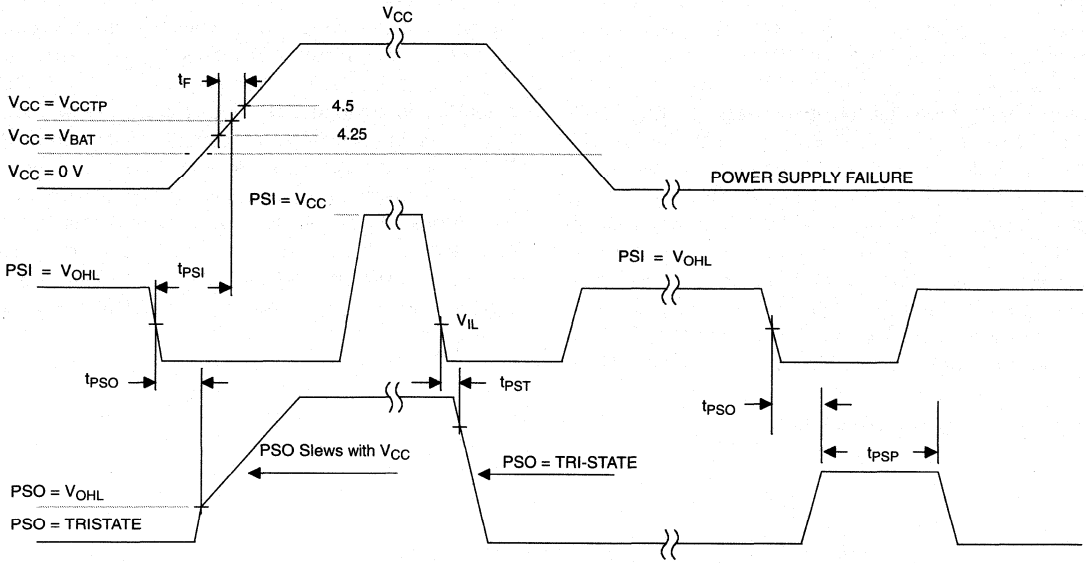
The DS1239 facilitates the power-up and power down sequencing of a main power supply from a keyboard or pushbutton. The Power Supply Control Input ($\overline{PSI}$) and Power Supply Control Output (PSO) are used for this purpose. Prior to establishing a voltage on V_{CC} (+5V), the $\overline{PSI}$ is internally held at a high level at all times with the V_{BAT} supply. When $\overline{PSI}$ is forced low via a key pad or other source, the PSO is connected to the V_{BAT} to provide a high level. As shown in Figure 1, this active high signal can be wired directly to an optically isolated SCR to initiate an AC to DC power-up sequence. This in turn will provide the supply voltage for V_{CC}. The timing is illustrated in Figure 2. Holding the $\overline{PSI}$ input low, the PSO output will supply a connection to the V_{BAT} pin until the V_{CC} reaches V_{BAT}, or a maximum of 500 ms. If the supply voltage on V_{CC} rises above the V_{BAT} level before the t_{PSI} time-out, the PSO pin will remain high and track the V_{CC} input. If V_{CC} does not rise above V_{BAT} before either t_{PSI} or $\overline{PSI}$ is allowed to return to a high level, the PSO output will return to tristate. Once the PSO output and V_{CC} are set at a high level, a subsequent falling edge on $\overline{PSI}$ will tristate PSO to initiate a shut down condition. The 10 microamp current supplied by the $\overline{PSI}$ pin allows the use of a 0.1 µF capacitor as a simple pushbutton debounce circuit. The battery size for this application must be selected to provide the SCR on-current for the power supply response time and is consequently application-specific.

3

POWER SUPPLY CONTROL Figure 1



POWER SUPPLY CONTROL TIMING Figure 2



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	–0.5V to +7.0V
Voltage on I/O Relative to Ground	–0.5V to V_{CC} + 0.5V
Operating Temperature	0°C to 70°C
Operating Temperature (Industrial Version)	–40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

These specifications reflect the power supply control feature of the DS1239. For complete electrical specifications, refer to the DS1236 data sheet.

3

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{PSI}$ Output Current	I_{PSI}		3		µA	
PSO Output Current	I_{PSO}	10			mA	3

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{PSI}$ to Valid V_{CC}	t_{PSI}			200	ms	1
$\overline{PSI}$ to PSO Tri-state	t_{PST}			20	ns	
$\overline{PSI}$ to Valid PSO	t_{PSO}			100	ns	
PSO Pulse Width	t_{PSP}		200	500	ms	2

NOTES:

1. Minimum turn-on response time for AC-to-DC power supply.
2. PSO pulse width for V_{CC} held below V_{BAT}.
3. PSO will typically source 1.5 mA at 1.5V with V_{CC} = 0V, V_{BAT} = 3V.

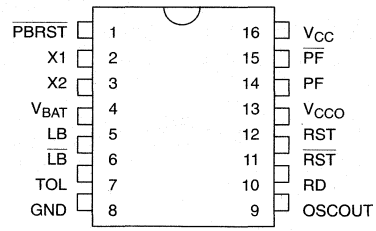
DALLAS SEMICONDUCTOR

DS1632
PC Power Fail and Reset Controller

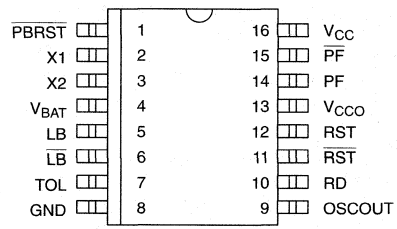
FEATURES

- Power fail detector for personal computers and workstations
- Connects directly to popular personal computer chip sets
- On chip 32.768 KHz oscillator for real time clock
- Provides battery backup power to clock chip
- Pushbutton reset input
- Accurate 5% or 10% +5 volt power supply monitoring
- Complementary outputs for reset, power fail, and low battery
- Provides for reset pulse width of either 95 ms or 190 ms
- Eliminates the need for discrete components
- Low–power CMOS circuitry
- 16-pin DIP or SOIC surface mount package
- 0°C to 70°C operation

PIN ASSIGNMENT



16-Pin DIP (300 Mil)
See Mech. Drawings Section



16-Pin SOIC (300 Mil)
See Mech. Drawings Section

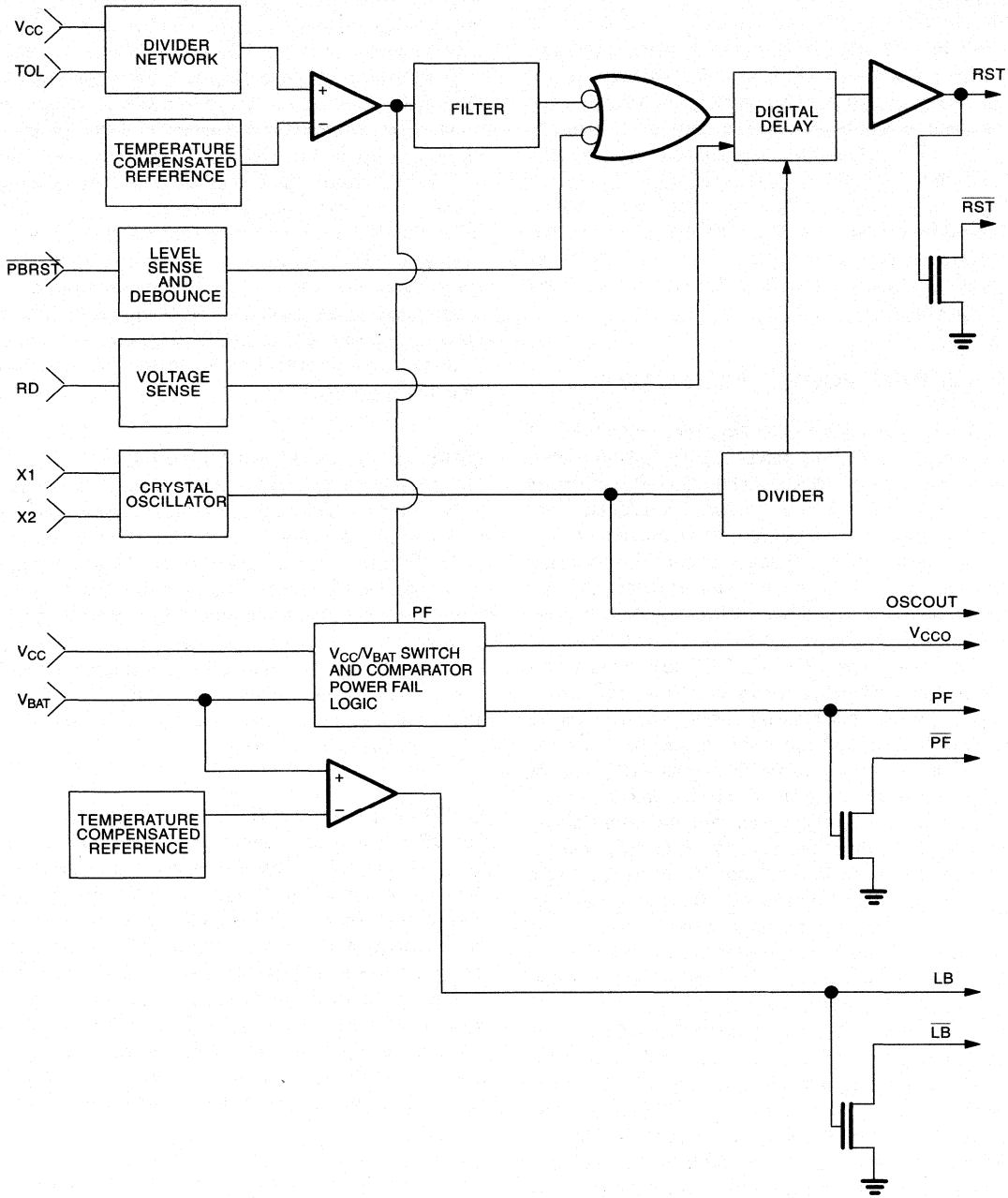
PIN DESCRIPTION

PBRST	-	Pushbutton Reset Input
X1, X2	-	Crystal Inputs
V_{BAT}	-	Battery Input
LB, LB	-	Low Battery Outputs
RST, RST	-	Reset Outputs
RD	-	Reset Duration
TOL	-	Selects 5% Or 10% Detection
GND	-	Ground
OSCOUT	-	Oscillator Out
V_{CCO}	-	Switched Power Out
PF, PF	-	Power Fail Outputs
V_{CC}	-	+5 Volt Power In

DESCRIPTION

The DS1632 PC Power Fail and Reset Controller is designed to do various functions involving battery backup and other functions typically accomplished with discrete components. The DS1632 provides a 32.768 KHz battery backed up crystal oscillator and switched V_{CC}/V_{BAT} power via V_{CCO} for the real–time clock function located in accompanying chip sets. In addition, the DS1632 provides for reset on both power up and via pushbutton input, power fail status signals for the processor, and low battery warning signals. The DS1632 is capable of detecting power failure at both the 5% and 10% power supply tolerances, and the reset pulse width can be set for either 95 ms or 190 ms. The device is designed to connect directly to popular laptop and notebook chip sets which eliminates the need for discrete components and reduces cost.

BLOCK DIAGRAM Figure 1



OPERATION – CRYSTAL OSCILLATOR SECTION

The DS1632 crystal oscillator is designed to be hooked directly to a 32.768 KHz crystal. By using the Daiwa Part No. DT26S, Seiko Part No. DS-VT-200 or equivalent, the oscillator will be accurate enough to run a real time clock to within ±2 minutes per month. If another crystal is to be selected, it should have a specified load capacitance (C_L) of 6 pF. The crystal oscillator will run as long as either V_{CC} or V_{BAT} is present, providing that V_{BAT} is greater than 2.3V. The oscillator output provides a rail to rail swing with regards to V_{CC} or V_{BAT}, whichever is greater. The crystal oscillator is also used internally as a time base.

OPERATION – POWER FAIL, BATTERY BACKUP

The DS1632 provides a switch to direct power from the battery (V_{BAT}) or the incoming supply (V_{CC}) depending on which is greater. This switch has a voltage drop of less than 0.2 volts. The V_{CC} input is constantly monitored by a precision comparator for an out of tolerance condition. When such a condition occurs, the power fail signals are driven to their active state immediately. The reset signals are also driven active, but this action is delayed by a time determined by the level of the input on the reset duration pin (RD). If RD is tied to ground then reset signals will become active after 9 ms. If RD is tied to V_{CC}, then reset signals will become active after 18 ms. Once active, both the reset signals and the power fail signals will remain active as long as a (V_{CC}) out of tolerance condition persists. If an out of tolerance condition is not long enough to activate the reset signals, then only the power fail signals would be affected. When power returns to within nominal limits the power fail signals will return immediately to the inactive state. However, the reset signals remain in the active state for a time which is dependent on the state of the RD pin. If RD is tied to ground, the reset signals will remain active for 95 ms. If RD is tied to V_{CC}, then the reset signals will remain active for 190 ms after power is within nominal limits. The delay action on the reset signals allows time for the power supply and microprocessor clock oscillators to stabilize. The tolerance pin (TOL) selects the point at which power fail detection occurs. With the tolerance pin grounded, power fail detection occurs in the range of 4.75V to 4.5V. If the tolerance pin is connected to V_{CC}, then power fail detection occurs in the range of 4.5V to 4.25V. During most power supply conditions the V_{CC} input will supply power to all functions within the chip and also to the V_{CCO} pin. The battery pin (V_{BAT}) only supplies power when V_{CC} is less than V_{BAT}. When V_{CC} is below the level of V_{BAT} only the V_{CCO} and the OSC OUT pin remain powered by V_{BAT}. All other outputs will be driven to ground when in a logic low state and will be driven to V_{CC} when in a logic high state. This is done to preserve battery capacity by avoiding battery drain resulting from loads on these outputs. The output ground level will be maintained for all levels of V_{CC}, even V_{CC} = GND. However, the output V_{CC} level will be maintained only for V_{CC} > 2.0V. Internal battery power consumption is less than 2 µA while V_{BAT} is supplying power. The external load on OSC OUT and V_{CCO} must be added to internal consumption to determine the total load on the battery.

OPERATION – PUSHBUTTON RESET

The DS1632 provides an input pin for direct connection to a pushbutton. The pushbutton reset input $\overline{\text{PBRST}}$ requires an active low level input. While TTL levels are sufficient to properly activate this input, it has been primarily designed for contact closure. Internally, this input is debounced and timed such that RST and $\overline{\text{RST}}$ signals of 95ms or 190 ms minimum are generated. If RD is tied to ground, then a reset pulse of 95 ms is generated. If RD is tied to V_{CC} then a reset pulse of 190 ms is generated. The delay time is started as the pushbutton reset input is released from low level.

OPERATION – LOW BATTERY WARNING

The DS1632 provides outputs which warn of a low battery condition. Whenever V_{CC} is within nominal limits, the V_{BAT} input is continuously monitored. If the V_{BAT} input is out of tolerance, the low battery outputs are driven to their active states, and will remain in the active state as long as V_{CC} is within nominal limits or until the battery input is restored to an in limit status. On power up, if the V_{BAT} input is out of tolerance, the low battery outputs are not guaranteed active until power fail is deactivated, but guaranteed active prior to reset inactive. When V_{CC} is below the V_{CC} fail trip point both LB and $\overline{\text{LB}}$ will be driven to ground.

For application information, please reference Application Note 64, published separately.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	-0.5V to +7.0V
Voltage on I/O Relative to Ground	–0.5V to V_{CC} + 0.5V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
$\overline{PBRST}$ Input High Level	V_{IH}	2.0		V_{CC}+0.3	V	1, 3
$\overline{PBRST}$ Input Low Level	V_{IL}	-0.3		+0.8	V	1, 3
Battery Supply Voltage	V_{BAT}	2.3	3.0	3.5	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Current @ 2.4V	I_{OH}	1			mA	5, 7
Output Current @ 0.4V	I_{OL}	4			mA	7
Output Voltage @ -500 µA	V_{OH}	V_{CC}-0.5V	V_{CC}-0.1V		V	1, 6
Low Level @ RST	V_{OL}			0.4	V	1
Operating Current	I_{CC}		0.5	2.0	mA	2
V_{CC} Trip Point (TOL=GND)	V_{CCTP}	4.50	4.62	4.75	V	1
V_{CC} Trip Point (TOL=V_{CC})	V_{CCTP}	4.25	4.37	4.50	V	1
Battery Fail Trip Point	V_{BATTP}	2.30	2.45	2.55	V	1
Supply Voltage Output	V_{CCO}	V_{CC}-0.2			V	
Supply Current Output	I_{CCO1}			100	mA	4

DC ELECTRICAL CHARACTERISTICS

(0°C; V_{CC} = < V_{BAT})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Battery Current	I_{BAT}			2	µA	
Battery Backup Current	I_{CCO2}			500	µA	4

CAPACITANCE

(t_A = 25°C)

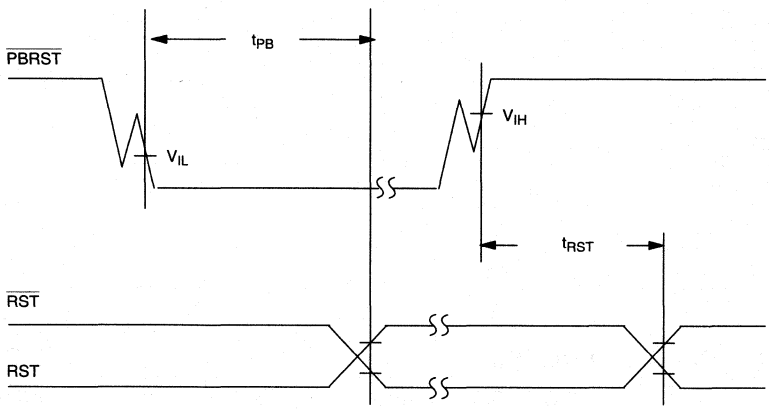
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

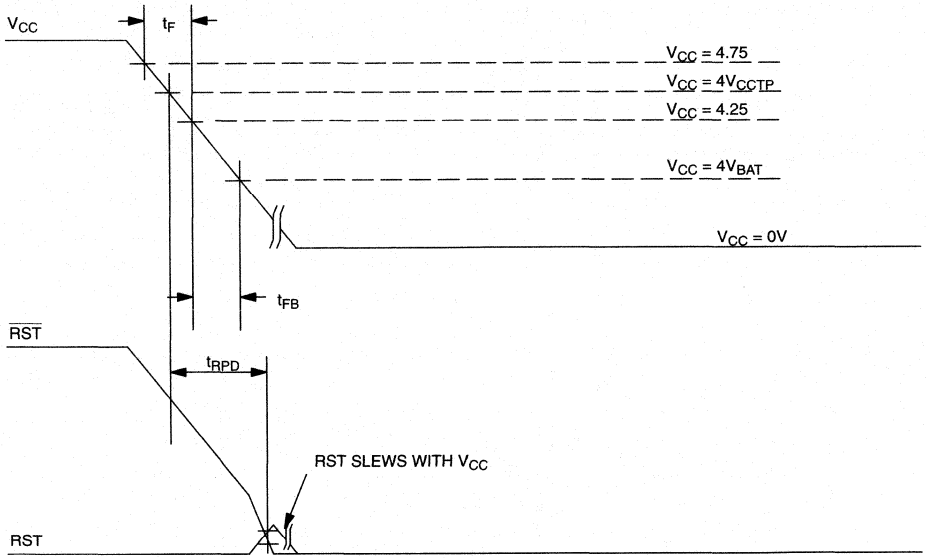
(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{PBRST}$ = V_{IL}	t_{PB}	t_{RPD}			ms	
Reset Pulse Width	t_{RST}	95		105	ms	RD=GND
Reset Pulse Width	t_{RST}	190		210	ms	RD=V_{CC}
Reset Active on Power Up	t_{RPU}	95		105	ms	RD=GND
Reset Active on Power Up	t_{RPU}	190		210	ms	RD=V_{CC}
Reset Active on Power Down	t_{RPD}	9		11	ms	RD=GND
Reset Active on Power Down	t_{RPD}	18		22	ms	RD=V_{CC}
V_{CC} Slew Rate Power Down	t_F	300			µs	
V_{CC} Slew Rate Power Down	t_{FB}	10			µs	
V_{CC} Slew Rate Power Up	t_R	10			µs	

TIMING DIAGRAM: PUSHBUTTON RESET



TIMING DIAGRAM: POWER DOWN



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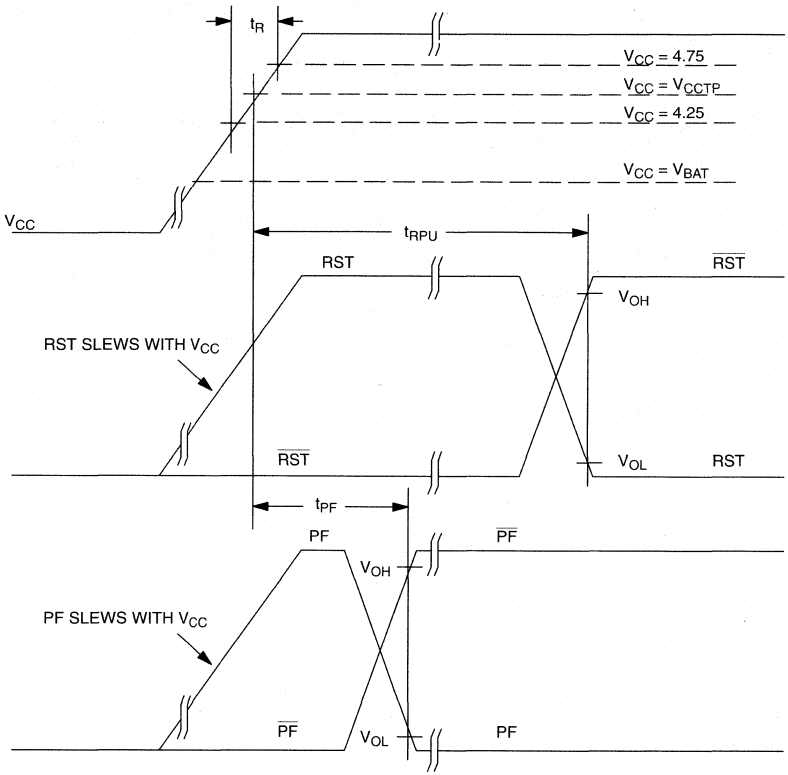
TIMING DIAGRAM: POWER UP



NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open.
3. The $\overline{PBRST}$ input has an internal pull up of 10KΩ to V_{CC}.
4. Supply current output is specified with 0.2V drop from V_{BAT} or V_{CC}.
5. $\overline{RST}$, $\overline{PF}$, and $\overline{LB}$ are open drain outputs.
6. RST and PF remain within 0.5 volts of V_{CC} on power down until V_{CC} drops below 2.0V.
7. Sink and source currents apply to all outputs except OSC OUT which has a drive capability of sourcing 500 µA at $V_{OH} = V_{CCO}$ - 0.5V and sinking 1 mA at V_{OL} = 0.5 V.

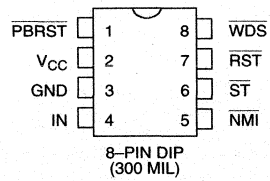
DALLAS SEMICONDUCTOR

DS1705/DS1706
3.3 and 5.0 Volt MicroMonitor

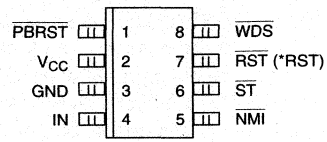
FEATURES

- Halts and restarts an out–of–control microprocessor
- Holds microprocessor in check during power transients
- Automatically restarts microprocessor after power failure
- Monitors pushbutton for external override
- Accurate 5%, 10% or 20% resets for 3.3 systems and 5% or 10% resets for 5.0 volt systems
- Eliminates the need for discrete components
- 3.3 volt 20% tolerance for use with 3.0 volt systems
- Pin compatible with the MAXIM MAX705/MAX706 in 8–pin DIP and 8–pin SOIC
- 8–pin DIP, 8–pin SOIC and 8–pin µ–SOP packages
- Industrial temperature range –40°C to +85°C

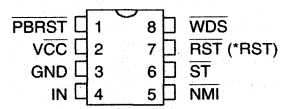
PIN ASSIGNMENT



8–PIN DIP
(300 MIL)



8–PIN SOIC
(150 MIL)



8–PIN µ–SOP
(118 MIL)

See Mech. Drawings
Section

DS1705 and DS1706_/R/S/T (*DS1706L and DS1706P)

PIN DESCRIPTION

$\overline{PBRST}$	–	Pushbutton Reset Input
V_{CC}	–	Power Supply
GND	–	Ground
IN	–	Input
$\overline{NMI}$	–	Non–maskable Interrupt
$\overline{ST}$	–	Strobe Input
$\overline{RST}$	–	Active Low Reset Output
*RST	–	Active High Reset Output (DS1706P and DS1706L only)
$\overline{WDS}$	–	Watchdog Status Output

DESCRIPTION

The DS1705/DS1706 3.3 or 5.0 Volt MicroMonitor monitors three vital conditions for a microprocessor: power supply, software execution, and external override. A precision temperature compensated reference and comparator circuit monitors the status of V_{CC} at the device and at an upstream point for maximum protection. When the sense input detects an out–of–tolerance condition a non–maskable interrupt is generated. As the voltage at the device degrades an internal power fail signal is generated which forces the reset to an active state. When V_{CC} returns to an in–tolerance condition, the reset signal is kept in the active state for a minimum of 130 ms to allow the power supply and processor to stabilize.

The second function the DS1705/DS1706 performs is pushbutton reset control. The DS1705/DS1706 debounces the pushbutton input and guarantees an active reset pulse width of 130 ms minimum.

The third function is a watchdog timer. The DS1705/DS1706 has an internal timer that forces the reset signals to the active state if the strobe input is not driven low prior to time–out.

OPERATION

Power Monitor

The DS1705/DS1706 detects out–of–tolerance power supply conditions and warns a processor–based system of impending power failure. When V_{CC} falls below the minimum V_{CC} tolerance, a comparator outputs the $\overline{RST}$ (or RST) signal. $\overline{RST}$ (or RST) is an excellent control signal for a microprocessor, as processing is stopped at the last possible moment of valid V_{CC}. On power–up, $\overline{RST}$ (or RST) are kept active for a minimum of 130 ms to allow the power supply and processor to stabilize.

Pushbutton Reset

The DS1705/DS1706 provides an input pin for direct connection to a pushbutton reset (see Figure 2). The pushbutton reset input requires an active low signal. Internally, this input is debounced and timed such that a $\overline{RST}$ (or RST) signal of at least 130 ms minimum will be generated. The 130 ms delay commences as the pushbutton reset input is released from the low level. The pushbutton can be initiated by connecting the $\overline{WDS}$ or $\overline{NMI}$ outputs to the $\overline{PBRST}$ input as shown in Figure 3.

Non–Maskable Interrupt

The DS1705/DS1706 generates a non–maskable interrupt ($\overline{NMI}$) for early warning of a power failure. A precision comparator monitors the voltage level at the IN pin relative to an on–chip reference generated by an internal band gap. The IN pin is a high impedance input allowing for a user–defined sense point. An external resistor voltage divider network (Figure 5) is used to interface with high voltage signals. This sense point may be derived from a regulated supply or from a higher DC voltage level closer to the main system power input. Since the IN trip point V_{TP} is 1.25 volts, the proper values for R1 and R2 can be determined by the equation as shown in Figure 5. Proper operation of the DS1705/DS1706 requires that the voltage at the IN pin be limited to V_{CC}. Therefore, the maximum allowable voltage at the supply being monitored (V_{MAX}) can also be derived as shown in Figure 5. A simple approach to solving the equation is to select a value for R2 high enough to keep power consumption low, and solve for R1. The flexibility of the IN input pin allows for detection of power loss at the earliest point in a power supply system, maximizing the amount of time for system shut–down between $\overline{NMI}$ and $\overline{RST}$ (or RST).

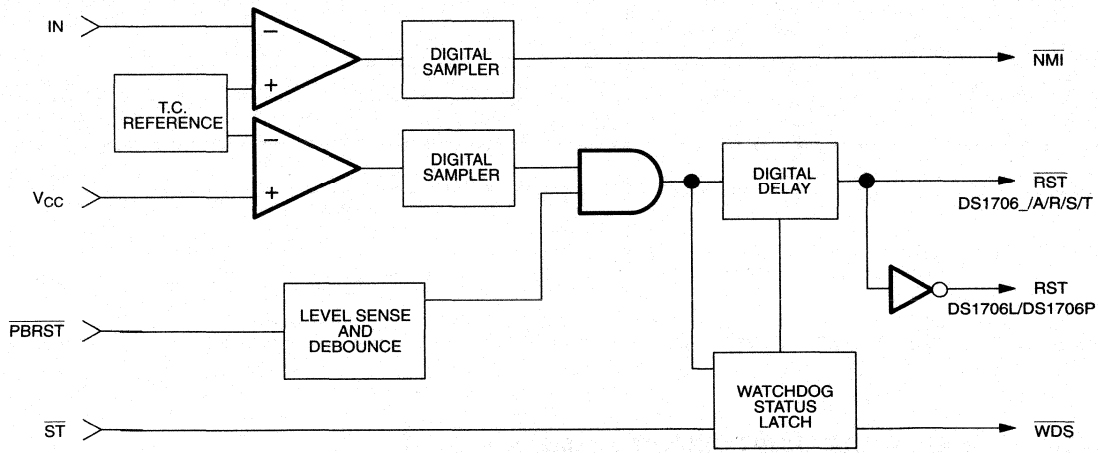
When the supply being monitored decays to the voltage sense point, the DS1705/DS1706 pulses the $\overline{NMI}$ output to the active state for a minimum 200 µs. The $\overline{NMI}$ power fail detection circuitry also has built–in hysteresis of 100 µV. The supply must be below the voltage sense point for approximately 5 µs before a low $\overline{NMI}$ will be generated. In this way, power supply noise is removed from the monitoring function, preventing false interrupts. During a power–up, any detected IN pin levels below V_{TP} by the comparator are disabled from generating an interrupt until V_{CC} rises to V_{CCTP}. As a result, any potential $\overline{NMI}$ pulse will not be initiated until V_{CC} reaches V_{CCTP}.

Connecting $\overline{NMI}$ to $\overline{PBRST}$ would allow non–maskable interrupt to generate an automatic reset when an out–of–tolerance condition occurred in a monitored supply. An example is shown in Figure 3.

Watchdog Timer

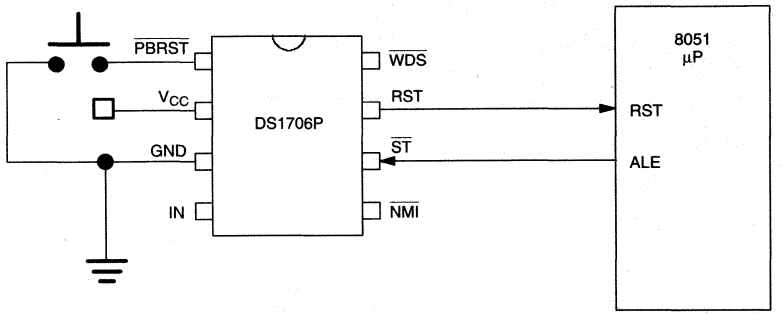
The watchdog timer function forces $\overline{WDS}$ signals active when the $\overline{ST}$ input is not clocked within the 1 second time out period. Timeout of the watchdog starts when $\overline{RST}$ (or RST) becomes inactive. If a high–to–low transition occurs on the $\overline{ST}$ input pin prior to time–out, the watchdog timer is reset and begins to time–out again. If the watchdog timer is allowed to time out, the $\overline{WDS}$ signal is driven active (low) for a minimum of 130 ms. The $\overline{ST}$ input can be derived from many microprocessor outputs. The typical signals used are the microprocessors address signals, data signals, or control signals. When the microprocessor functions normally, these signals would, as a matter of routine, cause the watchdog to be reset prior to time–out. To guarantee that the watchdog timer does not time–out, a high–to–low transition must occur at or less than the minimum watchdog time–out of 1 second. A typical circuit example is shown in Figure 6.

MICROMONITOR BLOCK DIAGRAM Figure 1

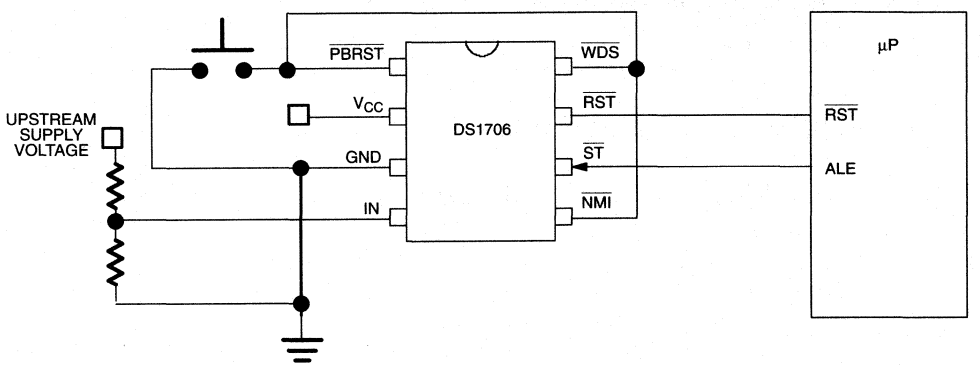


3

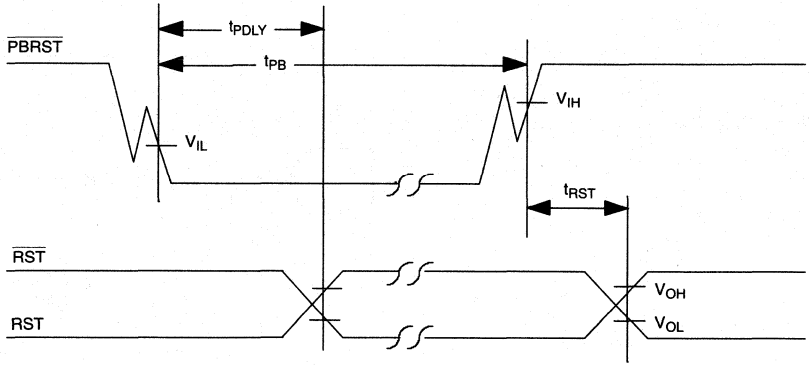
PUSHBUTTON RESET Figure 2



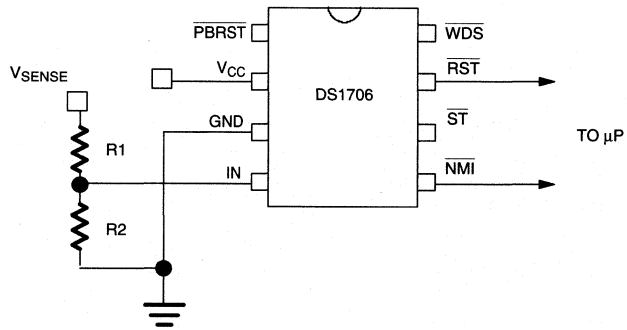
PUSHBUTTON RESET CONTROLLED BY NMI AND WDS Figure 3



TIMING DIAGRAM: PUSHBUTTON RESET Figure 4



NON–MASKABLE INTERRUPT CIRCUIT EXAMPLE Figure 5



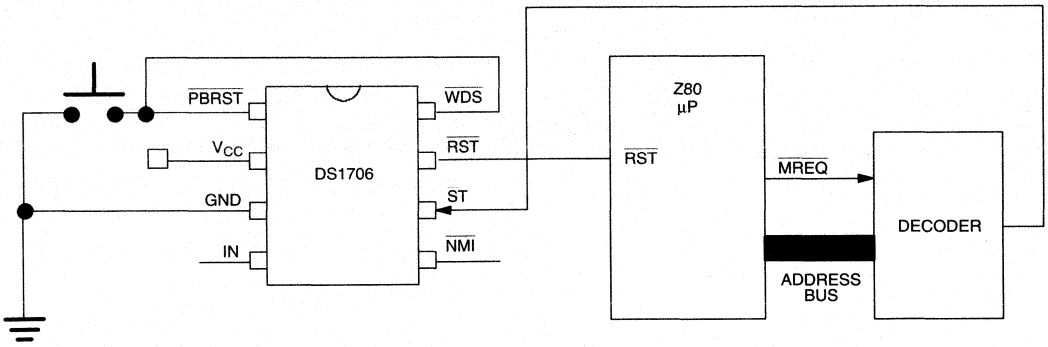
$$V_{SENSE} = \frac{R1 + R2}{R2} \times 1.25 \qquad V_{MAX} = \frac{V_{SENSE}}{V_{TP}} \times V_{CC}$$

Example: V_{SENSE} = 4.50 volts at the trip point
V_{CC} = 3.3 volts
10KΩ = R2

Therefore: $\frac{4.50}{1.25} \times 3.3 = 12.4$ volts maximum

$$4.5 = \frac{R1 + 10K}{10K} \times 1.25 \qquad R1 = 26K\Omega$$

WATCHDOG TIMER Figure 6



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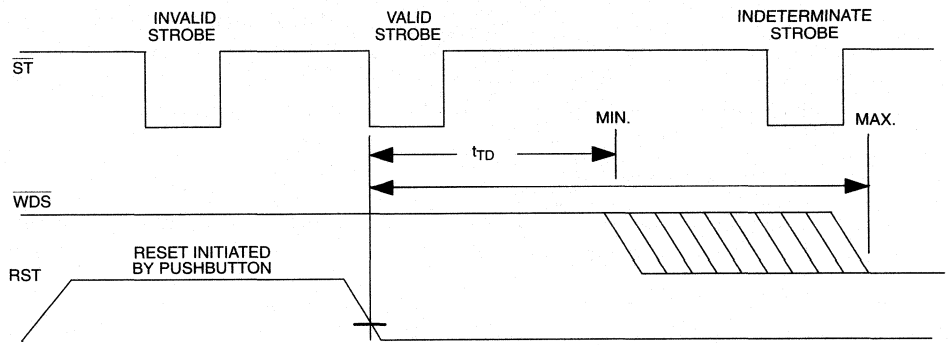
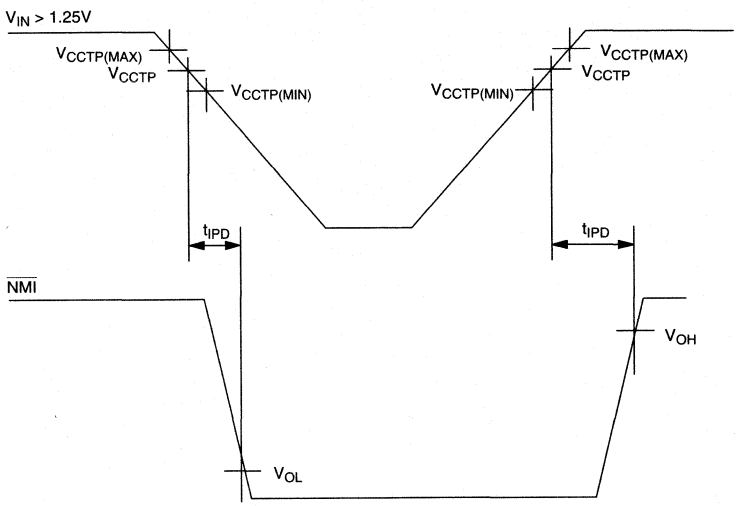
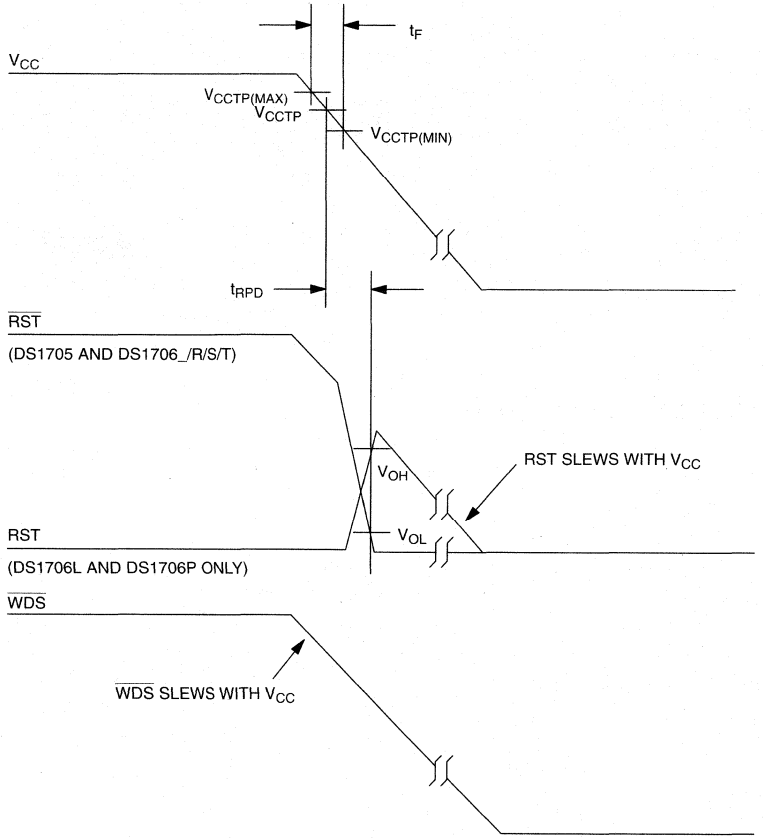
TIMING DIAGRAM: STROBE INPUT Figure 7



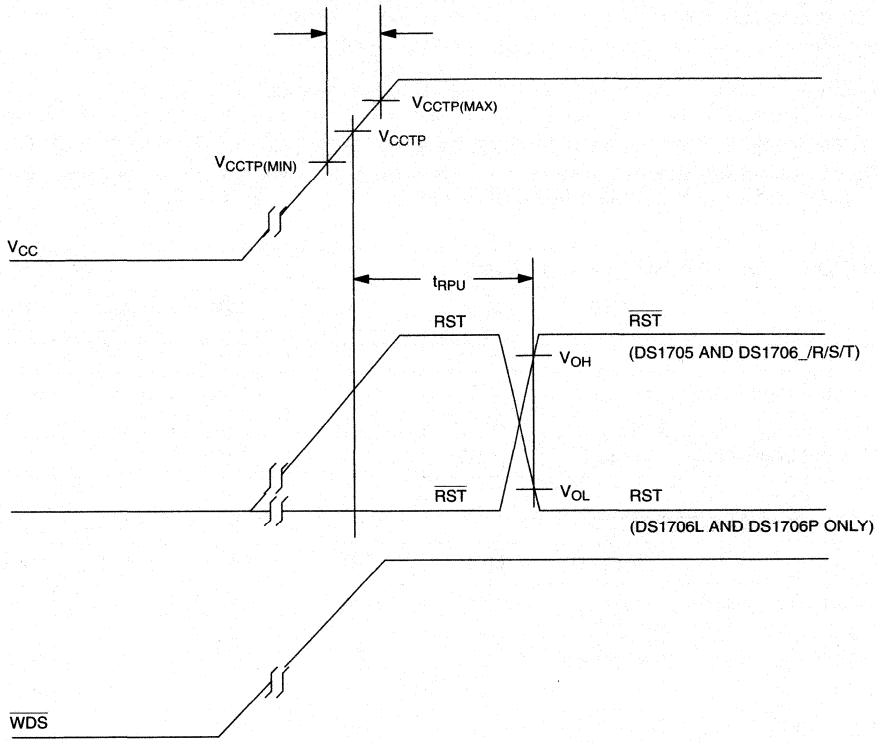
TIMING DIAGRAM: NON–MASKABLE INTERRUPT Figure 8



TIMING DIAGRAM: POWER DOWN Figure 9



TIMING DIAGRAM: POWER UP Figure 10



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	–0.5V to +7.0V
Voltage on I/O Relative to Ground	–0.5V to V_{CC} + 0.5V
Operating Temperature	–40°C to +85°C
Storage Temperature	–55°C to 125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(–40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	1.0		5.5	V	1
$\overline{ST}$ and $\overline{PBRST}$ Input High Level	V_{IH}	2.0 V_{CC}–0.5		V_{CC}+0.3	V	1, 3 1, 4
$\overline{ST}$ and $\overline{PBRST}$ Input Low Level	V_{IL}	–0.03		0.5	V	1

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC}=1.2V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} Trip Point DS1705/DS1706L	V_{CCTP}	4.50	4.65	4.75	V	1
V_{CC} Trip Point DS1706	V_{CCTP}	4.25	4.40	4.50	V	1
V_{CC} Trip Point DS1706T	V_{CCTP}	3.00	3.08	3.15	V	1
V_{CC} Trip Point DS1706S	V_{CCTP}	2.85	2.93	3.00	V	1
V_{CC} Trip Point DS1706P or R	V_{CCTP}	2.55	2.63	2.70	V	1
Input Leakage	I_{IL}	–1.0		+1.0	µA	2
Output Current @ 2.4V	I_{OH}		350		µA	3
Output Current @ 0.4V	I_{OL}	10			mA	3
Output Voltage @ –500 µA	V_{OH}	V_{CC}+–0.3	V_{CC}–0.1		V	3
Operating Current @ V_{CC} < 5.5V	I_{CC}			50	µA	5
Operating Current @ V_{CC} < 3.6V	I_{CC}			35	µA	5
IN Input Trip Point	V_{TP}	1.20	1.25	1.30	V	1

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC}=1.2V to 5.5V)

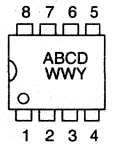
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{PBRST}$ = V_{IL}	t_{PB}	150			ns	
Reset Active Time	t_{RST}	130	205	285	ms	
$\overline{ST}$ Pulse Width	t_{ST}	10			ns	6
V_{CC} Detect to RST and $\overline{RST}$	t_{RPD}		5	8	µs	9
V_{CC} Slew Rate	t_F	20			µs	
V_{CC} Detect to RST and $\overline{RST}$	t_{RPU}	130	205	285	ms	7
V_{CC} Slew Rate	t_R	0			ns	
$\overline{PBRST}$ Stable Low to RST and $\overline{RST}$	t_{PDLY}			250	ns	
Watchdog Timeout	t_{TD}	1.0	1.6	2.2	s	8
VIN Detect to $\overline{NMI}$	t_{IPD}		5	8	µs	9

3

NOTES:

1. All voltages are referenced to ground.
2. $\overline{PBRST}$ is internally pulled up to V_{CC} with an internal impedance of 40KΩ typical and the $\overline{ST}$ input is internally pulled up to V_{CC} with an internal impedance of 180KΩ typical.
3. $V_{CC} \geq 2.4V$
4. $V_{CC} < 2.4V$
5. Measured with outputs open and all inputs at V_{CC} or ground.
6. Must not exceed t_{TD} minimum.
7. t_R = 5 µs
8. Minimum watchdog timeout tested at 2.7 volts for the 3.3 volt devices and 4.5 volts for the 5.0 volt devices.
9. Noise immunity – pulses < 2 µs at V_{CCTP} minimum will not cause a reset.

PART MARKING CODES



8–PIN μ–SOP
(118 MIL)

A, B, C and D represents the device type and tolerance.

ABCD		
705_	–	DS1705
706_	–	DS1706
706L	–	DS1706L
706P	–	DS1706P
706R	–	DS1706R
706S	–	DS1706S
706T	–	DS1706T

WWY represents the device manufacturing Work Week, Year.

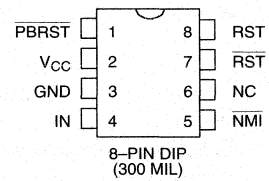
DALLAS SEMICONDUCTOR

DS1707/DS1708
3.3 and 5.0 Volt MicroMonitor

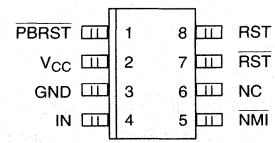
FEATURES

- Holds microprocessor in check during power transients
- Automatically restarts microprocessor after power failure
- Monitors pushbutton for external override
- Accurate 5%, 10% or 20% resets for 3.3 systems and 5% or 10% resets for 5.0 volt systems
- Eliminates the need for discrete components
- 20% tolerance compatible with 3.0 volt systems
- Pin compatible with the MAXIM MAX707/MAX708 in 8–pin DIP and 8–pin SOIC packages
- 8–pin DIP, 8–pin SOIC and 8–pin µ–SOP packages available
- Industrial temperature range –40°C to +85°C

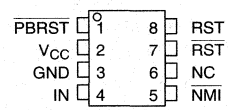
PIN ASSIGNMENT



8–PIN DIP
(300 MIL)



8–PIN SOIC
(150 MIL)



8–PIN µ–SOP
(118 MIL)

See Mech. Drawings Section

DS1705 and DS1706_/R/S/T (*DS1706L and DS1706P)

PIN DESCRIPTION

$\overline{PBRST}$	–	Pushbutton Reset Input
V_{CC}	–	Power Supply
GND	–	Ground
IN	–	Input
$\overline{NMI}$	–	Non–maskable Interrupt
NC	–	No Connect
$\overline{RST}$	–	Active Low Reset Output
RST	–	Active High Reset Output

DESCRIPTION

The DS1707/DS1708 3.3 or 5.0 Volt MicroMonitor monitors three vital conditions for a microprocessor: power supply, voltage sense, and external override. A precision temperature–compensated reference and comparator circuit monitors the status of V_{CC} at the device and at an upstream point for maximum protection. When the sense input detects an out–of–tolerance condition a non–maskable interrupt is generated. As the voltage at the device degrades an internal power fail signal is generated which forces the reset to an active state. When V_{CC} returns to an in–tolerance condition, the reset signal is kept in the active state for a minimum of 130 ms to allow the power supply and processor to stabilize.

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The third function the DS1707/DS1708 performs is pushbutton reset control. The DS1707/DS1708 debounces the pushbutton input and guarantees an active reset pulse width of 130 ms minimum.

OPERATION

Power Monitor

The DS1707/DS1708 detects out–of–tolerance power supply conditions and warns a processor–based system of impending power failure. When V_{CC} falls below the minimum V_{CC} tolerance, a comparator outputs the RST and $\overline{RST}$ signals. RST and $\overline{RST}$ are excellent control signals for a microprocessor, as processing is stopped at the last possible moment of valid V_{CC}. On power–up, RST and $\overline{RST}$ are kept active for a minimum of 130 ms to allow the power supply and processor to stabilize.

Pushbutton Reset

The DS1707/DS1708 provides an input pin for direct connection to a pushbutton reset (see Figure 2). The pushbutton reset input requires an active low signal. Internally, this input is debounced and timed such that RST and $\overline{RST}$ signals of at least 130 ms minimum will be generated. The 130 ms delay commences as the pushbutton reset input is released from the low level. The pushbutton can be initiated by connecting the $\overline{NMI}$ output to the $\overline{PBRST}$ input as shown in Figure 3.

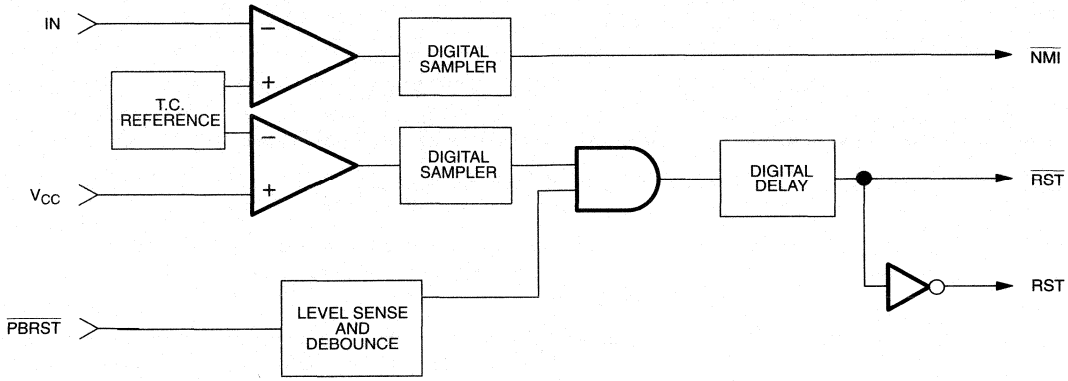
Non–Maskable Interrupt

The DS1707/DS1708 generates a non–maskable interrupt ($\overline{NMI}$) for early warning of a power failure. A precision comparator monitors the voltage level at the IN pin relative to an on–chip reference generated by an internal band gap. The IN pin is a high impedance input allowing for a user–defined sense point. An external resistor voltage divider network (Figure 5) is used to interface with high voltage signals. This sense point may be derived from a regulated supply or from a higher DC voltage level closer to the main system power input. Since the IN trip point V_{TP} is 1.25 volts, the proper values for R1 and R2 can be determined by the equation as shown in Figure 5. Proper operation of the DS1707/DS1708 requires that the voltage at the IN pin be limited to V_{CC}. Therefore, the maximum allowable voltage at the supply being monitored (V_{MAX}) can also be derived as shown in Figure 5. A simple approach to solving the equation is to select a value for R2 high enough to keep power consumption low, and solve for R1. The flexibility of the IN input pin allows for detection of power loss at the earliest point in a power supply system, maximizing the amount of time for system shut–down between $\overline{NMI}$ and RST/$\overline{RST}$.

When the supply being monitored decays to the voltage sense point, the DS1707/DS1708 pulses the $\overline{NMI}$ output to the active state for a minimum 200 µs. The $\overline{NMI}$ power fail detection circuitry also has built–in hysteresis of 100 µV. The supply must be below the voltage sense point for approximately 5 µs before a low $\overline{NMI}$ will be generated. In this way, power supply noise is removed from the monitoring function, preventing false interrupts. During a power–up, any detected IN pin levels below V_{TP} by the comparator are disabled from generating an interrupt until V_{CC} rises to V_{CCTP}. As a result, any potential $\overline{NMI}$ pulse will not be initiated until V_{CC} reaches V_{CCTP}.

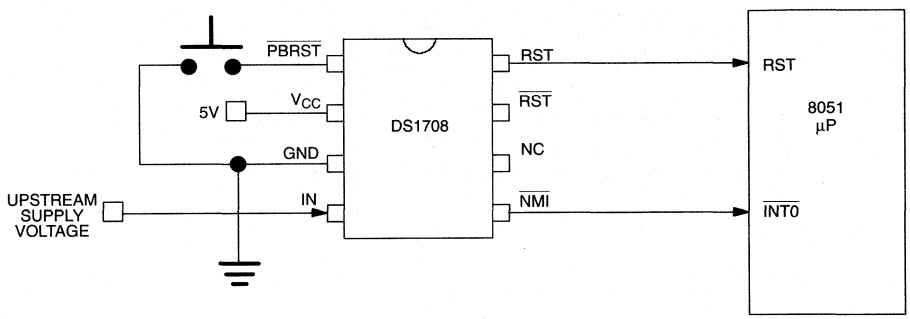
Connecting $\overline{NMI}$ to $\overline{PBRST}$ would allow the non–maskable interrupt to generate an automatic reset when an out–of–tolerance condition occurred in a monitored supply. An example is shown in Figure 3.

MICROMONITOR BLOCK DIAGRAM Figure 1

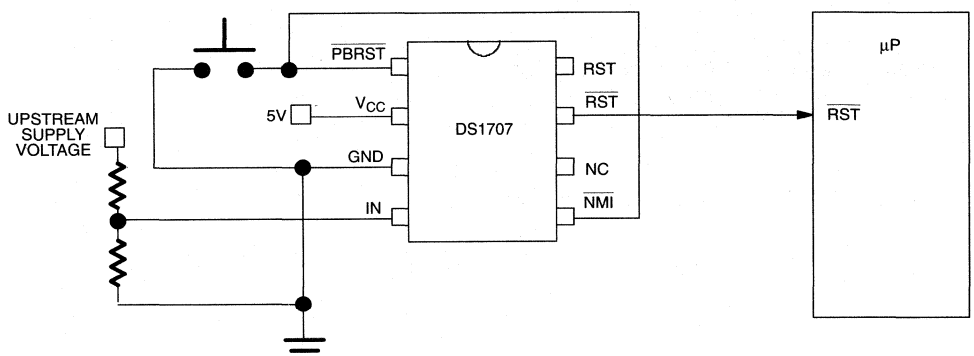


3

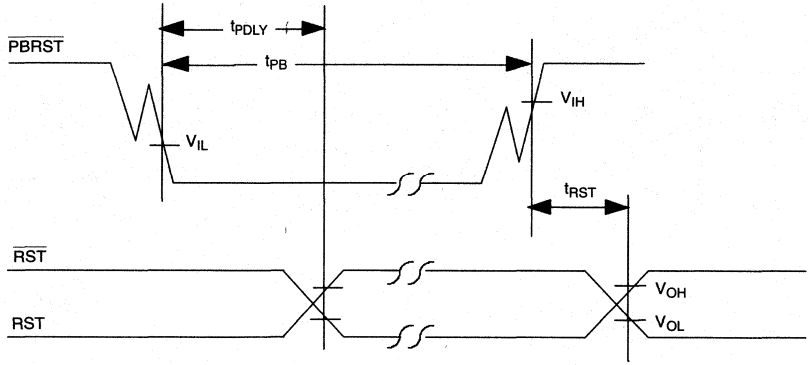
PUSHBUTTON RESET Figure 2



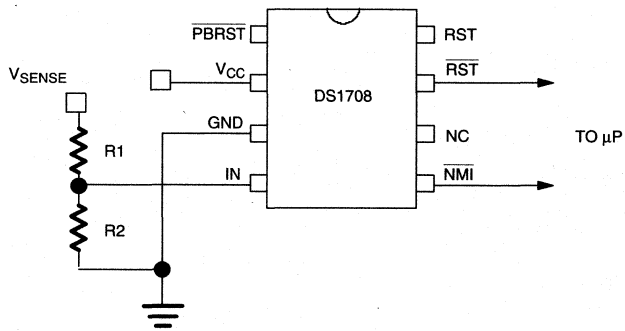
PUSHBUTTON RESET CONTROLLED BY NMI Figure 3



TIMING DIAGRAM: PUSHBUTTON RESET Figure 4



NON–MASKABLE INTERRUPT CIRCUIT EXAMPLE Figure 5



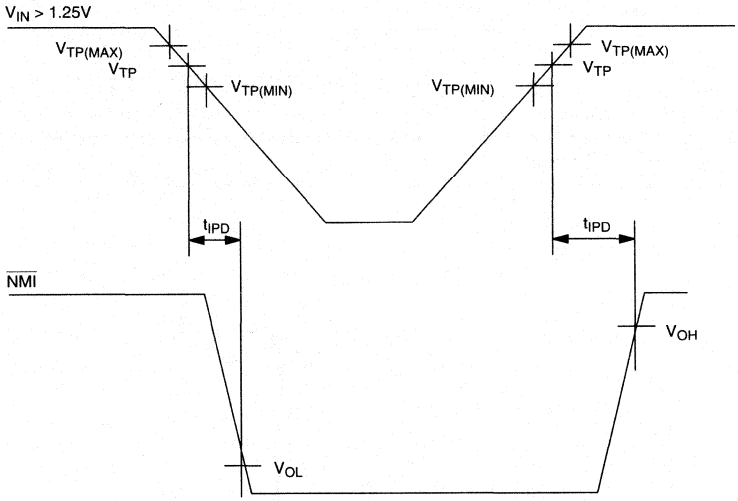
$$V_{SENSE} = \frac{R1 + R2}{R2} \times 1.25 \qquad V_{MAX} = \frac{V_{SENSE}}{V_{TP}} \times V_{CC}$$

Example: V_{SENSE} = 4.70 volts at the trip point
V_{CC} = 3.3 volts
10KΩ = R2

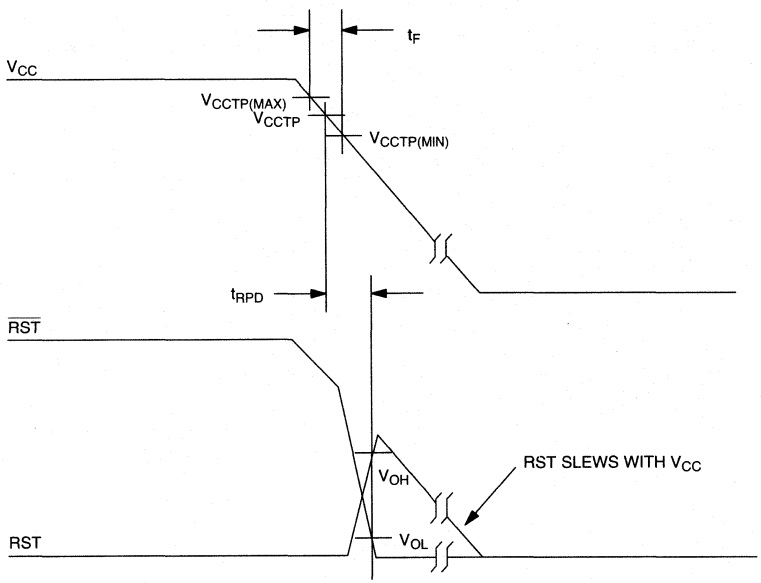
Therefore: $\frac{4.70}{1.25} \times 3.3 = 12.4$ volts maximum

$$4.5 = \frac{R1 + 10K}{10K} \times 1.25 \qquad R1 = 27.6K\Omega$$

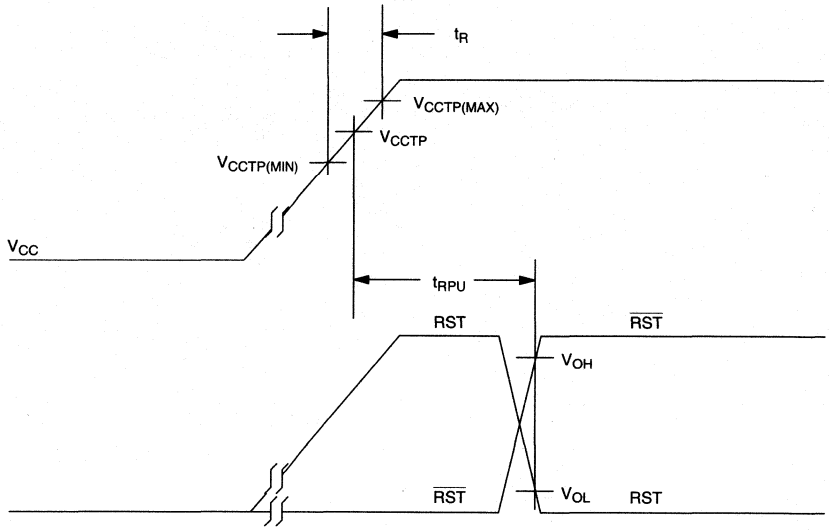
TIMING DIAGRAM: NON–MASKABLE INTERRUPT Figure 6



TIMING DIAGRAM: POWER DOWN Figure 7



TIMING DIAGRAM: POWER UP Figure 8



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	–0.5V to +7.0V
Voltage on I/O Relative to Ground	–0.5V to V_{CC} + 0.5V
Operating Temperature	–40°C to +85°C
Storage Temperature	–55°C to 125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(–40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	1.0		5.5	V	1
$\overline{PBRST}$ Input High Level	V_{IH}	2.0 V_{CC}–0.5		V_{CC}+0.3	V	1, 3 1, 4
$\overline{PBRST}$ Input Low Level	V_{IL}	–0.03		0.5	V	1

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC}=1.2V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} Trip Point DS1707	V_{CCTP}	4.50	4.65	4.75	V	1
V_{CC} Trip Point DS1708	V_{CCTP}	4.25	4.40	4.50	V	1
V_{CC} Trip Point DS1708T	V_{CCTP}	3.00	3.08	3.15	V	1
V_{CC} Trip Point DS1708S	V_{CCTP}	2.85	2.93	3.00	V	1
V_{CC} Trip Point DS1708R	V_{CCTP}	2.55	2.63	2.70	V	1
Input Leakage	I_{IL}	–1.0		+1.0	µA	2
Output Current @ 2.4V	I_{OH}		350		µA	3
Output Current @ 0.4V	I_{OL}	10			mA	3
Output Voltage	V_{OH}		V_{CC}–0.1		V	3
Operating Current @ V_{CC} < 5.5V	I_{CC}			50	µA	5
Operating Current @ V_{CC} < 3.6V	I_{CC}			35	µA	5
IN Input Trip Point	V_{TP}	1.20	1.25	1.30	V	1

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

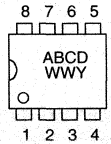
(–40°C to +85°C; V_{CC}=1.2V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{PBRST}$ = V_{IL}	t_{PB}	150			ns	
Reset Active Time	t_{RST}	130	205	285	ms	
V_{CC} Detect to RST and $\overline{RST}$	t_{RPD}		5	8	µs	7
V_{CC} Slew Rate	t_F	20			µs	
V_{CC} Detect to RST and $\overline{RST}$	t_{RPU}	130	205	285	ms	6
V_{CC} Slew Rate	t_R	0			ns	
$\overline{PBRST}$ Stable Low to RST and $\overline{RST}$	t_{PDLY}			250	ns	
VIN Detect to $\overline{NMI}$	t_{IPD}		5	8	µs	7

NOTES:

1. All voltages are referenced to ground.
2. $\overline{PBRST}$ is internally pulled up to V_{CC} with an internal impedance of 40KΩ typical.
3. $V_{CC} \geq 2.4V$
4. $V_{CC} < 2.4V$
5. Measured with outputs open and all inputs at V_{CC} or ground.
6. t_R = 5 µs
7. Noise immunity – pulses < 2 µs at V_{CCTP} minimum will not cause a reset.

PART MARKING CODES



8–PIN μ–SOP
(118 MIL)

A, B, C and D represents the device type and tolerance.

ABCD		
707_	–	DS1707
708_	–	DS1708
708R	–	DS1708R
708S	–	DS1708S
708T	–	DS1708T

WWY represents the device manufacturing Work Week, and Year.

PRODUCT PREVIEW

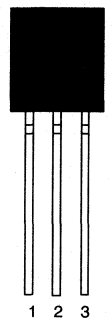
DALLAS SEMICONDUCTOR

DS1810
5V EconoReset

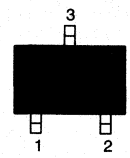
FEATURES

- Automatically restarts a microprocessor after power failure
- Maintains reset for 220 ms after V_{CC} returns to an in-tolerance condition
- Reduces need for discrete components
- Precision temperature-compensated voltage reference and voltage sensor
- Low-cost TO-92, surface-mount SOT-223, or space saving surface mount SOT–23 packages available
- Push-Pull output for low current operation

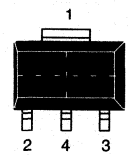
PIN ASSIGNMENT



TO-92 Package
See Mech. Drawings Section



SOT-23 Package



SOT-223 Package
See Mech. Drawings Section

PIN DESCRIPTIONS

TO–92

1	$\overline{RST}$	Active Low Reset Output
2	V_{CC}	Power Supply
3	GND	Ground

SOT–23

1	$\overline{RST}$	Active Low Reset Output
2	V_{CC}	Power Supply
3	GND	Ground

SOT–223

1	GND	Ground
2	$\overline{RST}$	Active Low Reset Output
3	GND	Ground
4	V_{CC}	Power Supply

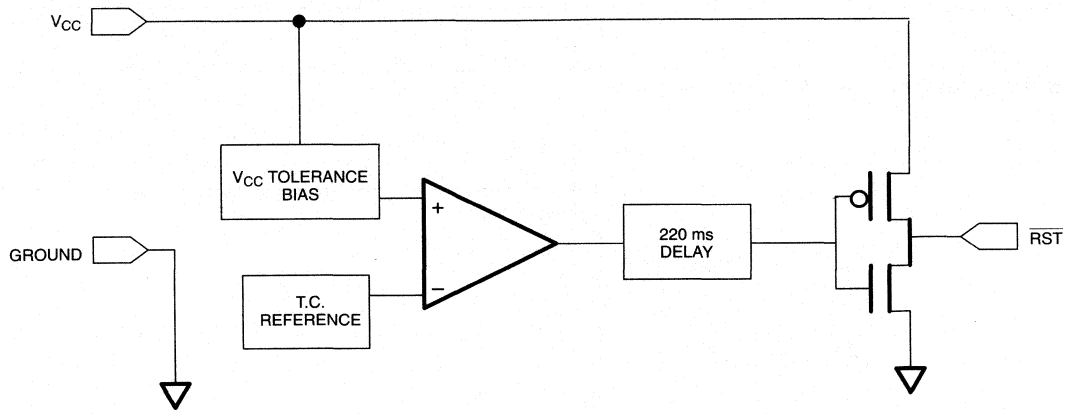
DESCRIPTION

The DS1810 EconoReset uses a precision temperature reference and comparator circuit to monitor the status of the power supply (V_{CC}). When an out-of-tolerance condition is detected, an internal power fail signal is generated which forces reset to the active state. When V_{CC} returns to an in-tolerance condition, the reset signal is kept in the active state for approximately 220 ms to allow the power supply and processor to stabilize.

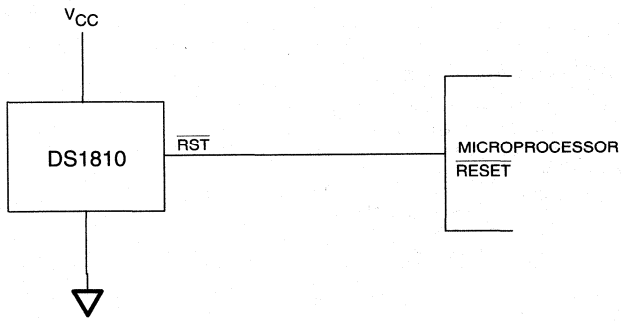
OPERATION – POWER MONITOR

The DS1810 provides the function of detecting out-of-tolerance power supply conditions and warning a processor-based system of impending power failure. When V_{CC} is detected as out-of-tolerance, the $\overline{RST}$ signal is asserted. On power-up, $\overline{RST}$ is kept active for approximately 220 ms after the power supply has reached the selected tolerance. This allows the power supply and microprocessor to stabilize before $\overline{RST}$ is released.

BLOCK DIAGRAM (OPEN-DRAIN OUTPUT) Figure 1



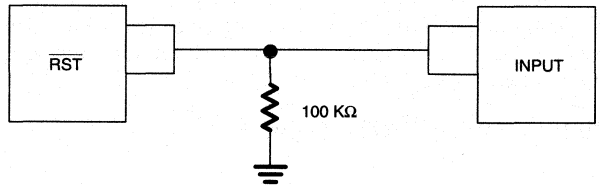
APPLICATION EXAMPLE Figure 2



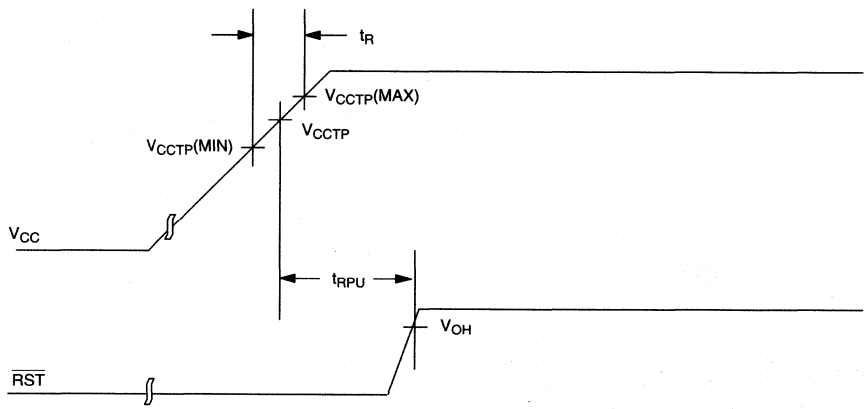
OUTPUT VALID CONDITIONS

All versions of the DS1810 can maintain a valid output as long as V_{CC} remains above 1.2 volt. However, the $\overline{RST}$ outputs on the DS1810 use a push-pull structure which can maintain a valid output below 1.2 volt on an input. To sink current below 1.2 volt, a resistor can be connected from $\overline{RST}$ to Ground (see Figure 3.) This arrangement will maintain a valid value on the $\overline{RST}$ outputs even it V_{CC} approaches 0 volts. During both power up and down this arrangement will draw current when $\overline{RST}$ is in the high state. A value of about 100 KΩ should be adequate to maintain a valid condition.

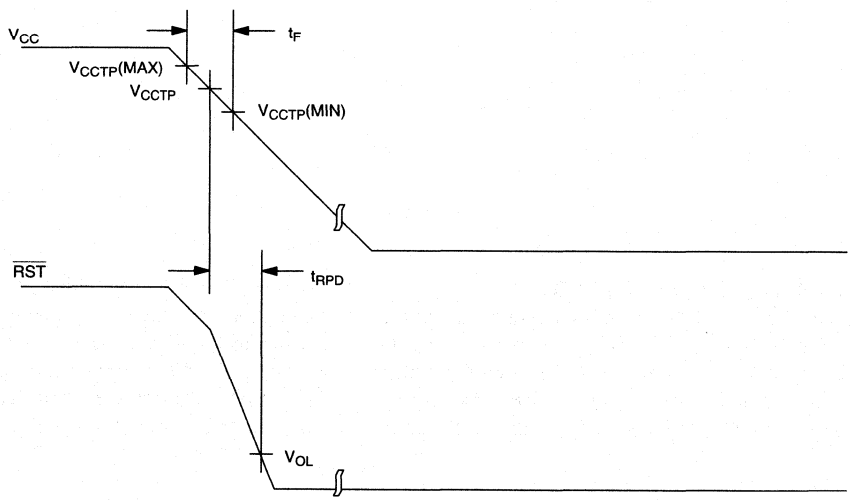
APPLICATION DIAGRAM: $\overline{RST}$ VALID TO 0 VOLTS VCC ON THE DS1810 Figure 3



TIMING DIAGRAM: POWER UP Figure 4



TIMING DIAGRAM: POWER DOWN Figure 5



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	–0.5V to +7.0V
Voltage on $\overline{RST}$ Relative to Ground	–0.5V to V_{CC} + 0.5V
Operating Temperature	0°C to +70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	+260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	1.2		5.5	V	1

3

DC ELECTRICAL CHARACTERISTICS

(0°C to +70°C; V_{CC} = 1.2V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Voltage @ 0-500µA	V_{OH}	V_{CC} -0.5V	V_{CC} -0.1V		V	1
Output Current @ 2.4V	I_{OH}		350		µA	2
Output Current @ 0.4V	I_{OL}	+10			mA	2,3
Operating Current V_{CC} <5.5	I_{CC}		28	50	µA	4
V_{CC} Trip Point (DS1810-5)	V_{CCTP}	4.50	4.62	4.75	V	1
V_{CC} Trip Point (DS1810-10)	V_{CCTP}	4.25	4.37	4.49	V	1
V_{CC} Trip Point (DS1810-15)	V_{CCTP}	4.00	4.12	4.24	V	1
Output Capacitance	C_{OUT}			10	pF	

AC ELECTRICAL CHARACTERISTICS

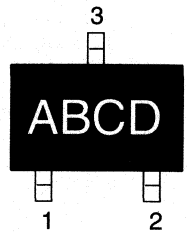
(0°C to +70°C; V_{CC} = 1.2V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RESET Active Time	t_{RST}	130	220	340	ms	
V_{CC} Detect to $\overline{RST}$	t_{RPD}		2	5	µs	
V_{CC} Slew Rate (V_{CCTP} (MAX) to V_{CCTP} (MIN))	t_F	300			µs	
V_{CC} Slew Rate (V_{CCTP} (MIN) to V_{CCTP} (MAX))	t_R	0			ns	
V_{CC} Detect to $\overline{RST}$	t_{RPU}	130	220	340	ms	5

NOTES:

1. All voltages are referenced to ground.
2. Measured with $V_{CC} \geq 2.7V$.
3. A 1KΩ external resistor may be required in some applications for proper operation of the microprocessor reset control circuit.
4. Measured with $\overline{RST}$ output open.
5. t_R = 5 µs.

PART MARKING CODES



"A", "B", & "C" represents the Device Type.

810	–	DS1810
811	–	DS1811
812	–	DS1812
813	–	DS1813
815	–	DS1815
816	–	DS1816
817	–	DS1817
818	–	DS1818

"D" represents the Device Tolerance.

A	–	5%
B	–	10%
C	–	15%
D	–	20%

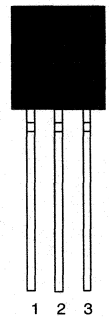
DALLAS SEMICONDUCTOR

DS1811
5V EconoReset

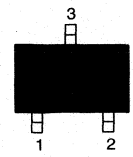
FEATURES

- Automatically restarts a microprocessor after power failure
- Maintains reset for 220 ms after V_{CC} returns to an in-tolerance condition
- Reduces need for discrete components
- Precision temperature-compensated voltage reference and voltage sensor
- Low-cost TO-92, SOT-223 surface-mount package, or space saving SOT–23 packages available
- Efficient open-drain output with internal 5 KΩ pull-up resistor

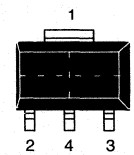
PIN ASSIGNMENT



TO-92 Package
See Mech. Drawings Section



SOT-23 Package



SOT-223 Package
See Mech. Drawings Section

PIN DESCRIPTIONS

TO–92

1	$\overline{RST}$	Active Low Reset Output
2	V_{CC}	Power Supply
3	GND	Ground

SOT–23

1	$\overline{RST}$	Active Low Reset Output
2	V_{CC}	Power Supply
3	GND	Ground

SOT–223

1	GND	Ground
2	$\overline{RST}$	Active Low Reset Output
3	GND	Ground
4	V_{CC}	Power Supply

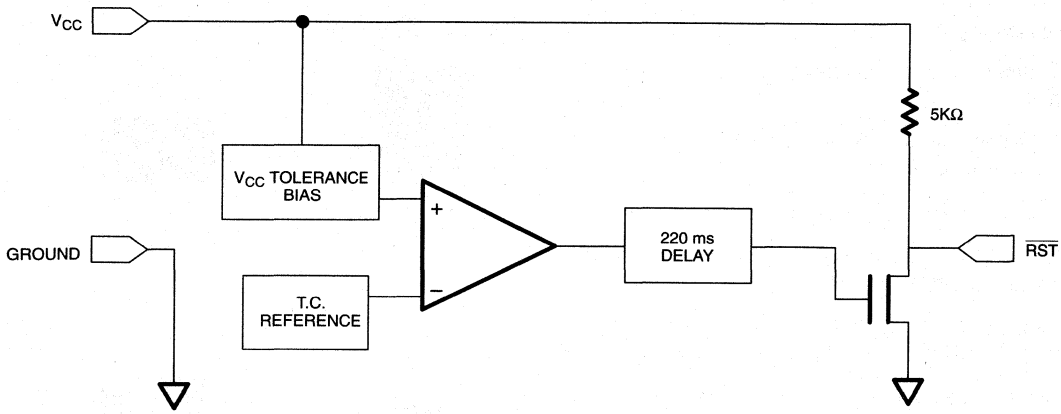
DESCRIPTION

The DS1811 EconoReset uses a precision temperature reference and comparator circuit to monitor the status of the power supply (V_{CC}). When an out-of-tolerance condition is detected, an internal power fail signal is generated which forces reset to the active state. When V_{CC} returns to an in-tolerance condition, the reset signal is kept in the active state for approximately 220 ms to allow the power supply and processor to stabilize.

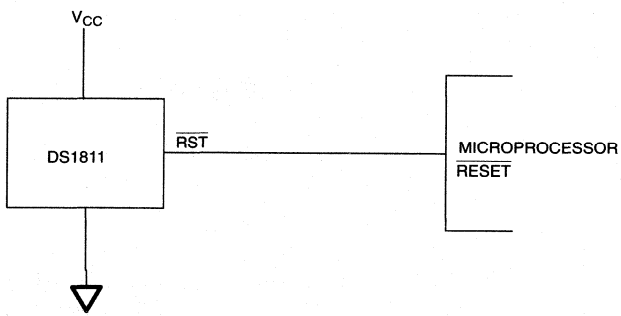
OPERATION – POWER MONITOR

The DS1811 provides the functions of detecting out-of-tolerance power supply conditions and warning a processor-based system of impending power failure. When V_{CC} is detected as out-of-tolerance, the $\overline{RST}$ signal is asserted. On power-up, $\overline{RST}$ is kept active for approximately 220 ms after the power supply has reached the selected tolerance. This allows the power supply and microprocessor to stabilize before $\overline{RST}$ is released.

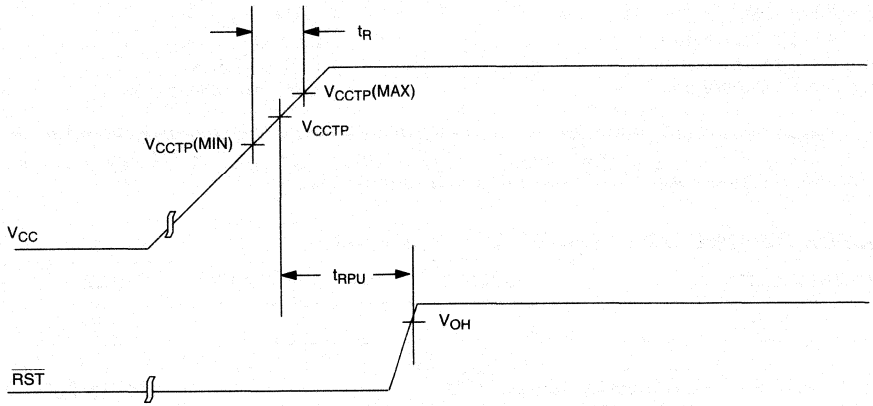
BLOCK DIAGRAM (OPEN-DRAIN OUTPUT) Figure 1



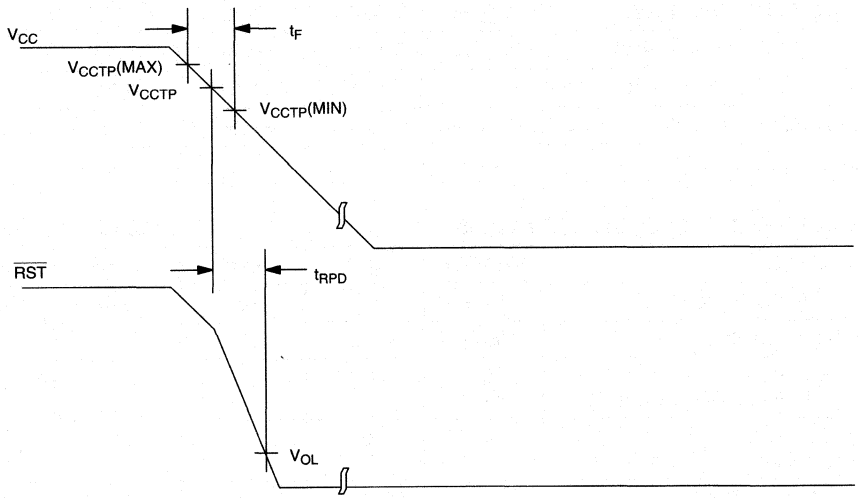
APPLICATION EXAMPLE Figure 2



TIMING DIAGRAM: POWER UP Figure 3



TIMING DIAGRAM: POWER DOWN Figure 4



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	–0.5V to +7.0V
Voltage on $\overline{RST}$ Relative to Ground	–0.5V to V_{CC} + 0.5V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	+260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	0.0		5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 1.2V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Current @ 0.4V	I_{OL}	+10			mA	2,3
Operating Current V_{CC} < 5.5V	I_{CC}		35	50	µA	4
V_{CC} Trip Point (DS1811–5)	V_{CCTP}	4.50	4.62	4.75	V	1
V_{CC} Trip Point (DS1811–10)	V_{CCTP}	4.25	4.35	4.49	V	1
V_{CC} Trip Point (DS1811–15)	V_{CCTP}	4.00	4.13	4.24	V	1
Internal Pull-Up Resistor	R_P	3.5	5.5	7.5	KΩ	
Output Capacitance	C_{OUT}			10	pF	

AC ELECTRICAL CHARACTERISTICS

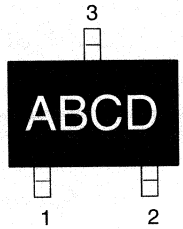
(0°C to 70°C; V_{CC} = 1.2V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RESET Active Time	t_{RST}	130	220	340	ms	5
V_{CC} Detect to $\overline{RST}$	t_{RPD}		2	5	µs	
V_{CC} Slew Rate (V_{CCTP} (MAX) to V_{CCTP} (MIN))	t_F	300			µs	
V_{CC} Slew Rate (V_{CCTP} (MIN) to V_{CCTP} (MAX))	t_R	0			ns	
V_{CC} Detect to $\overline{RST}$	t_{RPU}	130	220	340	ms	5, 6

NOTES:

1. All voltages are referenced to ground.
2. Measured with $V_{CC} \geq 2.7V$.
3. A 1KΩ external resistor may be required in some applications for proper operation of the microprocessor reset control circuit.
4. Measured with $\overline{RST}$ output open.
5. Measured with $4.5V \leq V_{CC} \leq 5.5V$.
6. t_R = 5 µs.

PART MARKING CODES



"A", "B", &"C" represent the device type.

810 .... DS1810
811 .... DS1811
812 .... DS1812
813 .... DS1813
815 .... DS1815
816 .... DS1816
817 .... DS1817
818 .... DS1818

"D" represents the device tolerance.

A 5%
B 10%
C 15%
D 20%

3

PRODUCT PREVIEW

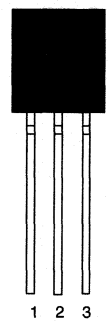
DALLAS SEMICONDUCTOR

DS1813
5V EconoReset with Pushbutton

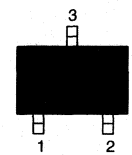
FEATURES

- Automatically restarts a microprocessor after power failure
- Monitors pushbutton for external override
- Maintains reset for typically 220 ms after V_{CC} returns to an in-tolerance condition
- Reduces need for discrete components
- Precision temperature-compensated voltage reference and voltage sensor
- Low-cost TO-92, surface-mount package SOT-223, or space saving surface-mount SOT–23 packages available
- Efficient open-drain output with internal 5.5 KΩ pull-up resistor

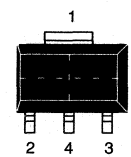
PIN ASSIGNMENT



TO-92 Package
See Mech. Drawings Section



SOT-23 Package



SOT-223 Package
See Mech. Drawings Section

PIN DESCRIPTIONS

TO–92

1	$\overline{RST}$	Active Low Reset Output
2	V_{CC}	Power Supply
3	GND	Ground

SOT–23

1	$\overline{RST}$	Active Low Reset Output
2	V_{CC}	Power Supply
3	GND	Ground

SOT–223

1	GND	Ground
2	$\overline{RST}$	Active Low Reset Output
3	GND	Ground
4	V_{CC}	Power Supply

DESCRIPTION

The DS1813 EconoReset uses a precision temperature reference and comparator circuit to monitor the status of the power supply (V_{CC}). When an out-of-tolerance condition is detected, an internal power fail signal is generated which forces reset to the active state. When V_{CC} returns to an in-tolerance condition, the reset signal is kept in the active state for approximately 220 ms to allow the power supply and processor to stabilize.

The DS1813 also monitors a pushbutton on the reset output. If the reset line is pulled low, a reset is generated upon release and will be held in reset output low for typically 220 ms.

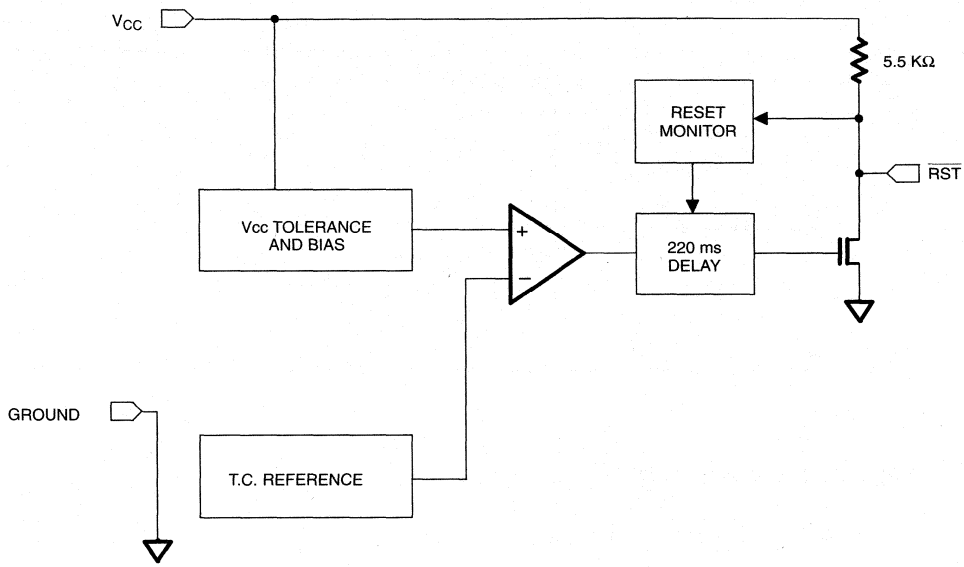
OPERATION – POWER MONITOR

The DS1813 provides the functions of detecting out-of-tolerance power supply conditions and warning a processor-based system of impending power failure. When V_{CC} is detected as out-of-tolerance, the $\overline{RST}$ signal is asserted. On power-up, $\overline{RST}$ is kept active for approximately 220 ms after the power supply has reached the selected tolerance. This allows the power supply and microprocessor to stabilize before $\overline{RST}$ is released.

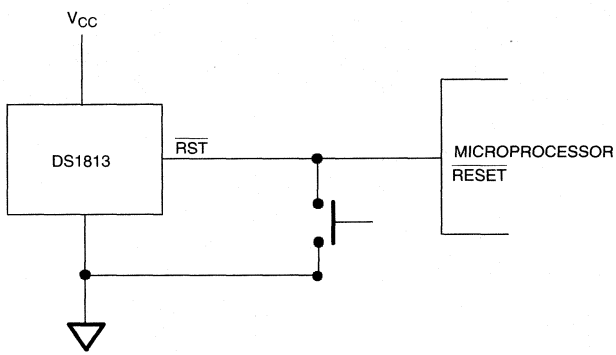
OPERATION – PUSHBUTTON RESET

The DS1813 provides for a pushbutton switch for manual reset control. When the DS1813 is not in a reset cycle, a pushbutton reset can be generated by pulling the $\overline{RST}$ pin low for at least 1 µs. When the pushbutton is held low, the $\overline{RESET}$ is forced active low and will remain active low for about 220 ms after the pushbutton is released. See Figure 2 for an application example and Figure 3 for the timing diagram.

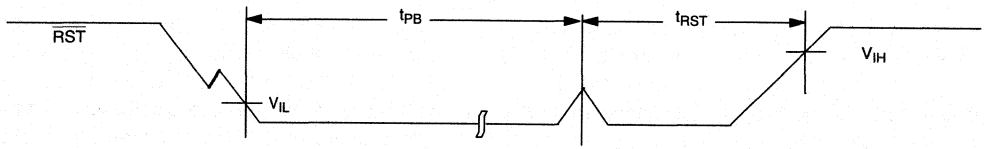
BLOCK DIAGRAM (OPEN-DRAIN OUTPUT) Figure 1



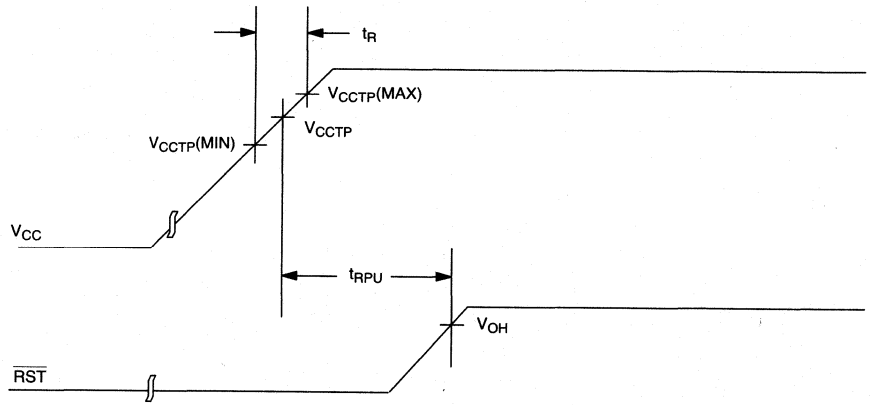
APPLICATION EXAMPLE Figure 2



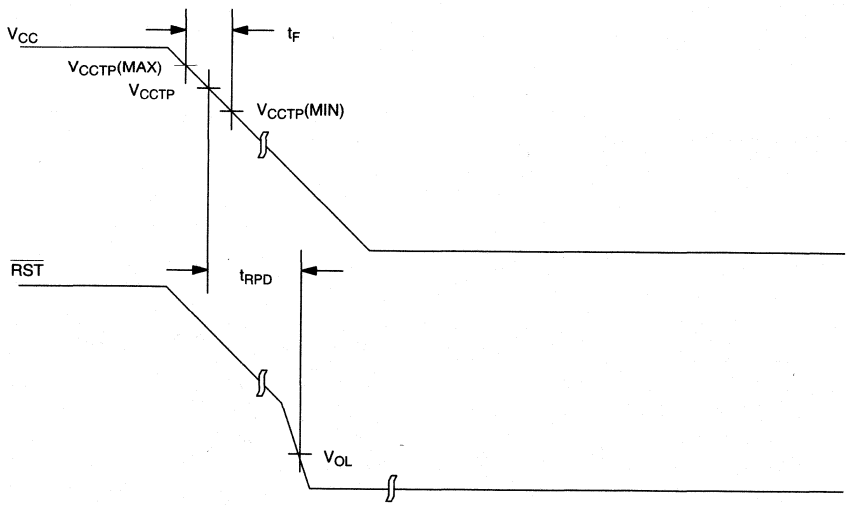
TIMING DIAGRAM: PUSHBUTTON RESET Figure 3



TIMING DIAGRAM: POWER UP Figure 4



TIMING DIAGRAM: POWER DOWN Figure 5



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	-0.5V to +7.0V
Voltage on $\overline{RST}$ Relative to Ground	–0.5V to $5V_{CC}$ + 0.5V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	+260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	0.0		5.5	V	1

3

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 1.2V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Current @ 0.4V	I_{OL}	+10			mA	2,3
Operating Current V_{CC} < 5.5	I_{CC}		35	50	µA	4
V_{CC} Trip Point (DS1813-5)	V_{CCTP}	4.50	4.62	4.75	V	1
V_{CC} Trip Point (DS1813-10)	V_{CCTP}	4.25	4.35	4.49	V	1
V_{CC} Trip Point (DS1813-15)	V_{CCTP}	4.00	4.13	4.24	V	1
Internal Pull-Up Resistor	R_P	3.50	5.5	7.5	K	
Output Capacitance	C_{OUT}			10	pF	

AC ELECTRICAL CHARACTERISTICS

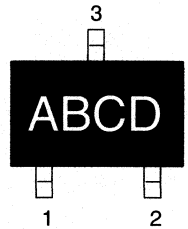
(0°C to 70°C; V_{CC} = 1.2V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RESET Active Time	t_{RST}	130	220	340	ms	6
V_{CC} Detect to $\overline{RST}$	t_{RPD}		2	5	µs	
V_{CC} Slew Rate (V_{CCTP} (MAX) – V_{CCTP} (MIN))	t_F	300			µs	
V_{CC} Slew Rate (V_{CCTP} (MIN) – V_{CCTP} (MAX))	t_R	0			ns	
V_{CC} Detect to $\overline{RST}$	t_{RPU}	130	220	340	ms	5,6
Pushbutton Detect to $\overline{RST}$	t_{PB}	1			µs	
Pushbutton Reset	t_{PBRST}	130	220	340	ms	6

NOTES:

1. All voltages are referenced to ground.
2. Measured with $V_{CC} \geq 2.7V$.
3. A 1KΩ external resistor may be required in some applications for proper operation of the microprocessor reset control circuit.
4. Measured with $\overline{RST}$ output open and V_{CC} high.
5. t_R = 5 µs.
6. Measured with $4.5V \leq V_{CC} \leq 5.5V$.

PART MARKING CODES



"A", "B", &"C" represent the device type.

810 .... DS1810
811 .... DS1811
812 .... DS1812
813 .... DS1813
815 .... DS1815
816 .... DS1816
817 .... DS1817
818 .... DS1818

"D" represents the device tolerance.

A 5%
B 10%
C 15%
D 20%

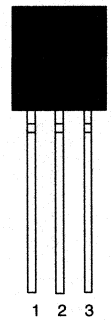
DALLAS SEMICONDUCTOR

DS1815
5V EconoReset

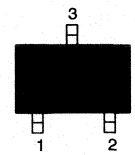
FEATURES

- Automatically restarts a microprocessor after power failure
- Maintains reset for 220 ms after V_{CC} returns to an in-tolerance condition
- Reduces need for discrete components
- Precision temperature-compensated voltage reference and voltage sensor
- Accurate 10% or 20% power monitoring
- Low-cost TO-92, surface-mount SOT-223, or space saving surface-mount SOT–23 packages available
- Push–Pull output for low current operation

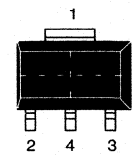
PIN ASSIGNMENT



TO-92 Package
See Mech. Drawings Section



SOT-23 Package



SOT-223 Package
See Mech. Drawings Section

PIN DESCRIPTIONS

TO–92

1	$\overline{RST}$	Active Low Reset Output
2	V_{CC}	Power Supply
3	GND	Ground

SOT–23

1	$\overline{RST}$	Active Low Reset Output
2	V_{CC}	Power Supply
3	GND	Ground

SOT–223

1	GND	Ground
2	$\overline{RST}$	Active Low Reset Output
3	GND	Ground
4	V_{CC}	Power Supply

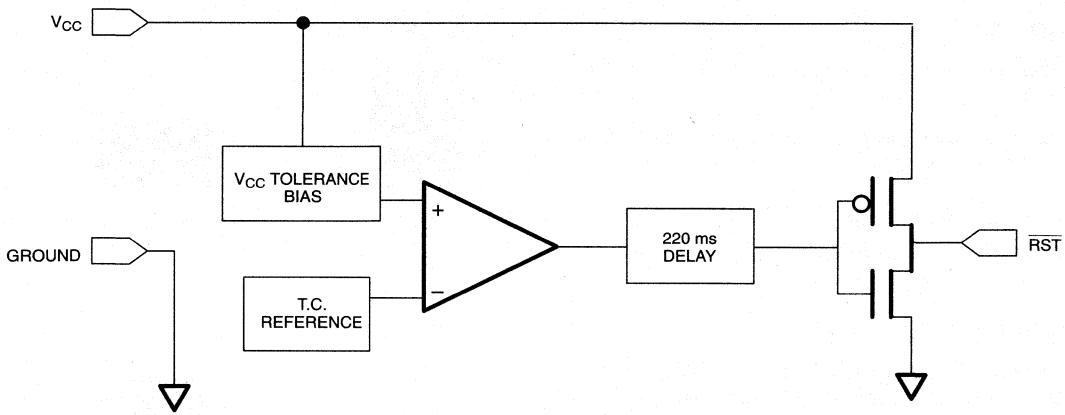
DESCRIPTION

The DS1815 EconoReset uses a precision temperature reference and comparator circuit to monitor the status of the power supply (V_{CC}). When an out-of-tolerance condition is detected, an internal power fail signal is generated which forces reset to the active state. When V_{CC} returns to an in-tolerance condition, the reset signal is kept in the active state for approximately 220 ms to allow the power supply and processor to stabilize.

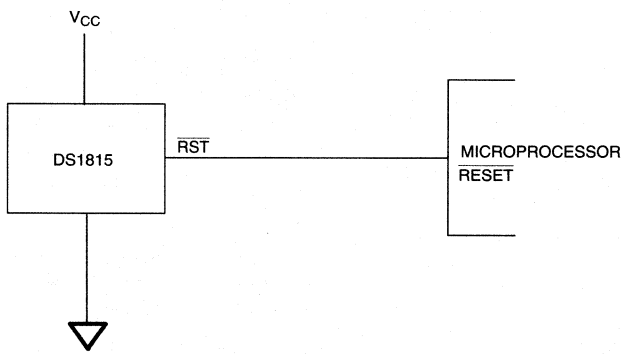
OPERATION – POWER MONITOR

The DS1815 provides the functions of detecting out-of-tolerance power supply conditions and warning a processor-based system of impending power failure. When V_{CC} is detected as out of tolerance, the $\overline{RST}$ signal is asserted. On power-up, $\overline{RST}$ is kept active for approximately 220 ms after the power supply has reached the selected tolerance. This allows the power supply and microprocessor to stabilize before $\overline{RST}$ is released.

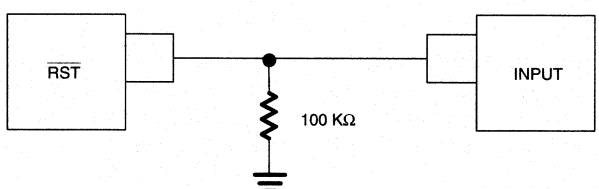
BLOCK DIAGRAM (CMOS OUTPUT) Figure 1



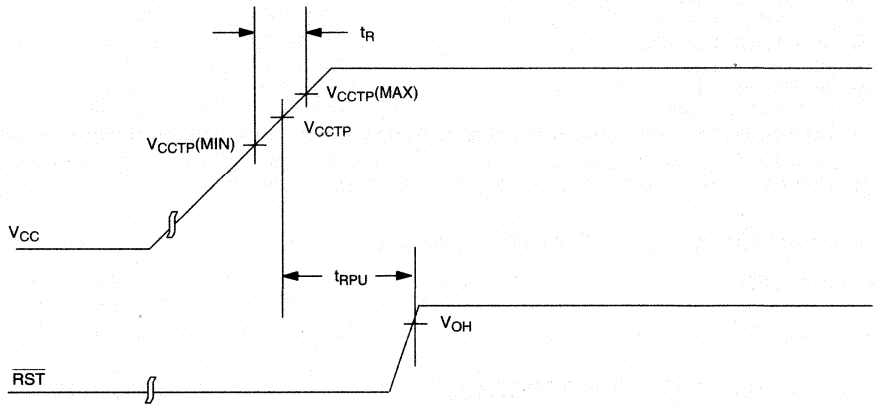
APPLICATION EXAMPLE Figure 2



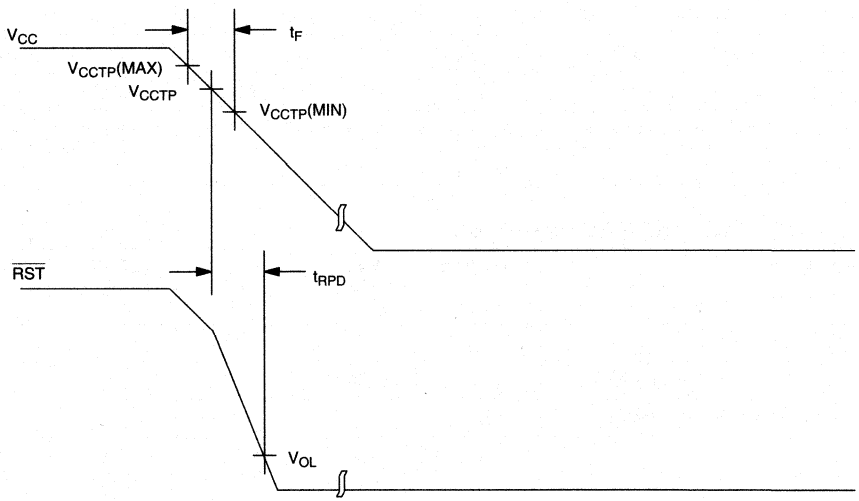
APPLICATION DIAGRAM: $\overline{RST}$ VALID TO 0 VOLTS V_{CC} ON THE DS1815 Figure 3



TIMING DIAGRAM: POWER UP Figure 4



TIMING DIAGRAM: POWER DOWN Figure 5



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	-0.5V to +7.0V
Voltage on $\overline{RST}$ Relative to Ground	–0.5V to $5V_{CC}$ + 0.5V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	+260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	0.0		5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 1.2V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Voltage @ -500 µA	V_{OH}	V_{CC}–0.5V	V_{CC}–0.1V		V	1
Output Current @ 2.4V	I_{OH}		350		µA	2
Output Current @ 0.4V	I_{OL}	+10			mA	2
Operating Current V_{CC} <5.5	I_{CC}		28	35	µA	3
V_{CC} Trip Point (DS1815-10)	V_{CCTP}	2.80	2.88	2.97	V	1
V_{CC} Trip Point (DS1815-15)	V_{CCTP}	2.47	2.55	2.64	V	1
Output Capacitance	C_{OUT}			10	pF	

AC ELECTRICAL CHARACTERISTICS

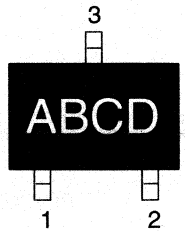
(0°C to 70°C; V_{CC} = 1.2V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RESET Active Time	t_{RST}	130	220	340	ms	4
V_{CC} Detect to $\overline{RST}$	t_{RPD}		2	5	µs	
V_{CC} Slew Rate (V_{CCTP} (MAX)	t_F	300			µs	
V_{CC} Slew Rate (V_{CCTP} (MIN)	t_R	0			ns	
V_{CC} Detect to $\overline{RST}$	t_{RPU}	130	220	340	ms	4, 5

NOTES:

1. All voltages are referenced to ground.
2. Measured with $V_{CC} \geq 2.7V$.
3. Measured with $\overline{RST}$ output open.
4. Measured with $2.7V \leq V_{CC} \leq 3.3V$.
5. t_R = 5 µs.

PART MARKING CODES



"A", "B", &"C" represent the device type.

810 .... DS1810
811 .... DS1811
812 .... DS1812
813 .... DS1813
815 .... DS1815
816 .... DS1816
817 .... DS1817
818 .... DS1818

"D" represents the device tolerance.

A 5%
B 10%
C 15%
D 20%

3

PRODUCT PREVIEW

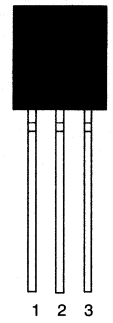
DALLAS SEMICONDUCTOR

DS1816
3.3V EconoReset

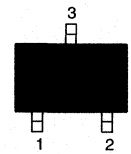
FEATURES

- Automatically restarts a microprocessor after power failure
- Maintains reset for 220 ms after V_{CC} returns to an in-tolerance condition
- Reduces need for discrete components
- Precision temperature-compensated voltage reference and voltage sensor
- Accurte 10% or 20% power monitoring
- 20% tolerance for use with 3.0 volt systems
- Low-cost TO-92, SOT-223 surface-mount package, or space saving SOT–23 packages available
- Efficient open-drain output with internal 5 KΩ pull-up resistor

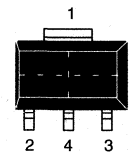
PIN ASSIGNMENT



TO-92 Package
See Mech. Drawings Section



SOT-23 Package



SOT-223 Package
See Mech. Drawings Section

PIN DESCRIPTIONS

TO–92

1	$\overline{RST}$	Active Low Reset Output
2	V_{CC}	Power Supply
3	GND	Ground

SOT–23

1	$\overline{RST}$	Active Low Reset Output
2	V_{CC}	Power Supply
3	GND	Ground

SOT–223

1	GND	Ground
2	$\overline{RST}$	Active Low Reset Output
3	GND	Ground
4	V_{CC}	Power Supply

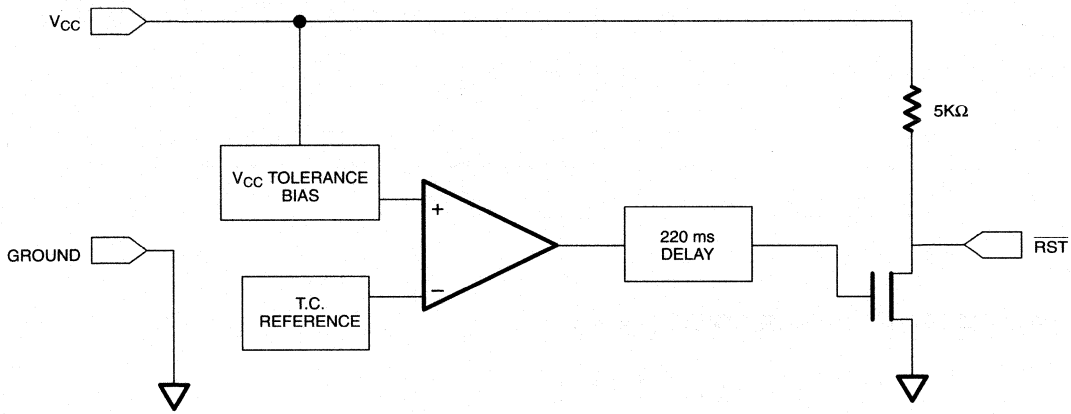
DESCRIPTION

The DS1816 EconoReset uses a precision temperature reference and comparator circuit to monitor the status of the power supply (V_{CC}). When an out-of-tolerance condition is detected, an internal power fail signal is generated which forces reset to the active state. When V_{CC} returns to an in-tolerance condition, the reset signal is kept in the active state for approximately 220 ms to allow the power supply and processor to stabilize.

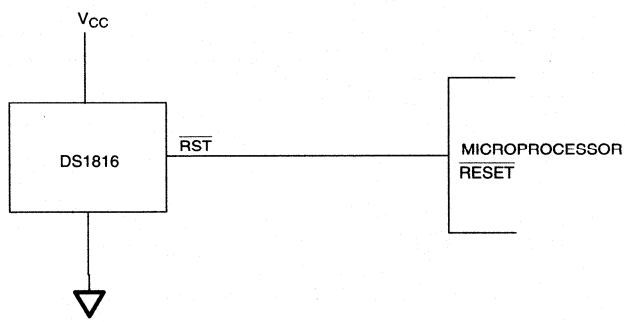
OPERATION – POWER MONITOR

The DS1816 provides the functions of detecting out-of-tolerance power supply conditions and warning a processor-based system of impending power failure. When V_{CC} is detected as out-of-tolerance, the $\overline{RST}$ signal is asserted. On power-up, $\overline{RST}$ is kept active for approximately 220 ms after the power supply has reached the selected tolerance. This allows the power supply and microprocessor to stabilize before $\overline{RST}$ is released.

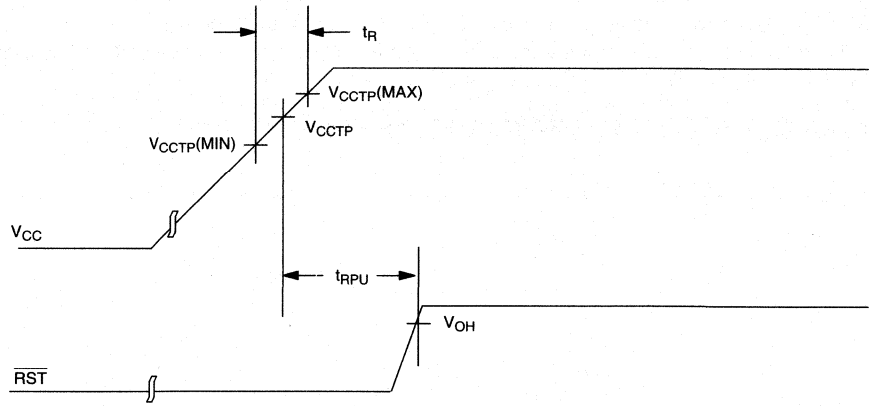
BLOCK DIAGRAM (OPEN-DRAIN OUTPUT) Figure 1



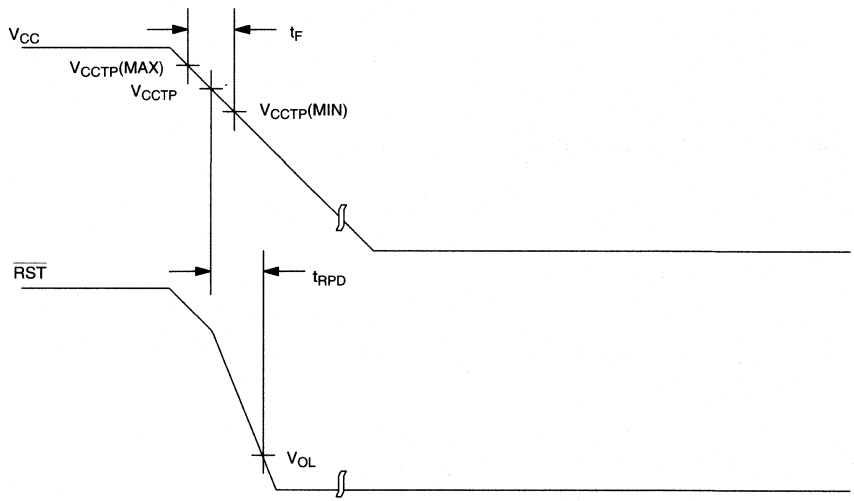
APPLICATION EXAMPLE Figure 2



TIMING DIAGRAM: POWER UP Figure 3



TIMING DIAGRAM: POWER DOWN Figure 4



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	–0.5V to +7.0V
Voltage on $\overline{RST}$ Relative to Ground	–0.5V to V_{CC} + 0.5V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	+260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	0.0		5.5	V	1

3

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 1.2V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Current @ 0.4V	I_{OL}	+10			mA	2,3
Operating Current V_{CC} < 5.5V	I_{CC}		28	35	µA	4
V_{CC} Trip Point (DS1816–10)	V_{CCTP}	2.80	2.88	2.97	V	1
V_{CC} Trip Point (DS1816–20)	V_{CCTP}	2.47	2.55	2.64	V	1
Internal Pull-Up Resistor	R_P	3.5	5.5	7.5	KΩ	
Output Capacitance	C_{OUT}			10	pF	

AC ELECTRICAL CHARACTERISTICS

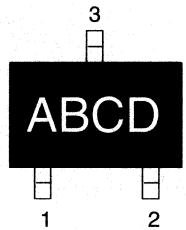
(0°C to 70°C; V_{CC} = 1.2V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RESET Active Time	t_{RST}	130	220	340	ms	5
V_{CC} Detect to $\overline{RST}$	t_{RPD}		2	5	µs	
V_{CC} Slew Rate (V_{CCTP} (MAX) to V_{CCTP} (MIN))	t_F	300			µs	
V_{CC} Slew Rate (V_{CCTP} (MIN) to V_{CCTP} (MAX))	t_R	0			ns	
V_{CC} Detect to $\overline{RST}$	t_{RPU}	130	220	340	ms	5,6

NOTES:

1. All voltages are referenced to ground.
2. Measured with $V_{CC} \geq 2.7V$.
3. A 1KΩ external resistor may be required in some applications for proper operation of the microprocessor reset control circuit.
4. Measured with $\overline{RST}$ output open.
5. Measured with $2.7V \leq V_{CC} \leq 3.3V$.
6. t_R = 5 µs.

PART MARKING CODES



"A", "B", &"C" represent the device type.

810 .... DS1810
811 .... DS1811
812 .... DS1812
813 .... DS1813
815 .... DS1815
816 .... DS1816
817 .... DS1817
818 .... DS1818

"D" represents the device tolerance.

A 5%
B 10%
C 15%
D 20%

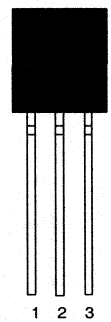
DALLAS SEMICONDUCTOR

DS1818
3.3V EconoReset with Pushbutton

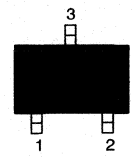
FEATURES

- Automatically restarts a microprocessor after power failure
- Monitors pushbutton for external override
- Maintains reset for 220 ms after V_{CC} returns to an in-tolerance condition
- Reduces need for discrete components
- Precision temperature-compensated voltage reference and voltage sensor
- Accurate 10% or 20% power monitoring
- Low-cost TO-92, surface-mount SOT-223, or space saving surface mount SOT–23 packages available
- Efficient open-drain output with internal 5.5 KΩ pull-up resistor

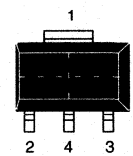
PIN ASSIGNMENT



TO-92 Package
See Mech. Drawings Section



SOT-23 Package



SOT-223 Package
See Mech. Drawings Section

PIN DESCRIPTIONS

TO–92

1	$\overline{RST}$	Active Low Reset Output
2	V_{CC}	Power Supply
3	GND	Ground

SOT–23

1	$\overline{RST}$	Active Low Reset Output
2	V_{CC}	Power Supply
3	GND	Ground

SOT–223

1	GND	Ground
2	$\overline{RST}$	Active Low Reset Output
3	GND	Ground
4	V_{CC}	Power Supply

DESCRIPTION

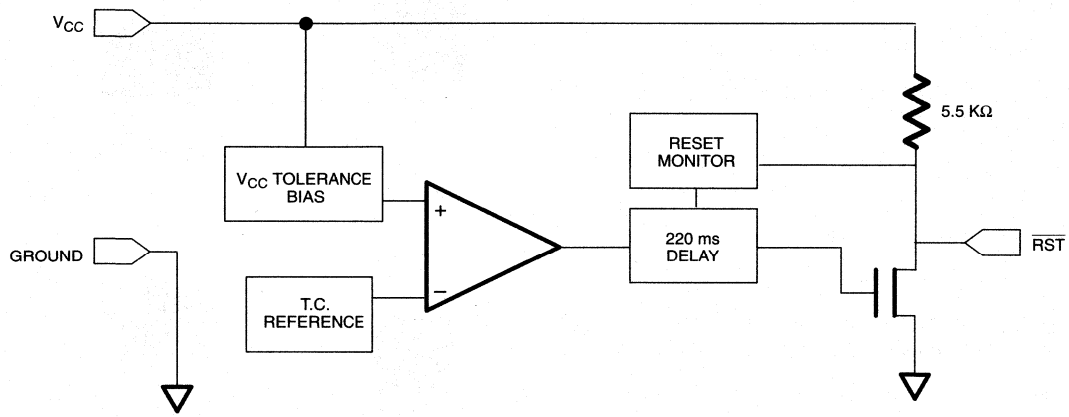
The DS1818 EconoReset uses a precision temperature compensated reference and comparator circuit to monitor the status of the power supply (V_{CC}). When an out-of-tolerance condition is detected, an internal power fail signal is generated which forces reset to the active state. When V_{CC} returns to an in-tolerance condition, the reset signal is kept in the active state for approximately 220 ms to allow the power supply and processor to stabilize.

The DS1818 also monitors a pushbutton on the reset output. If the reset line is pulled low, a reset is generated upon release and the DS1818 output will be held in reset output low for typically 220 ms.

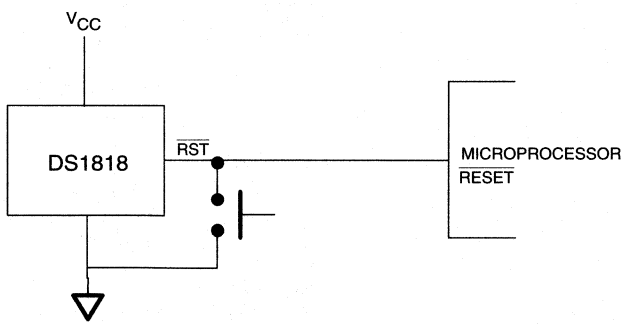
OPERATION – POWER MONITOR

The DS1818 provides the functions of detecting out-of-tolerance power supply conditions and warning a processor-based system of impending power failures. When V_{CC} is detected as out-of-tolerance, the $\overline{RST}$ signal is asserted. On power-up, $\overline{RST}$ is kept active for approximately 200 ms after the power supply has reached the selected tolerance. This allows the power supply and microprocessor to stabilize before $\overline{RST}$ is released.

BLOCK DIAGRAM (OPEN-DRAIN OUTPUT) Figure 1



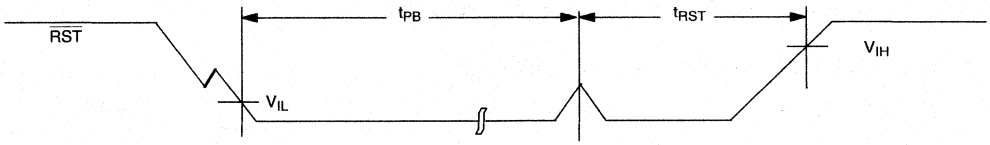
APPLICATION EXAMPLE Figure 2



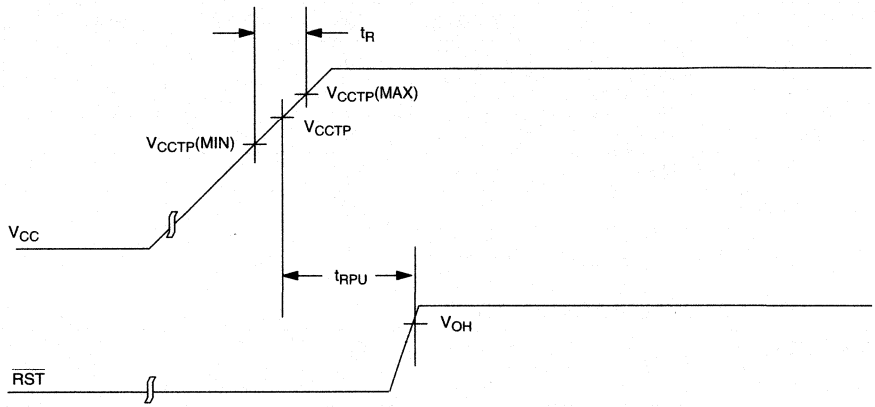
OPERATION – PUSHBUTTON RESET

The DS1818 provides a pushbutton switch for manual reset control. When the DS1818 is not in a reset cycle, a pushbutton reset can be generated by pulling the $\overline{RST}$ pin low for at least 1 µs. When the pushbutton is held low, the $\overline{RST}$ is forced active low and will remain active low for about 220 ms after the pushbutton is released. See Figure 2 for an application example and Figure 3 for the timing diagram.

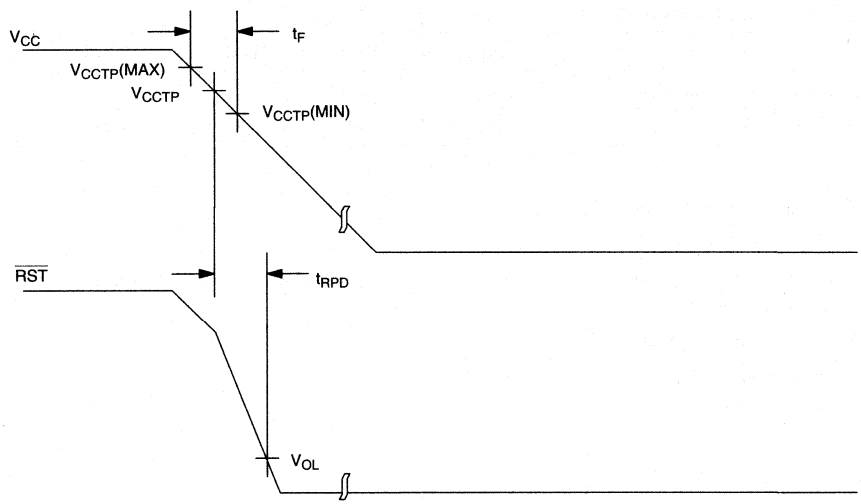
TIMING DIAGRAM: PUSHBUTTON RESET Figure 3



TIMING DIAGRAM: POWER UP Figure 4



TIMING DIAGRAM: POWER DOWN Figure 5



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	–0.5V to +7.0V
Voltage on $\overline{RST}$ Relative to Ground	–0.5V to V_{CC} + 0.5V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	+260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	1.0		5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 1.2V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Current @ 0.4V	I_{OL}	+10			mA	2,3
Operating Current V_{CC} <5.5V	I_{CC}		28	35	µA	4
V_{CC} Trip Point (DS1818-10)	V_{CCTP}	2.80	2.88	2.97	V	1
V_{CC} Trip Point (DS1818-20)	V_{CCTP}	2.47	2.55	2.64	V	1
Internal Pull-up Resistor	R_P	3.50	5.5	7.5	KΩ	
Output Capacitance	C_{OUT}			10	pF	

AC ELECTRICAL CHARACTERISTICS

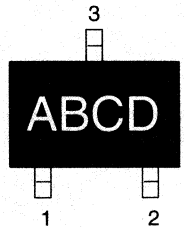
(0°C to 70°C; V_{CC} = 1.2V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RESET Active Time	t_{RST}	130	220	340	ms	5
V_{CC} Detect to $\overline{RST}$	t_{RPD}		2	5	µs	
V_{CC} Slew Rate (V_{CCTP}(MAX))	t_F	300			µs	
V_{CC} Slew Rate (V_{CCTP} (MIN))	t_R	0			ns	
V_{CC} Detect to $\overline{RST}$	t_{RPU}	130	220	340	ms	5,6
Pushbutton Detect to $\overline{RST}$	t_{PB}	1			µs	
Pushbutton Reset	t_{PBRST}	130	220	340	ms	5

NOTES:

1. All voltages are referenced to ground.
2. Measured with $V_{CC} \geq 2.7V$.
3. A 1KΩ external resistor may be required in some applications for proper operation of the microprocessor reset control circuit.
4. Measured with $\overline{RST}$ output open.
5. Measured with $2.7V \leq V_{CC} \leq 3.3V$.
6. t_R = 5 µs.

PART MARKING CODES



"A", "B", & "C" represents the Device Type.

- 810 DS1810
- 811 DS1811
- 812 DS1812
- 813 DS1813
- 815 DS1815
- 816 DS1816
- 817 DS1817
- 818 DS1818

3

PRODUCT PREVIEW

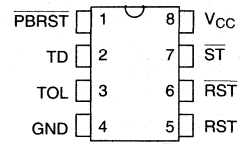
DALLAS SEMICONDUCTOR

DS1832
3.3 Volt MicroMonitor Chip

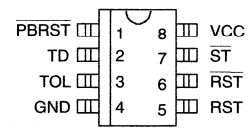
FEATURES

- Halts and restarts an out-of-control microprocessor
- Holds microprocessor in check during power transients
- Automatically restarts microprocessor after power failure
- Monitors pushbutton for external override
- Accurate 10% or 20% microprocessor power monitoring
- Eliminates need for discrete components
- 20% tolerance for use with 3.0 volt systems
- Pin compatible with the DS1232
- Low cost 8–pin DIP and 8–pin SOIC packages available
- Industrial temperature range of -40°C to +85°C available, designated N

PIN ASSIGNMENT



DS1832 8-Pin DIP (300 Mil)
See Mech. Drawings Section



DS1832 8-Pin SOIC (150 Mil)
See Mech. Drawings Section

PIN DESCRIPTION

$\overline{PBRST}$	–	Pushbutton Reset Input
TD	–	Time Delay Set
TOL	–	Selects 10% or 20% V_{CC} Detect
GND	–	Ground
RST	–	Active High Reset Output
$\overline{RST}$	–	Active Low Reset Output
$\overline{ST}$	–	Strobe Input
V_{CC}	–	Power Supply

DESCRIPTION

The DS1832 3.3 Volt MicroMonitor monitors three vital conditions for a microprocessor: power supply, software execution, and external override. First, a precision temperature–compensated reference and comparator circuit monitors the status of V_{CC}. When an out–of–tolerance condition occurs, an internal power fail signal is generated which forces the resets to an active state. When V_{CC} returns to an in–tolerance condition, the reset signals are kept in the active state for a minimum of 250 ms to allow the power supply and processor to stabilize.

The second function the DS1832 performs is pushbutton reset control. The DS1832 debounces the pushbutton input and guarantees an active reset pulse width of 250 ms minimum. The third function is a watchdog timer. The DS1832 has an internal timer that forces the reset signals to the active state if the strobe input is not driven low prior to time–out. The watchdog timer function can be set to operate on time–out settings of approximately 150 ms, 600 ms, or 1.2 seconds.

OPERATION - POWER MONITOR

The DS1832 detects out-of-tolerance power supply conditions and warns a processor-based system of impending power failure. When V_{CC} falls below a preset level as defined by TOL, the V_{CC} comparator outputs the signals RST and $\overline{RST}$. When TOL is connected to ground, the RST and $\overline{RST}$ signals become active as V_{CC} falls below 2.98 volts. When TOL is connected to V_{CC}, the RST and $\overline{RST}$ signals become active as V_{CC} falls below 2.64 volts. The RST and $\overline{RST}$ are excellent control signals for a microprocessor, as processing is stopped at the last possible moments of valid V_{CC}. On power-up, RST and $\overline{RST}$ are kept active for a minimum of 250 ms to allow the power supply and processor to stabilize.

OPERATION - PUSHBUTTON RESET

The DS1832 provides an input pin for direct connection to a pushbutton reset (see Figure 2). The pushbutton reset input requires an active low signal. Internally, this input is debounced and timed such that RST and $\overline{RST}$ signals of at least 250 ms minimum are generated. The 250 ms delay commences as the pushbutton reset input is released from the low level.

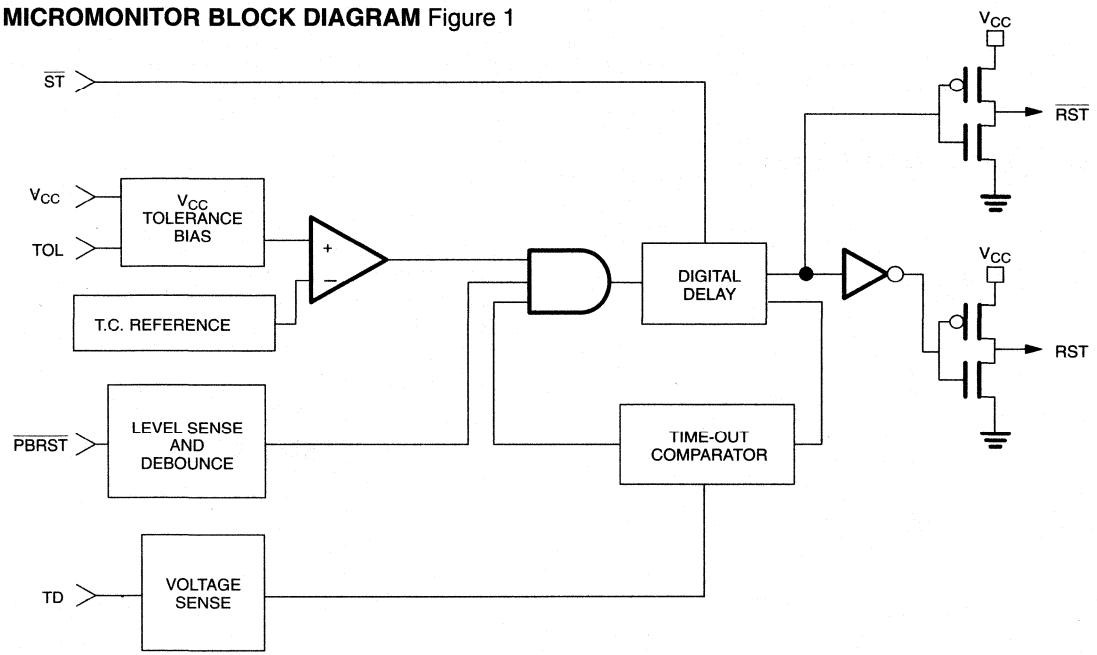
OPERATION - WATCHDOG TIMER

The watchdog timer function forces RST and $\overline{RST}$ signals active when the $\overline{ST}$ input is not clocked within the predetermined time period. The timeout period is determined by the condition of the TD pin. if TD is connected to ground the minimum watchdog timeout would be 62.5 ms, TD floating would yield a minimum timeout of 250 ms, and TD connected to V_{CC} would provide a timeout of 500 ms minimum. Timeout of the watchdog starts when RST and $\overline{RST}$ become inactive. If a high–to–low transition occurs on the $\overline{ST}$ input pin prior to time–out, the watchdog timer is reset and begins to time–out again. If the watchdog timer is allowed to time–out, then the RST and $\overline{RST}$ signals are driven active for a minimum of 250 ms. The $\overline{ST}$ input can be derived from many microprocessor outputs. The most typical signals used are the microprocessor address signals, data signals or control signals. When the microprocessor functions normally, these signals would, as a matter of routine, cause the watchdog to be reset prior to time–out. To guarantee that the watchdog timer does not time–out, a high–to–low transition must occur at or less than the minimum times shown in Table 1. A typical circuit example is shown in Figure 4.

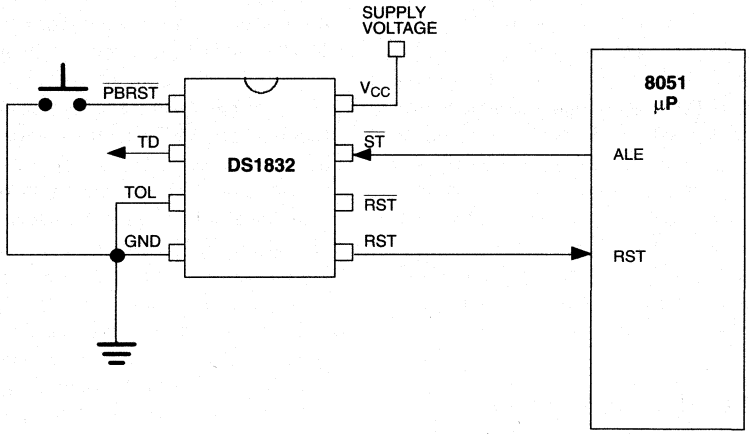
The DS1832 watchdog function cannot be disabled. The watchdog strobe input must be strobed to avoid a watchdog timeout and reset.

3

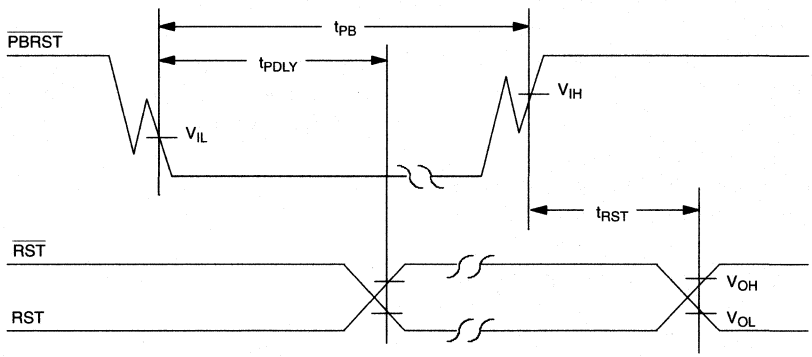
MICROMONITOR BLOCK DIAGRAM Figure 1



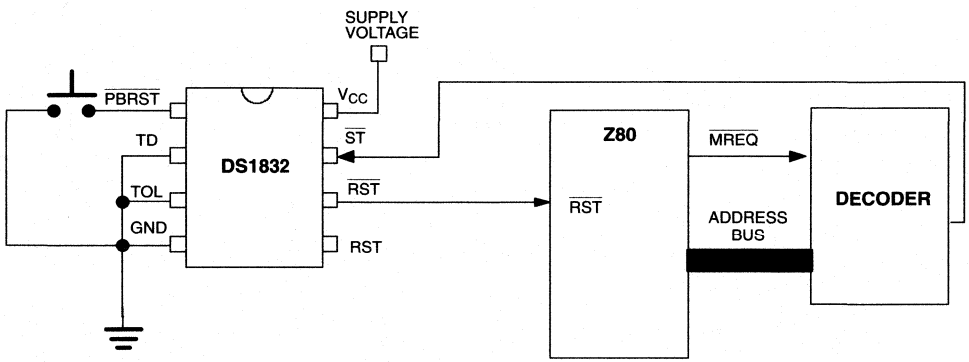
PUSHBUTTON RESET Figure 2



TIMING DIAGRAM: PUSHBUTTON RESET Figure 3



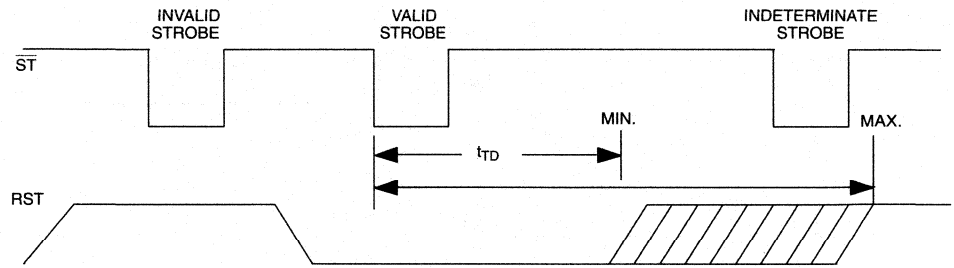
WATCHDOG TIMER Figure 4



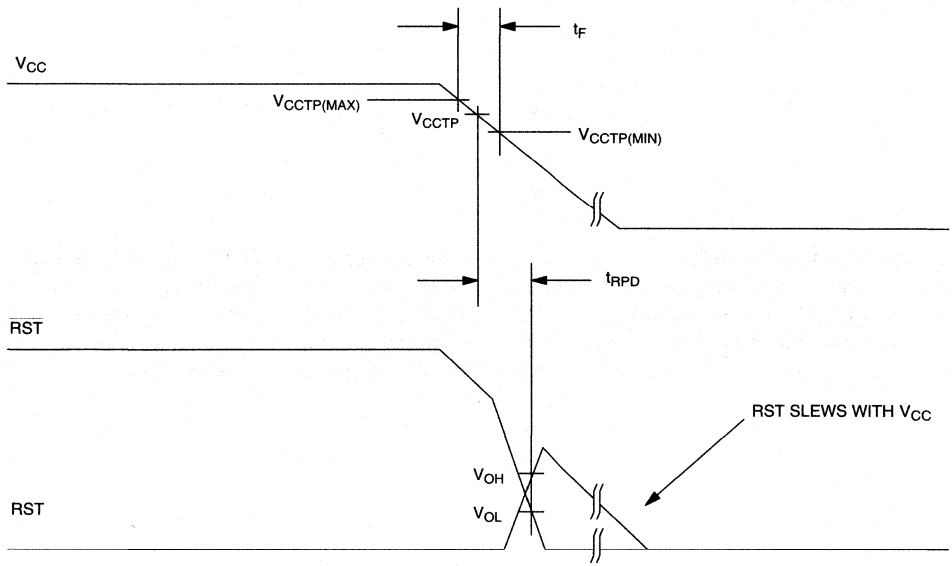
WATCHDOG TIME-OUTS Table 1

TD	TIME-OUT		
	MIN	TYP	MAX
GND	62.5 ms	150 ms	250 ms
Float	250 ms	600 ms	1000 ms
V_{CC}	500 ms	1200 ms	2000 ms

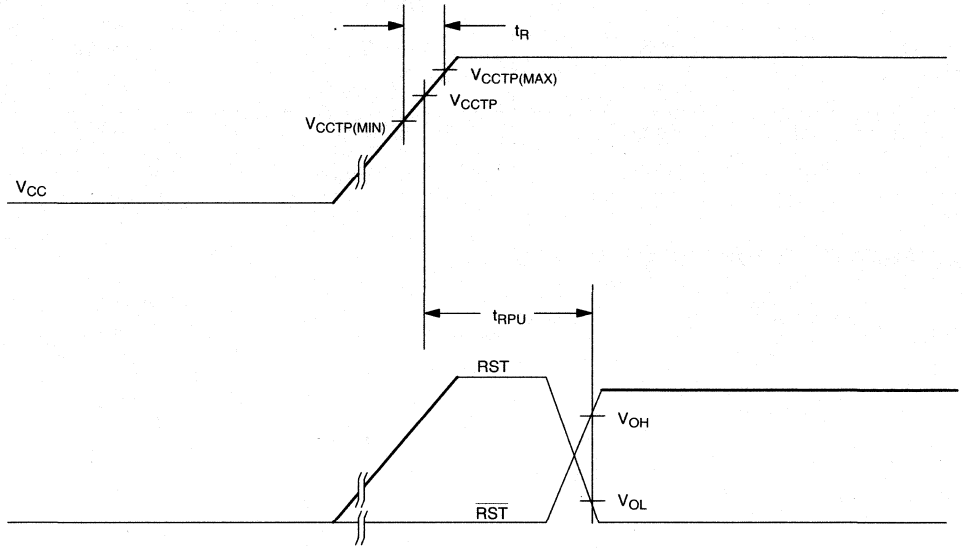
TIMING DIAGRAM: STROBE INPUT Figure 5



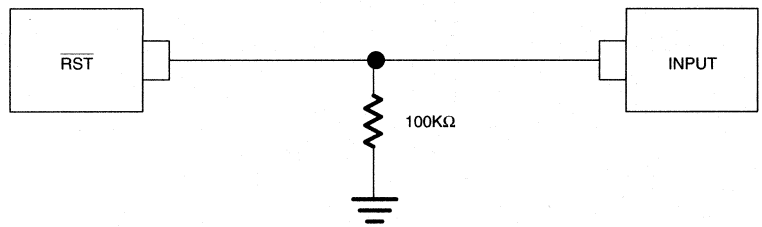
TIMING DIAGRAM: POWER DOWN Figure 6



TIMING DIAGRAM: POWER UP Figure 7



$\overline{RST}$ VALID TO 0 VOLTS V_{CC} Figure 8



OUTPUT VALID CONDITIONS

The $\overline{RST}$ output uses a push–pull output which can maintain a valid output down to 0.8 volts V_{CC}. To sink current below 0.8 volts a resistor can be connected from $\overline{RST}$ to Ground (see Figure 8). This arrangement will maintain a valid value on $\overline{RST}$ during both power up and power down but will draw current when $\overline{RST}$ is in the high state. A value of about 100KΩ should be adequate in most situations. The output with a resistor pull–down can maintain a valid reset down to V_{CC} equal to 0 volts.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +7.0V
Voltage on I/O Relative to Ground	-0.5V to V_{CC} + 0.5V
Operating Temperature	–40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	1.0		5.5	V	1
ST and PBRST Input High Level	V_{IH}	2.0		V_{CC}+0.3	V	1, 3
		V_{CC}–0.4				1, 4
$\overline{ST}$ and $\overline{PBRST}$ Input Low Level	V_{IL}	–0.3		0.5	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=1.2V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} Trip Point (TOL = GND)	V_{CCTP}	2.80	2.88	2.97	V	1
V_{CC} Trip Point (TOL = V_{CC})	V_{CCTP}	2.47	2.55	2.64	V	1
Input Leakage	I_{IL}	-1.0		+1.0	µA	2
Output Current @ 2.4V	I_{OH}		350		µA	3
Output Current @ 0.4V	I_{OL}	10			mA	3
Output Voltage @ -500 uA	V_{OH}	V_{CC}–0.3V	V_{CC}–0.1V		V	4
Operating Current	I_{CC}			35	µA	5

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 1.2V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{PBRST}$ = V_{IL}	t_{PB}	20			ms	
RESET Active Time	t_{RST}	250	610	1000	ms	
$\overline{ST}$ Pulse Width	t_{ST}	20			ns	6, 7
V_{CC} Detect to RST and $\overline{RST}$	t_{RPD}		5	8	µs	8
V_{CC} Slew Rate	t_F	20			µs	
V_{CC} Detect to RST and $\overline{RST}$	t_{RPU}	250	610	1000	ms	9
V_{CC} Slew Rate	t_R	0			ns	
$\overline{PBRST}$ Stable Low to $\overline{RST}$ and RST	t_{DLY}			20	ms	

NOTES:

1. All voltages referenced to ground.
2. $\overline{PBRST}$ is internally pulled up to V_{CC} with an internal impedance of 40KΩ typical.
3. Measured with $V_{CC} \geq 2.7V$.
4. Measured with $V_{CC} < 2.7V$.
5. Measured with outputs open, $V_{CC} \leq 3.6$ volts, and all inputs at V_{CC} or Ground.
6. Must not exceed t_{TD} minimum.
7. The Watchdog cannot be disabled it must be strobed to avoid resets.
8. Noise Immunity – Pulses < 2 µs at V_{CCTP} minimum will not cause a reset.
9. t_R = 5 µs.

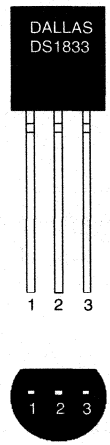
DALLAS SEMICONDUCTOR

DS1833
5V EconoReset

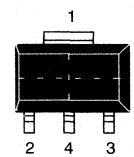
FEATURES

- Automatically restarts microprocessor after power failure
- Maintains active–high reset for 350 ms after V_{CC} returns to an in-tolerance condition
- Accurate 5%, 10% or 15% microprocessor 5V power supply monitoring
- Reduces need for discrete components
- Precision temperature-compensated voltage reference and voltage sensor
- Low-cost TO-92 package or surface mount SOT-223 package
- Internal 5K pull-up resistor
- Operating temperature of –40°C to +85°C

PIN ASSIGNMENT



TO-92 Package
See Mech. Drawings Section



SOT-223 Package
See Mech. Drawings Section

PIN DESCRIPTION

Pin 1	Ground
Pin 2	Reset
Pin 3	V_{CC}
Pin 4	Ground (SOT–223 only)

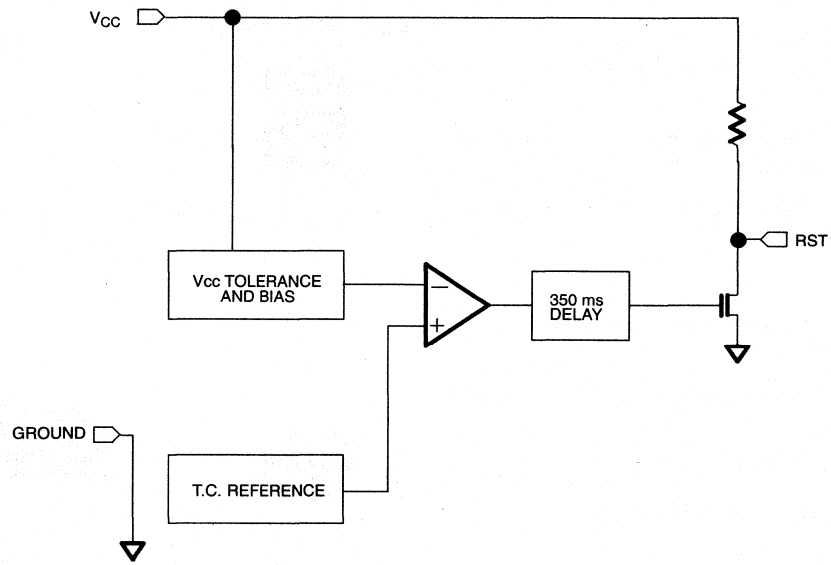
DESCRIPTION

The DS1833 EconoReset uses a precision temperature compensated reference and comparator circuit to monitor the status of the power supply (V_{CC}). When an out-of-tolerance condition is detected, an internal power fail signal is generated which forces reset to the active (high) state. When V_{CC} returns to an in-tolerance condition, the reset signal is kept in the active state for approximately 350 ms to allow the power supply and processor to stabilize.

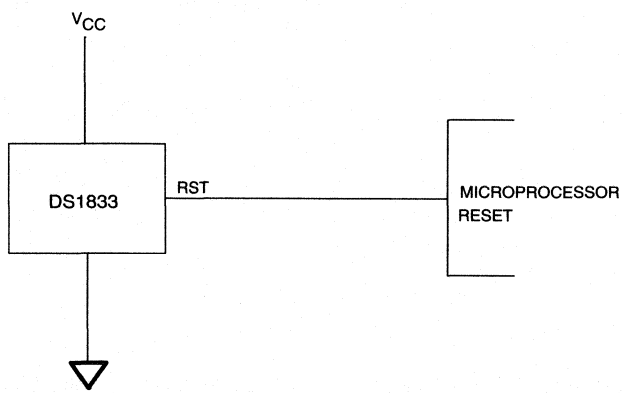
OPERATION - POWER MONITOR

The DS1833 provides the functions of detecting out-of-tolerance power supply conditions and warning a processor-based system of impending power failure. When V_{CC} is detected as out-of-tolerance, as defined by the tolerance of the part selected, the RST signal is asserted. On power-up, RST is kept active for approximately 350 ms after the power supply has reached the selected tolerance. This allows the power supply and microprocessor to stabilize before RST is released.

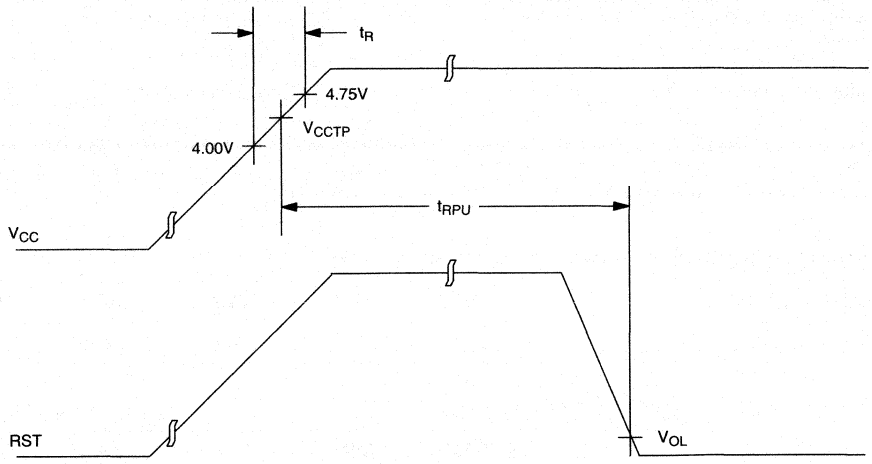
BLOCK DIAGRAM Figure 1



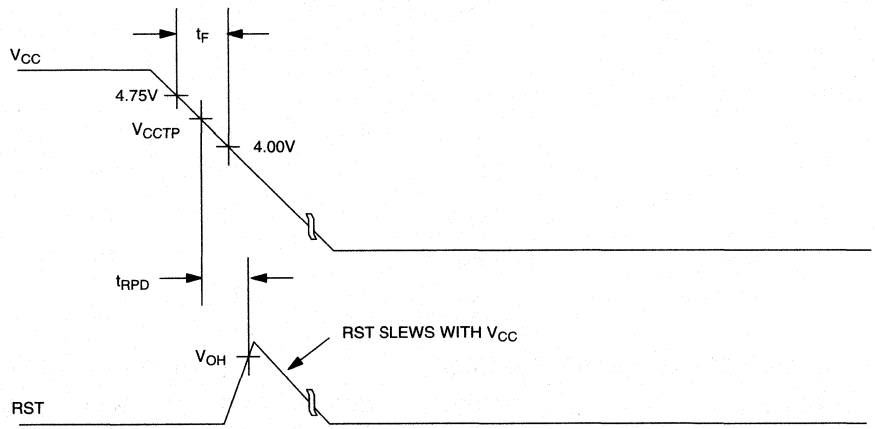
APPLICATION EXAMPLE Figure 2



POWER UP Figure 3



POWER DOWN Figure 4



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	–0.5V to +7.0V
Voltage on I/O Relative to Ground	–0.5V to V_{CC} + 0.5V
Operating Temperature	–40°C to +85°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(–40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	1.2	5.0	5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Low Level @ RST	V_{OL}			0.4	V	1
Output Voltage @ –500 µA	V_{OH}	V_{CC}–0.5V	V_{CC}–0.1V		V	1
Output Current @ 2.4V	I_{OH}		350		µA	
Output Current @ 0.4V	I_{OL}	+10			mA	
Operating Current	I_{CC}		1.5	2	mA	
V_{CC} Trip Point 5%	V_{CCTP1}	4.5	4.625	4.74	V	1
V_{CC} Trip Point 10%	V_{CCTP2}	4.25	4.375	4.49	V	1
V_{CC} Trip Point 15%	V_{CCTP3}	4.0	4.125	4.24	V	1
Output Capacitance	C_{OUT}			10	pF	
Internal Pull-Up Resistor	R_P	3.75	5	6.25	KΩ	

AC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Reset Active Time	t_{RST}	250	350	450	ms	
V_{CC} Detect to RST	t_{RPD}			100	ns	
V_{CC} Slew Rate (4.75V - 4.00V)	t_F	300			µs	
V_{CC} Slew Rate (4.00V - 4.75V)	t_R	0			ns	
V_{CC} detect to RST	t_{RPU}	250	350	450	ms	

NOTE:

1. All voltages are referenced to ground.

ECONORESET SELECTION GUIDE

		VCC TRIP POINT			PUSHBUTTON DETECT		
		MIN	TYP	MAX	MIN	TYP	MAX
5V	DS1233-15	4.0	4.125	4.24	2.4	–	3.3
	DS1233-10	4.25	4.375	4.49	2.4	–	3.3
	DS1233-5	4.5	4.625	4.75	2.4	–	3.3
	DS1233D–15	4.0	4.125	4.24	N/A		N/A
	DS1233D–10	4.25	4.375	4.49	N/A		N/A
	DS1233D–5	4.5	4.625	4.75	N/A		N/A
	DS1833–15	4.0	4.125	4.24	N/A		N/A
	DS1833–10	4.25	4.375	4.49	N/A		N/A
	DS1833–5	4.5	4.625	4.75	N/A		N/A
3.3V	DS1233A-15	2.64	2.72	2.80	1.8	–	3.0
	DS1233A-10	2.8	2.88	2.97	1.8	–	3.0

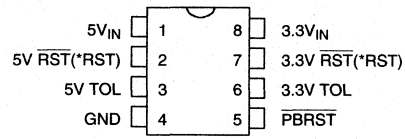
DALLAS SEMICONDUCTOR

DS1834/A/D
Dual EconoReset with Pushbutton

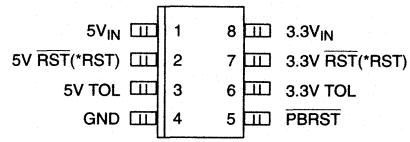
FEATURES

- 5 volt power–on reset
- 3.3 volt power–on reset
- Internal power is drawn from higher of either the 5V IN input or the 3.3V IN input
- Excellent for systems designed to operate with dual power supplies
- Asserts resets during power transients
- Pushbutton reset input for system override
- Maintains reset for 350 ms after V_{CC} returns to an in–tolerance condition
- Reduces need for discrete components
- Precision temperature–compensated voltage reference and voltage sensor
- 8–pin DIP, 8–pin SOIC, or space saving 8–pin µ–SOP available
- CMOS output for low current operation on the DS1834 and DS1834D
- Operating temperature of –40°C to +85°C

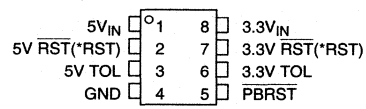
PIN ASSIGNMENT



DS1834 8–PIN DIP
(300 MIL)



DS1834 8–PIN SOIC
(150 MIL)



DS1834D 8–PIN µ–SOP
(118 MIL)

See Mech. Drawings
Section

PIN DESCRIPTION

$5V_{IN}$	–	5V Power Supply Input
5V RST(*RST)	–	5V Reset Output
5V TOL	–	Selects 5V Input Tolerance
GND	–	Ground
PBRST	–	Pushbutton Reset
3.3V TOL	–	Selects 3.3V Input Tolerance
3.3V RST(*RST)	–	3.3V Reset Output
$3.3V_{IN}$	–	3.3V Power Supply Input

*DS1834D Active High Reset

DESCRIPTION

The DS1834 Dual EconoResets monitors three vital system conditions: 5 volt supply, 3.3 volt supply, and an external override. First a precision temperature reference and comparator circuit monitors the status of the 5 volt supply and the 3.3 volt supply. When an out–of–tolerance condition is detected, an internal power fail signal is generated which forces the reset of the affected supply to an active state.

Lastly, the DS1834 supports an external reset via an internally debounced pushbutton input. When the pushbutton is pulled low both resets will be asserted for approximately 350 ms after the pushbutton is released.

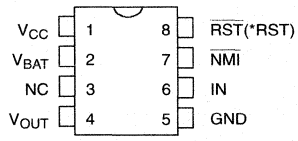
DALLAS SEMICONDUCTOR

DS1836A/B/C/D
3.3V/5V MicroManager

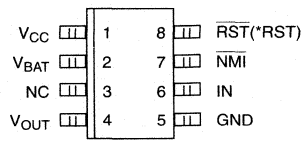
FEATURES

- 5 volt or 3.3 volt power–on reset
- True 3 volt operation power switch
- Switches to battery at 2.6 volts
- Excellent for systems designed to operate with dual power supplies
- Asserts resets during power transients
- Maintains reset for 350 ms after V_{CC} returns to an in–tolerance condition
- Reduces need for discrete components
- Precision temperature–compensated voltage reference and voltage sensor
- 8–pin DIP or space saving 8–pin SOIC surface mount available
- CMOS reset output for low current operation
- Operating temperature of –40°C to +85°C
- Perfect for PIC microprocessor applications

PIN ASSIGNMENT



8–PIN DIP
(300 MIL)



8–PIN SOIC
(150 MIL)

See Mech. Drawings Section

DS1836A/B (*DS1836C/D)

PIN DESCRIPTION

V_{CC}	–	Power Supply Input
V_{BAT}	–	Battery Supply Input
NC	–	No Connect
V_{OUT}	–	Power Supply Output
GND	–	Ground
IN	–	Sense Input
$\overline{NMI}$	–	Non–maskable Interrupt
$\overline{RST}$(*RST)	–	Reset Output

DESCRIPTION

The DS1836 MicroManager performs three vital system functions. First a precision temperature compensated reference and comparator circuit monitors the status of the voltage on V_{CC} and when an out–of–tolerance condition is detected, an internal power fail signal is generated which forces the reset active. If V_{CC} continues to degrade it switches to the battery supply when V_{CC} drops below 2.6 volts. When V_{CC} exceeds 2.8 volts; V_{OUT} will again be supplied from V_{CC}. Reset will remain active for 350 ms after V_{CC} returns to an in–tolerance condition.

Lastly, the DS1836 supports a sense input that sends a non–maskable interrupt whenever the sense input drops below 1.25 volts.

DIGITAL POTENTIOMETERS

4

DALLAS SEMICONDUCTOR

DS1267
Dual Digital Potentiometer Chip

FEATURES

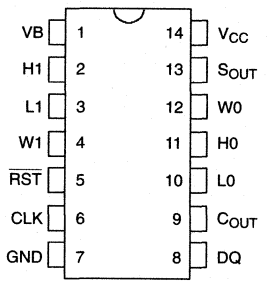
- Ultra–low power consumption, quiet, pumpless design
- Two digitally controlled, 256–position potentiometers
- Serial port provides means for setting and reading both potentiometers
- Resistors can be connected in series to provide increased total resistance
- 14–pin DIP, 16–pin SOIC, 20–pin TSSOP packages
- Resistive elements are temperature compensated to ±0.3 LSB relative linearity
- Standard resistance values:
  - DS1267–10 ~ 10KΩ
  - DS1267–50 ~ 50KΩ
  - DS1267–100 ~ 100KΩ
- Temperature:
  - Commercial: 0°C to 70°C
  - Industrial: –40°C to 85°C

DESCRIPTION

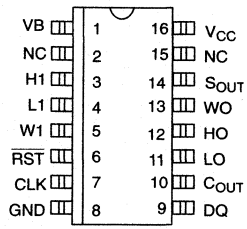
The DS1267 consist of two digitally controlled solid–state potentiometers. Each potentiometer is composed of 256 resistive sections. Between each resistive section and both ends of the potentiometer are tap points which are accessible to the wiper. The position of the wiper on the resistive array is set by an 8–bit value that controls which tap point is connected to the wiper output. Communication and control of the device is accomplished via a 3–wire serial port interface. This interface allows the device wiper position to be read or written.

Both potentiometers can be connected in series (or stacked) for an increased total resistance with the same resolution. For multiple device–single processor environments, the DS1267 can be cascaded or daisy chained. This feature provides for control of multiple devices over a single 3–wire bus.

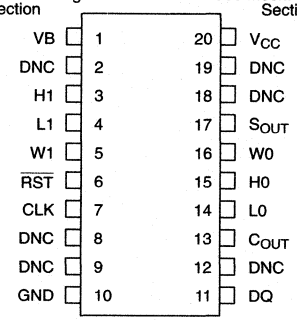
PIN ASSIGNMENT



14–Pin DIP (300 Mil)
See Mech. Drawings Section



16–Pin SOIC (300 Mil)
See Mech. Drawings Section



20–Pin TSSOP (173 Mil)

PIN DESCRIPTION

L0, L1	– Low End of Resistor
H0, H1	– High End of Resistor
W0, W1	– Wiper Terminal of Resistor
V_B	– Substrate Bias Voltage
S_{OUT}	– Stacked Configuration Output
$\overline{RST}$	– Serial Port Reset Input
DQ	– Serial Port Data Input
CLK	– Serial Port Clock Input
C_{OUT}	– Cascade Port Output
V_{CC}	– +5 Volt Supply
GND	– Ground
NC	– No Internal Connection
DNC	– Do Not Connect

The DS1267 is offered in three standard resistance values which include 10K, 50K, and 100K ohm versions. Commercial and industrial temperature parts are also available. Available packages for the device include a 14–pin DIP, 16–pin SOIC, and 20–pin TSSOP.

OPERATION

The DS1267 contains two 256–position potentiometers whose wiper positions are set by an 8–bit value. These two 8–bit values are written to a 17–bit I/O shift register which is used to store the two wiper positions and the stack select bit when the device is powered. A block diagram of the DS1267 is presented in Figure 1.

Communication and control of the DS1267 is accomplished through a 3–wire serial port interface that drives an internal control logic unit. The 3–wire serial interface consists of the three input signals: $\overline{RST}$, CLK, and DQ.

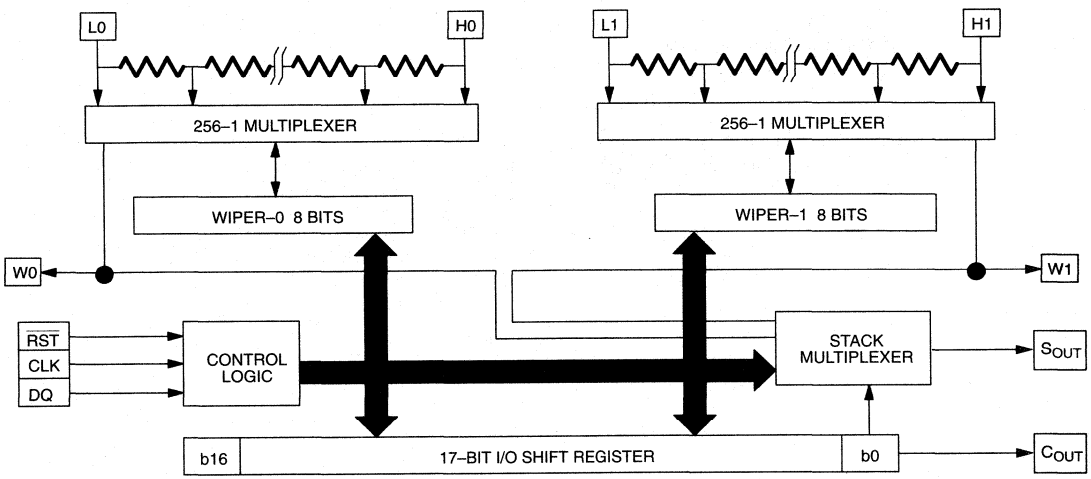
The $\overline{RST}$ control signal is used to enable the 3–wire serial port operation of the device. The $\overline{RST}$ signal is an active high input and is required to begin any communication to the DS1267. The CLK signal input is used to provide timing synchronization for data input and output. The DQ signal line is used to transmit potentiometer wiper settings and the stack select bit configuration to the 17–bit I/O shift register of the DS1267.

Figure 9(a) presents the 3–wire serial port protocol. As shown, the 3–wire port is inactive when the $\overline{RST}$ signal input is low. Communication with the DS1267 requires the transistion of the $\overline{RST}$ input from a low state to a high state. Once the 3–wire port has been activated, data is entered into the part on the low to high transistion of the CLK signal inputs. Three–wire serial timing requirements are provided in the timing diagrams of Figure 9(b),(c).

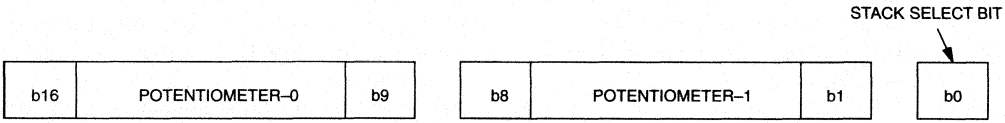
Data written to the DS1267 over the 3–wire serial interface is stored in the 17–bit I/O shift register (see Figure 2). The 17–bit I/O shift register contains both 8–bit potentiometer wiper position values and the stack select bit. The composition of the I/O shift register is presented in Figure 2. Bit 0 of the I/O shift register contains the stack select bit. This bit will be discussed in the section entitled Stacked Configuration. Bits 1 through 8 of the I/O shift register contain the potentiometer–1 wiper position value. Bit 1 will contain the MSB of the wiper setting for potentiometer–1 and bit 8 the LSB for the wiper setting. Bits 9 through 16 of the I/O shift register contain the value of the potentiometer–0 wiper position with the MSB for the wiper position occupying bit 9 and the LSB bit 16.

4

DS1267 BLOCK DIAGRAM Figure 1



I/O SHIFT REGISTER Figure 2



17–BIT I/O SHIFT REGISTER

Transmission of data always begins with the stack select bit followed by the potentiometer–1 wiper position value and lastly the potentiometer–0 wiper position value.

When wiper position data is to be written to the DS1267, 17 bits (or some integer multiple) of data should always be transmitted. Transactions which do not send a complete 17–bits (or multiple) will leave the register incomplete and possibly an error in the desired wiper positions.

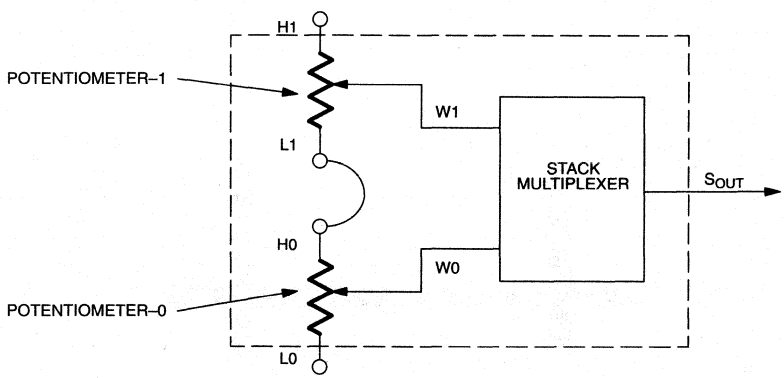
After a communication transaction has been completed the $\overline{RST}$ signal input should be taken to a low state to prevent any inadvertent changes to the device shift register. Once $\overline{RST}$ has reached a low state, the contents of the I/O shift register are loaded into the respective multiplexers for setting wiper position. A new wiper position will only engage after a $\overline{RST}$ transition to the inactive state. On device power–up the DS1267 wiper positions will be set at 50% of the total resistance or binary value 1000 0000.

STACKED CONFIGURATION

The potentiometers of the DS1267 can be connected in series as shown in Figure 3. This is referred to as the stacked configuration and allows the user to double the total end–to–end resistance of the part. The resolution of the combined potentiometers will remain the same as a single potentiometer but with a total of 512 wiper positions available. Device resolution is defined as Rtot/256 (per potentiometer); where Rtot equals the total potentiometer resistance.

The wiper output for the combined stacked potentiometer will be taken at the S_{OUT} pin, which is the multiplexed output of the wiper of potentiometer–0 (W0) or potentiometer–1 (W1). The potentiometer wiper selected at the S_{OUT} output is governed by the setting of the stack select bit (bit 0) of the 17–bit I/O shift register. If the stack select bit has value 0, the multiplexed output, S_{OUT}, will be that of the potentiometer–0 wiper. If the stack select bit has value 1, the multiplexed output, S_{OUT}, will be that of the potentiometer–1 wiper.

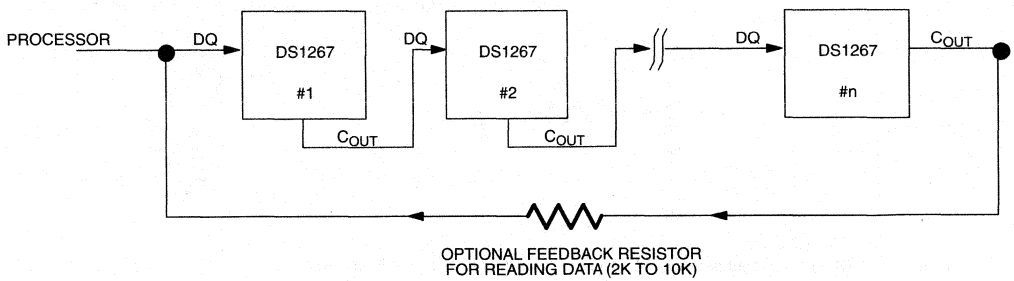
STACKED CONFIGURATION Figure 3



CASCADE OPERATION

A feature of the DS1267 is the ability to control multiple devices from a single processor. Multiple DS1267s can be linked or daisy chained as shown in Figure 4. As a data bit is entered into the I/O shift register of the DS1267 a bit will appear at the C_{OUT} output after a minimum delay of 50 nanoseconds. The stack select bit of the DS1267 will always be the first out the part at the beginning of a transaction. Additionally the C_{OUT} pin is always active regardless of the state of $\overline{RST}$. This allows one to read the I/O shift register without changing its value.

CASCADING MULTIPLE DEVICES Figure 4



The C_{OUT} output of the DS1267 can be used to drive the DQ input of another DS1267. When connecting multiple devices, the total number of bits transmitted is always 17 times the number of DS1267s in the daisy chain.

An optional feedback resistor can be placed between the C_{OUT} terminal of the last device and the first DS1267 DQ input thus allowing the controlling processor to read, as well as, write data, or circularly clock data through the daisy chain. The value of the feedback or isolation resistor should be in the range from 1K to 10K ohms.

When reading data via the C_{OUT} pin and isolation resistor, the DQ line is left floating by the reading device. When $\overline{RST}$ is driven high, bit 17 is present on the C_{OUT} pin, which is fed back to the input DQ pin through the isolation resistor. When the CLK input transitions low to high, bit 17 is loaded into the first position of the I/O shift register and bit 16 becomes present on C_{OUT} and DQ of the next device. After 17 bits (or 17 times the number of DS1267s in the daisy chain), the data has shifted completely around and back to its original position. When $\overline{RST}$ transitions to the low state to end data transfer, the value (the same as before the read occurred) is loaded into the wiper–0, wiper–1, and stack select bit I/O register.

ABSOLUTE AND RELATIVE LINEARITY

Absolute linearity is defined as the difference between the actual measured output voltage and the expected output voltage. Figure 5 presents the test circuit used to measure absolute linearity. Absolute linearity is given in terms of a minimum increment or expected output when the wiper is moved one position. In the case of the test circuit, a minimum increment (MI) or one LSB would equal 10/512 volts. The equation for absolute linearity is given as follows:

(1) ABSOLUTE LINEARITY

$$AL=\{V_O(actual) - V_O(expected)\}/MI$$

Relative Linearity is a measure of error between two adjacent wiper position points and is given in terms of MI by equation (2).

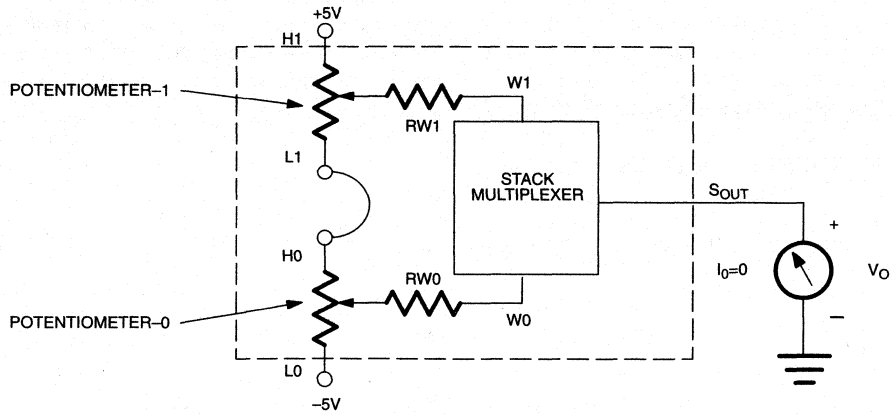
(2) RELATIVE LINEARITY

$$RL=\{V_O(n+1) - V_O(n)\}/MI$$

Figure 6 is a plot of absolute linearity and relative linearity versus wiper position for the DS1267 at 25°C. The specification for absolute linearity of the DS1267 is ±0.75 MI typical. The specification for relative linearity of the DS1267 is ±0.3 MI typical.

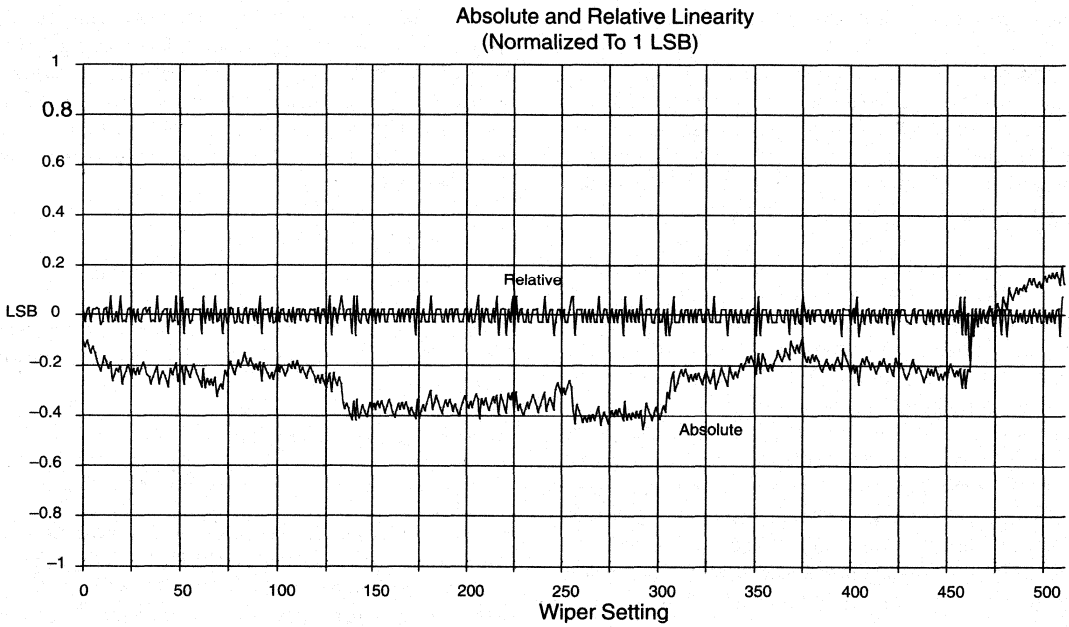
4

LINEARITY MEASUREMENT CONFIGURATION Figure 5



NOTE:
In this setup, a ±2% delta in total resistance R0 to R1 would cause a ±2.5 MI error.

DS1267 ABSOLUTE AND RELATIVE LINEARITY Figure 6



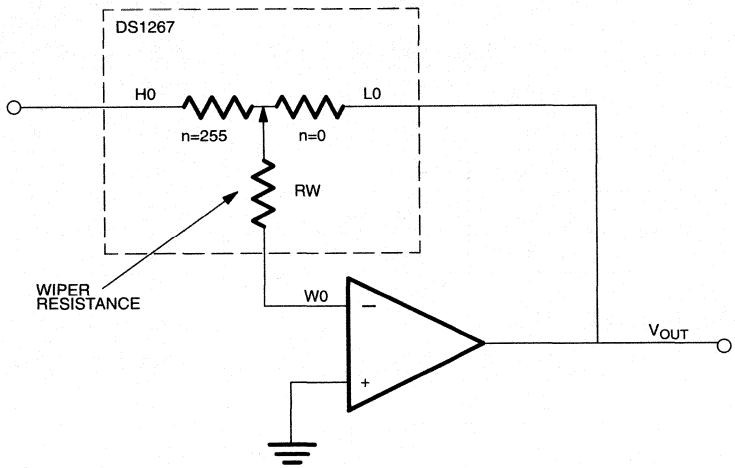
TYPICAL APPLICATION CONFIGURATIONS

Figures 7 and 8 show two typical application configurations for the DS1267. By connecting the wiper terminal of the part to a high impedance load, the effects of the wiper resistance is minimized, since the wiper resistance can vary from 400 to 1000 ohms depending on wiper voltage. Figure 7 presents the device connected in an inverting varible gain amplifier. The gain of the circuit on Figure 7 is given by the following equation:

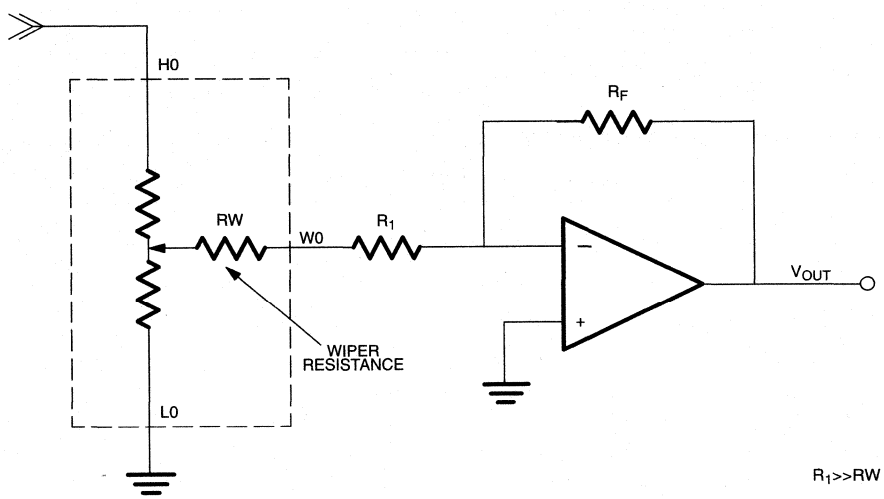
$$Av = -n/(255-n); \text{ where } n = 0 \text{ to } 255$$

Figure 8 shows the deivce operaing in a fixed gain attenuator where the potentiometer is used to attenuate an incoming signal. Note the resistance R1 is chosen to be much greater than the wiper resistance to minimize its effect on circuit gain.

INVERTING VARIABLE GAIN AMPLIFIER Figure 7



FIXED GAIN ATTENUATOR Figure 8



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground (VB=GND)	–1.0V to +7.0V
Voltage on Resistor Pins when VB=–5.5V	–5.5V to +7.0V
Voltage on V_B	–5.5 to GND
Operating Temperature	0°C to 70°C commercial; –40°C to +85°C industrial
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C; V_{CC}=5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5		5.5	V	1
Input Logic 1	V_{IH}	2.0		V_{CC}+0.5	V	1, 2
Input Logic 0	V_{IL}	–0.5		+0.8	V	1, 2
Substrate Bias	V_B	–5.5		GND	V	1
Resistor Inputs	L, H, W	V_B–0.5		V_{CC}+0.5	V	2

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}		22	650	µA	12
Input Leakage	I_{LI}	–1		+1	µA	
Wiper Resistance	R_W		400	1000	Ω	
Wiper Current	I_W			1	mA	
Output Leakage	I_{LO}	–1		+1	µA	
Logic 1 Output @ 2.4 Volts	I_{OH}	–1			mA	8, 9
Logic 0 Output @ 0.4 Volts	I_{OL}			4	mA	8, 9
Standby Current	I_{STBY}		22		µA	

ANALOG RESISTOR CHARACTERISTICS

(0°C to 70°C; V_{CC}=5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
End–to–End Resistor Tolerance		–20		+20	%	
Absolute Linearity			±0.75		LSB	4
Relative Linearity			±0.3		LSB	5
–3 dB Cutoff Frequency	F_{CUTOFF}				Hz	7
Noise Figure						11
Temperature Coefficient			±800		ppm/C	

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	3
Output Capacitance	C_{OUT}			7	pF	3

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CLK Frequency	f_{CLK}	DC		10	MHz	10
Width of CLK Pulse	t_{CH}	50			ns	10
Data Setup Time	t_{DC}	30			ns	10
Data Hold Time	t_{CDH}	10			ns	10
Propagation Delay Time Low to High Level Clock to Output	t_{PLH}			50	ns	10
Propagation Delay Time High to Low Level	t_{PLH}			50	ns	10
$\overline{RST}$ High to Clock Input High	t_{CC}	50			ns	10
$\overline{RST}$ Low from Clock Input High	t_{HLT}	50			ns	10
$\overline{RST}$ Inactive	t_{RLT}	125			ns	
Clock Low to Data Valid on a Read	t_{CDD}			30	ns	10
CLK Rise Time, CLK Fall Time	t_{CR}			50	ns	10

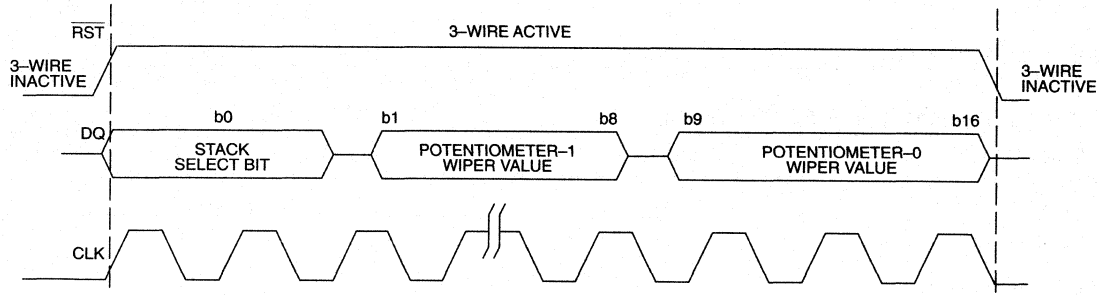
4

NOTES:

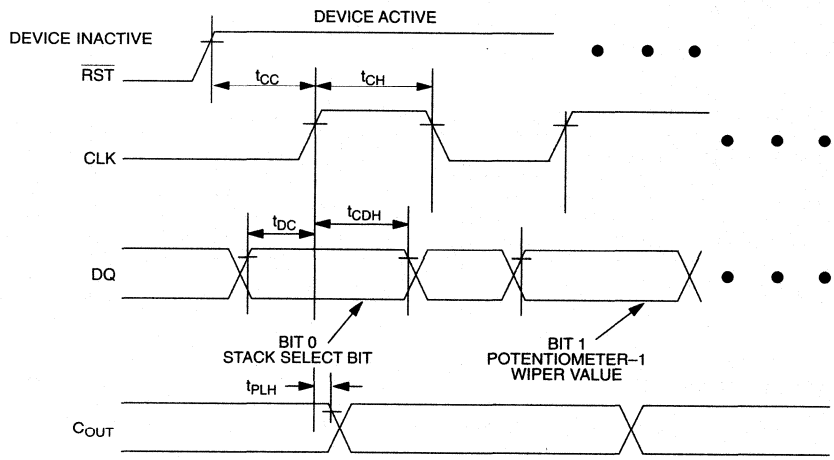
1. All voltages are referenced to ground.
2. Resistor inputs cannot exceed the substrate bias voltage, Vb, in the negative direction.
3. Capacitance values apply at 25°C.
4. Absolute linearity is used to determine wiper voltage versus expected voltage as determined by wiper position. Device test limits ±1.6 LSB.
5. Relative linearity is used to determined the change in voltage between successive tap positions. Device test limits ±0.5 LSB.
6. Typical values are for ta = 25°C and nominal supply voltage.
7. –3 dB cutoff frequency characteristics for the DS1267 depend on potentiometer total resistance: DS1267–010; 1 MHz, DS1267–050; 200 KHz, DS1267–100; 100 KHz.
8. Cout is active regardless of the state of $\overline{RST}$.
9. V_{REF}= 1.5 volts .
10. See Figure 9(a), (b), and (c).
11. Noise < –120 dB/√Hz. Reference 1 volt (thermal).
12. See Figure 11.

TIMING DIAGRAMS Figure 9

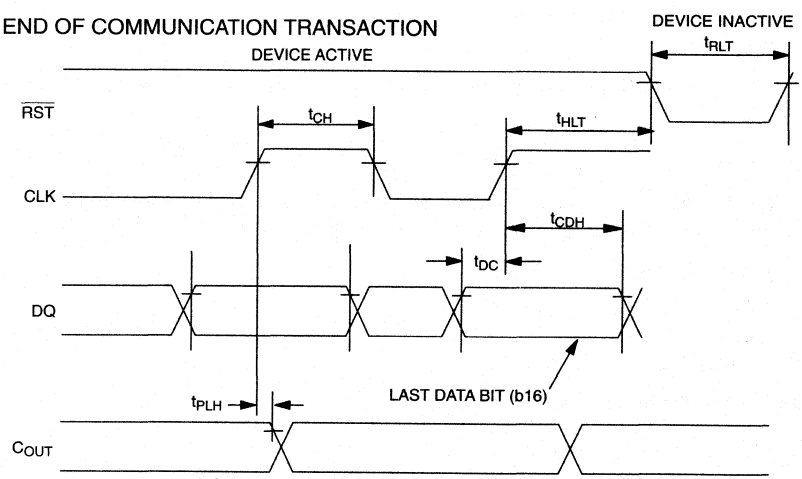
(A) 3–WIRE SERIAL INTERFACE GENERAL OVERVIEW



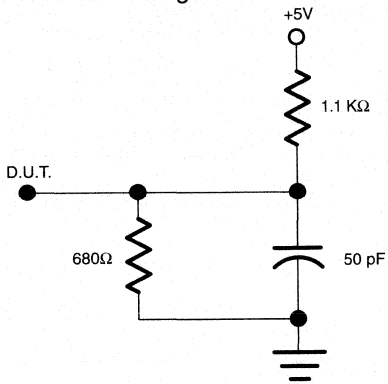
(B) START OF COMMUNICATION TRANSACTION



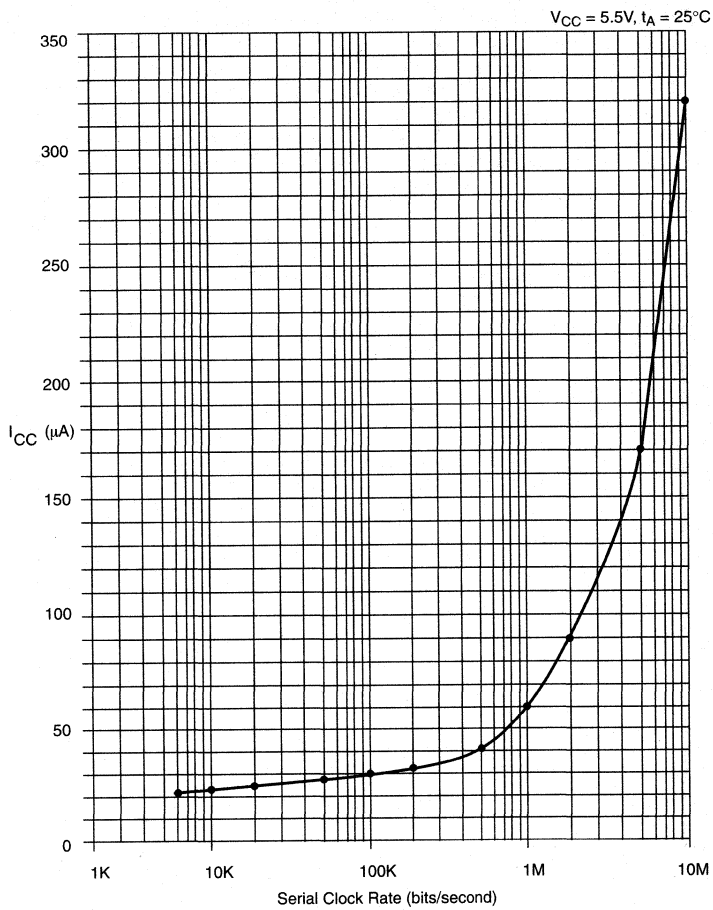
(C) END OF COMMUNICATION TRANSACTION



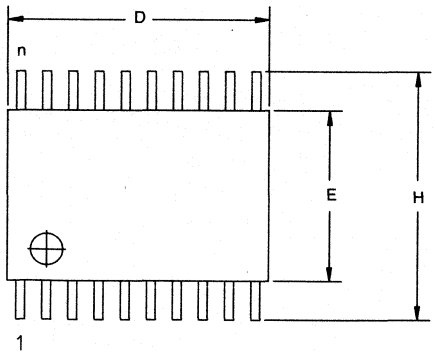
DIGITAL OUTPUT LOAD SCHEMATIC Figure 10

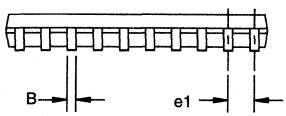


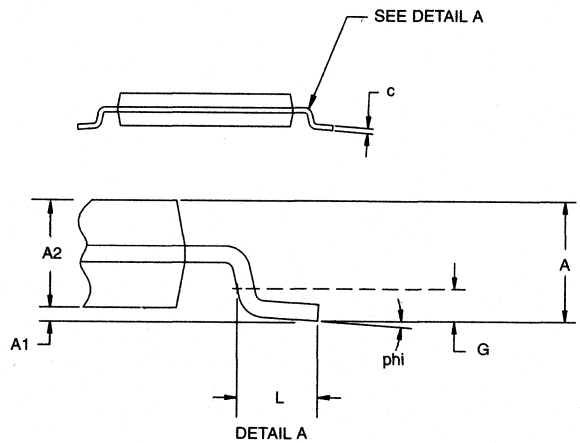
TYPICAL SUPPLY CURRENT VS. SERIAL CLOCK RATE Figure 11



DS1267E 20-PIN TSSOP







DIM	MIN	MAX
A MM	–	1.10
A1 MM	0.05	–
A2 MM	0.75	1.05
C MM	0.09	0.18
L MM	0.50	0.70
e1 MM	0.65 BSC	
B MM	0.18	0.30
D MM	6.40	6.90
E MM	4.40 NOM	
G MM	0.25 REF	
H MM	6.25	6.55
phi	0°	8°

DALLAS SEMICONDUCTOR

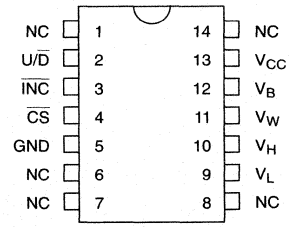
DS1666, DS1666S
Audio Digital Resistor

FEATURES

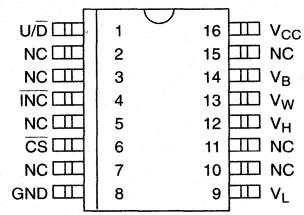
- 128 position, digitally controlled potentiometer
- Operates from a +5 volts power supply with TTL signal inputs
- Wide analog voltage range of ±5 volts
- Resistive elements are temperature compensated to ±20 percent end to end
- Low–power CMOS
- 14–pin DIP or 16–pin SOIC for surface mount applications
- Default position on power up sets wiper position at 10%
- Operating temperature range
  - 0°C to 70°C; commercial version
  - –40°C to +85°C; industrial version

		Resolution/Step		
Resistance values		Low End	High End	-3dB Point
DS1666-10	10KΩ	24Ω	152Ω	1.1 MHz
DS1666-50	50KΩ	122Ω	759Ω	200 KHz
DS1666-100	100KΩ	243Ω	1.519KΩ	100 KHz

PIN ASSIGNMENT



14-Pin DIP (300 Mil)
See Mech. Drawings Section



16-Pin SOIC (300 Mil)
See Mech. Drawings Section

PIN DESCRIPTION

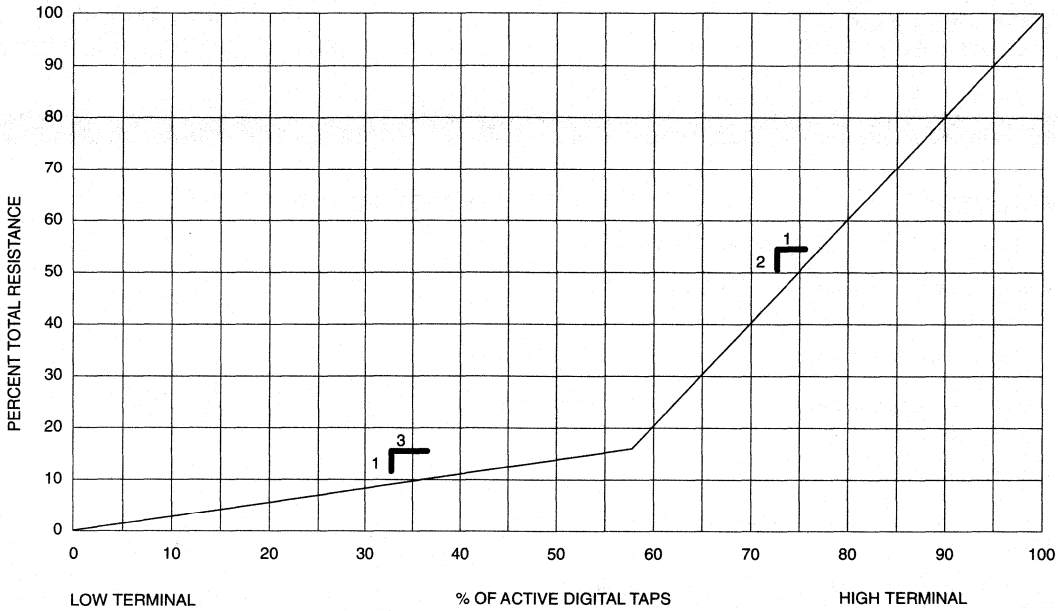
V_H	– High Terminal of Resistor
V_L	– Low Terminal of Resistor
V_W	– Wiper Terminal of Resistor
$\overline{U/D}$	– Up/Down Control
$\overline{INC}$	– Wiper Movement Control
$\overline{CS}$	– Chip Select for Wiper Movement
NC	– No Connection
V_{CC}	– +5 Volts
GND	– Ground
V_B	– 0 to –5 Volts

DESCRIPTION

The DS1666 is a solid–state potentiometer which is set to value by digitally controlled resistive elements. The potentiometer is composed of 127 resistive sections. Between each resistive section and both ends of the potentiometer are TAP points accessible to the wiper. The position of the wiper on the resistance array is controlled by the $\overline{CS}$, $\overline{U/D}$ and $\overline{INC}$ inputs. The position of the wiper defaults to the 10% position on power up. The resolution of the DS1666 is shown in Figure 1.

The DS1666 Digital Audio Resistor is uniquely designed to provide a potentiometer that is logarithmic rather than linear across its entire range. The lower half of the potentiometer advances 1% of total resistance for each 3% of scale advanced, providing for precise amplification of low volume signals. The upper half of the potentiometer advances 2% of resistance for every 1% of scale advanced, providing for the lower resolution gain required for high volume amplification.

GRAPH OF AUDIO TAPER Figure 1



OPERATION

The $\overline{CS}$, U/$\overline{D}$ and $\overline{INC}$ inputs control the position of the wiper along the resistor array (Figure 1). When $\overline{CS}$ is active (low), a high to low transition on the $\overline{INC}$ will increment or decrement an internal counter depending on the level of the U/$\overline{D}$ pin. When the U/$\overline{D}$ pin is low, the counter will decrement. When the U/$\overline{D}$ pin is high, the counter will increment. The state of the U/$\overline{D}$ pin can be changed while $\overline{CS}$ is active allowing for precise adjustment during calibration. The output of the counter is decoded to set the position of the wiper. When the $\overline{CS}$ input transitions to the high (inactive) level, the value of the counter is stored and the wiper position is maintained until power (V_{CC}) is lost. When power is restored, the DS1666 returns to the default setting and positions the wiper to 10 percent. The value of the end-to-end and end-to-wiper position is indeterminate while V_{CC} is not applied.

The DS1666 has a resistor array that resembles an audio taper potentiometer as shown in Figure 1 1. Since the taper is not linear, exact resistance values for each of the 128 positions of the resistor is not specified. However, the end-to-end resistance is specified to be within ±20 percent of the stated resistor value over a temperature range of 0°C to 70°C for commercial version and –40°C to +85°C for industrial version of the part.

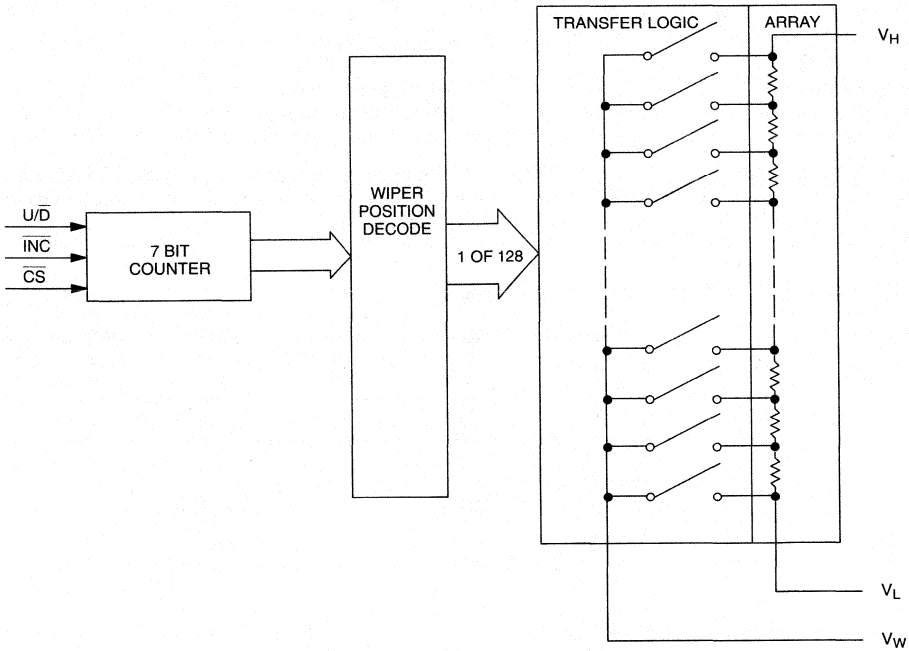
ANALOG CHARACTERISTICS

End-to-End Resistance Tolerance = ±20 percent
Typical Noise = <120 dB/Hz REF:IV
Temperature Coefficient = ±800 PPM/°C typical
Resistance at tap #74=18% ± 2% of total resistance.

PIN DESCRIPTIONS

V_H	The high end of the potentiometer. This terminal is capable of handling input voltages between ±5 volts.
V_L	The Low end of the potentiometer. This terminal is capable of handling input voltages between ±5 volts.
V_W	The wiper terminal of the potentiometer. The value of the wiper is controlled by the U/$\overline{D}$ and the $\overline{INC}$ pins.
Up/Down (U/$\overline{D}$)	The U/$\overline{D}$ input controls the direction of the wiper movement when setting the potentiometer.
Increment ($\overline{INC}$)	Toggling $\overline{INC}$ will move the potentiometer wiper by either incrementing or decrementing the counter.
Chip Select ($\overline{CS}$)	The device is selected when $\overline{CS}$ input is low. The current counter value is stored when CS is returned high.

BLOCK DIAGRAM Figure 2



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MODE SELECTION Figure 3

$\overline{CS}$	$\overline{INC}$	U/$\overline{D}$	MODE
L	↓	H	WIPER UP
L	↓	L	WIPER DOWN
↑	H	X	STORE WIPER POSITION

ABSOLUTE MAXIMUM RATINGS*

Voltage on $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$, and V_{CC} Relative to Ground	–0.5V to +7.0V
Voltage on V_H, V_L, and V_W Relative to Ground	-6.5V to +6.5V
Voltage on V_B	-6.5V to Ground
Operating Temperature	–40°C to +85°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(–40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	+4.5	5.0	5.5	V	1
Input Logic 1	V_{IH}	2.0		V_{CC}+0.5	V	1
Input Logic 0	V_{IL}	-0.5		+0.8	V	1
V_H, V_L, V_W Voltage	V_R	V_B-0.3		V_{CC}+0.3	V	1
V_B Voltage	V_B	-5.5		GND	V	1

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC} = 5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}		0.1	5	mA	3
Input Leakage	I_{LI}	-1		+1	µA	2
Wiper Resistance	R_W		350	650	Ω	
Wiper Current	I_W			1	mA	3

CAPACITANCE

(t_A = 25°C)

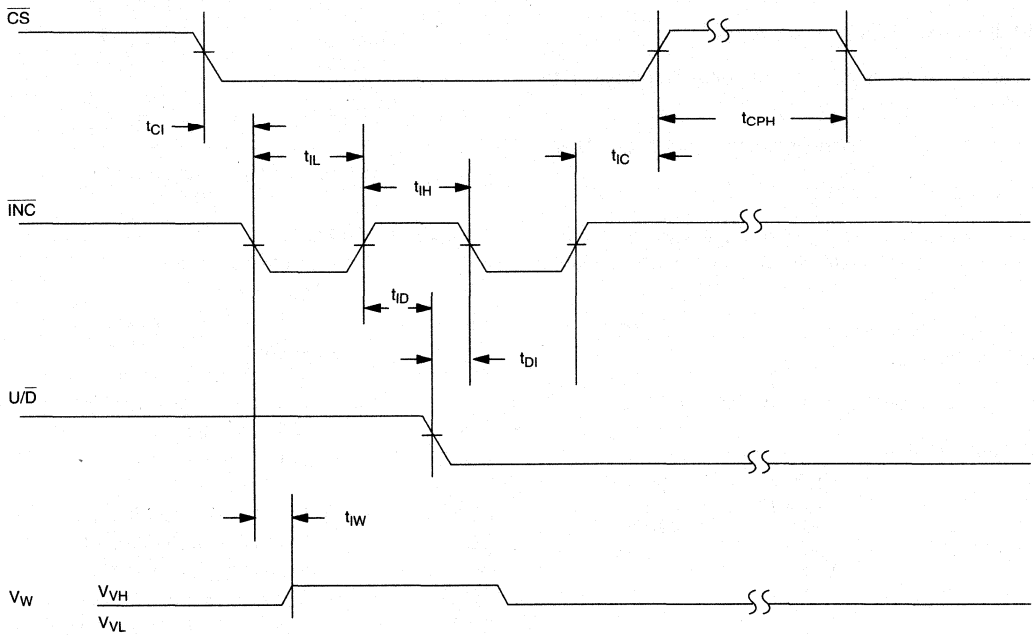
PARAMETER	SYMBOL	CONDITION	TYP	MAX	UNITS	NOTES
Capacitance	C_{IN}	t_A=25°C	6	10	pF	2

AC ELECTRICAL CHARACTERISTICS

(t_A=–40°C to +85°C; V_{CC}=+5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CS}$ to $\overline{INC}$ Setup	t_{CI}	100			ns	
$\overline{INC}$ High to U/$\overline{D}$ Change	t_{ID}	100			ns	
U/$\overline{D}$ to $\overline{INC}$ Setup	t_{DI}	1			µs	
$\overline{INC}$ Low Period	t_{IL}	500			ns	
INC High Period	t_{IH}	1			µs	
$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	t_{IC}	500			ns	
$\overline{CS}$ Deselect Time	t_{CPH}	100			ns	

AC TIMING Figure 4



NOTES:

1. All voltages are referenced to ground.
2. This parameter is periodically sampled and not 100% tested.
3. Typical values are for t_A = 25°C and nominal supply voltages.
4. Wiper output open circuited.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10 ns
Input Level	1.5V

DALLAS SEMICONDUCTOR

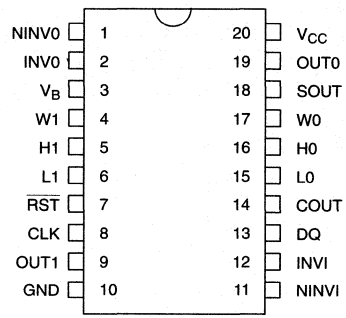
DS1667
Digital Resistor with OP AMP

FEATURES

- Two digitally controlled 256-position potentiometers
- Serial port provides means for setting and reading both potentiometers
- Resistors can be connected in series to provide additional resolution
- Default wiper position on power up is 50%
- Resistive elements are temperature compensated to ±20% end to end
- Two high gain wide bandwidth operational amplifiers
- Low power CMOS design
- Applications include analog–to–digital and digital–to–analog converters, variable oscillators, and variable gain amplifiers
- 20–pin DIP package or optional 20–pin SOIC surface mount package
- Operating temperature range of 0°C to 70°C
- Resistance Values

		RESOLUTION	-3 dB POINT
DS1667-10:	10K	39 ohms	1.1 MHz
DS1667-50:	50K	195 ohms	200 kHz
DS1667-100:	100K	390 ohms	100 kHz

PIN ASSIGNMENT



20-Pin DIP (300 Mil) and 20-Pin SOIC
See Mech. Drawings Section

PIN DESCRIPTION

V_{CC}	–	+5 Volt Supply
GND	–	Ground
L0, L1	–	Low End of Resistor
H0, H1	–	High End of Resistor
W0, W1	–	Wiper End of Resistor
V_B	–	Substrate Bias and OP AMP Negative Supply
SOUT	–	Wiper for Stacked Configuration
$\overline{RST}$	–	Serial Port Reset Input
DQ	–	Serial Port Input/Output
CLK	–	Serial Port Clock Input
COUT	–	Cascade Serial Port Output
NINV0, NINVI	–	Noninverting OP AMP Input
INV0, INVI	–	Inverting OP AMP Input
OUT0, OUT1	–	OP AMP Outputs

DESCRIPTION

The DS1667 is a dual–solid state potentiometer that is adjustable by digitally selected resistive elements. Each potentiometer is composed of 256 resistive elements. Between each resistive section of each potentiometer are tap points accessible to the wiper. The position of the wiper on the resistive array is set by an 8–bit register that controls which tap point is connected to the wiper output. Each 8–bit register can be read or written by sending or receiving data bits over a 3–wire serial port. In addition, the resistors can be stacked such that a single potentiometer of 512 sections results. When two separate potentiometers are used, the resolution of the DS1667 is equal to the resistance value divided by 256. When the potentiometers are stacked end to end, the resistance value is doubled while the resolution remains the same. The DS1667 also contains two high gain wide bandwidth operational amplifiers. Each amplifier has both the inverting and non-inverting inputs and the output available for user configuration. The operational amplifiers can be paired with the resistive ele-

ments to perform such functions as analog to digital conversion, digital to analog conversion, variable gain amplifiers, and variable oscillators.

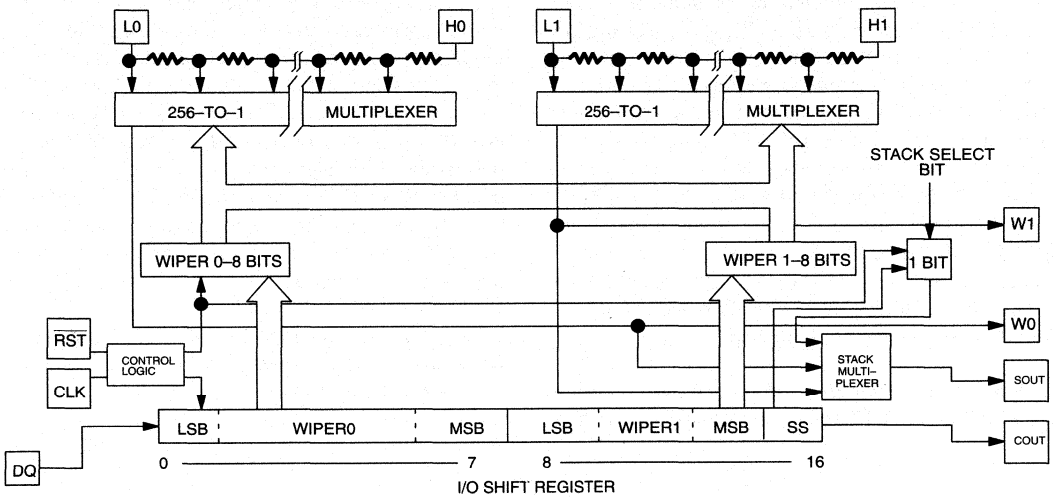
OPERATION - DIGITAL RESISTOR SECTION

The DS1667 contains two potentiometers, each of which has its wiper set by a value contained in an 8 bit register (see Figure 1). Each potentiometer consists of 256 resistors of equal value with tap points between each resistor and at the low end.

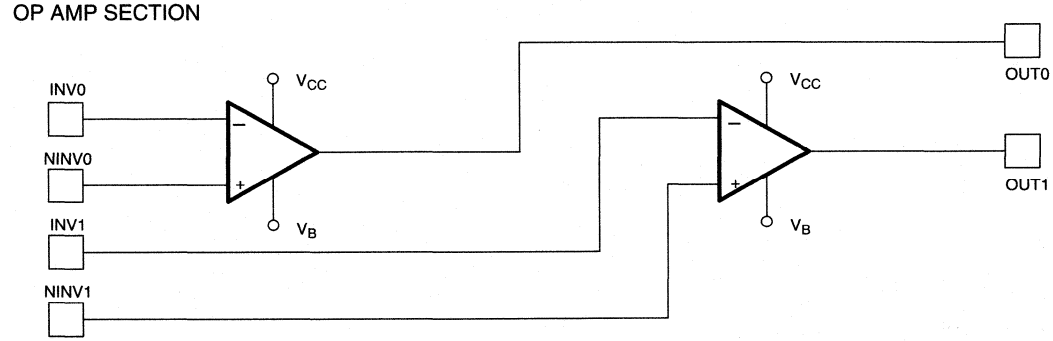
In addition, the potentiometer can be stacked by connecting them in series such that the high end of potentiometer 0 is connected to the low end of potentiometer 1. When stacking potentiometers, the stack select bit is used to select which potentiometer wiper will appear at the stack multiplexer output (SOUT). A zero written to the stack multiplexer will connect wiper 0 to the SOUT pin. This wiper will determine which of the 256 bottom taps of the stacked potentiometer is selected. When a 1 is written to the stack multiplexer, wiper 1 is selected and one of the upper 256 taps of the stacked potentiometer is presented at the SOUT pin.

BLOCK DIAGRAM Figure 1

RESISTOR SECTION



OP AMP SECTION



Information is written to and read from the wiper 0 and wiper 1 registers and the stack select bit via the 17-bit I/O shift register. The I/O shift register is serially loaded by a 3 wire serial port consisting of $\overline{RST}$, DQ, and CLK. It is updated by transferring all 17 bits (Figure 2). Data can be entered into the 17 bit shift register only when the $\overline{RST}$ input is at a high level. While at a high level, the $\overline{RST}$ function allows serial entry of data via the D/Q pin. The potentiometers always maintain their previous value until $\overline{RST}$ is taken to a low level, which terminates data transfer. While $\overline{RST}$ input is low, the DQ and CLK inputs are ignored.

Valid data is entered into the I/O shift register while $\overline{RST}$ is high on the low-to-high transition of the CLK input. Data input on the DQ pin can be changed while the clock input is high or low, but only data meeting the setup requirements will enter the shift register. Data is always entered starting with the value of the stack select bit. The next 8 bits to be entered are those specifying the wiper 1 setting. The MSB of these 8 bits is sent first. The next 8 bits to be entered are those specifying the wiper 0 setting, sent MSB first. The 17th bit to be entered, therefore, will be the least significant bit of the wiper 0 setting. If fewer than 17 bits are entered, the value of the potentiometer settings will result from the number of bits that were entered plus the remaining bits of the old value shifted over by the number of bits sent. If more than 17 bits are sent, only the last 17 bits are left in the shift register. Therefore, sending other than 17 bits can produce indeterminate potentiometer settings.

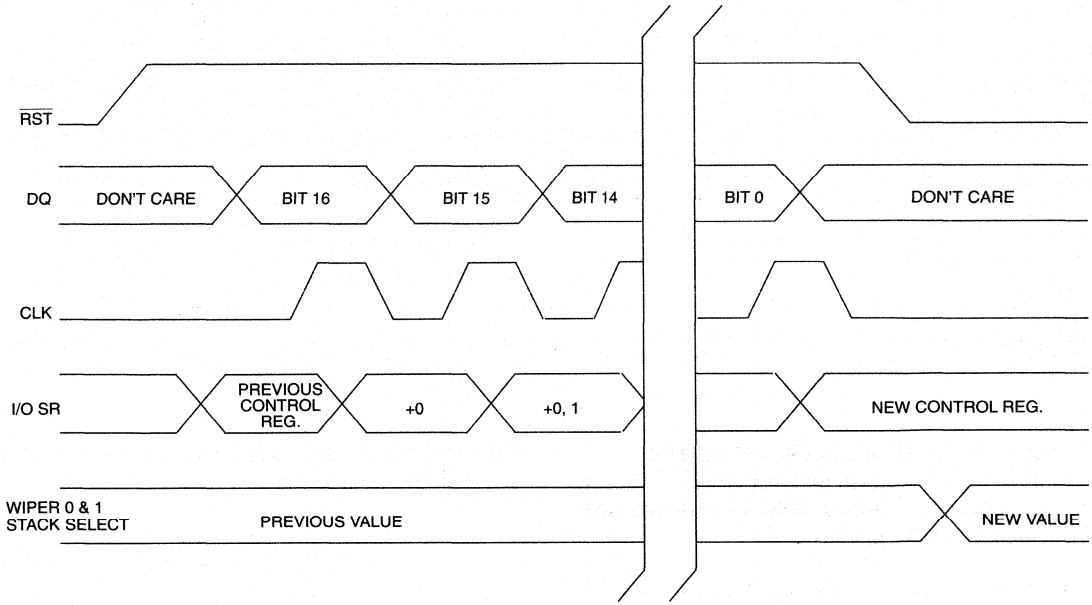
As bits are entered into the shift register, the previous value is shifted out bit by bit on the cascade serial port pin (COUT). By connecting the COUT pin to the DQ pin of a second DS1667, multiple devices can be daisy chained together as shown in Figure 3.

When connecting multiple devices, the total number of bits sent is always 17 times the number of DS1667s in the daisy chain. In applications where it is desirable to read the settings of potentiometers, the COUT pin of the last device connected in a daisy chain must be connected back to the DQ input of the first device through a resistor with a value of 1K to 10K. This resistor provides isolation between COUT and DQ when writing to the device (see Figure 3).

When reading data, the DQ line is left floating by the reading device. When $\overline{RST}$ is held low, bit 17 is always present on the COUT pin, which is fed back to the input DQ pin through the resistor (see Figure 4).This data bit can now be read by the reading device. The $\overline{RST}$ pin is then transitioned high to initiate a data transfer. When the CLK input transitions low to high, bit 17 is loaded into the first position of the I/O shift register and bit 16 becomes present on COUT and DQ. After 17 bits (or 17 times the number of devices for a daisy chain), the data has shifted completely around and back to its original position. When $\overline{RST}$ is transitioned back low to end data transfer, the value (the same as before the read occurred) is loaded into the wiper 0 and wiper 1 registers and the stack select bit.

When power is applied to the DS1667, the device always has the wiper settings at half position and the stack select bit is at zero.

WRITING DATA Figure 2



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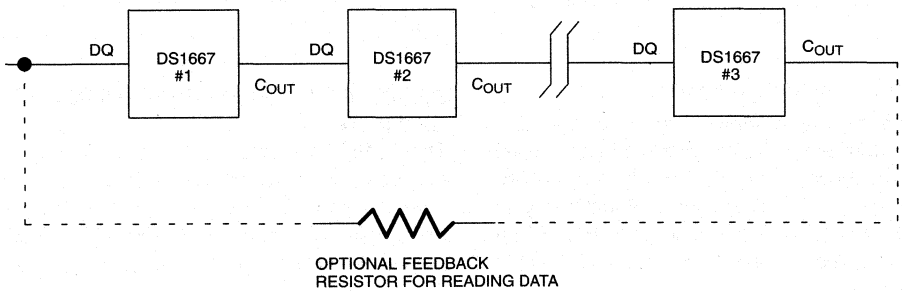
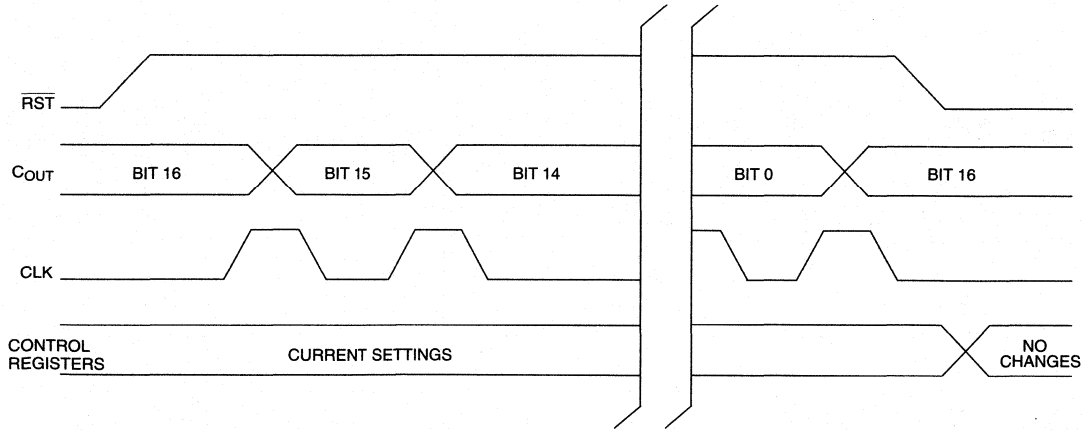
CASCADING MULTIPLE DEVICES Figure 3



READING DATA Figure 4



DS1667 LINEARITY MEASUREMENTS

An important specification for the DS1667 is linearity, that is, for a given digital input, how close the analog output is to that which is expected.

The test circuit used to measure the linearity of the DS1667 is shown in Figure 5. Note that to get an accurate output voltage it is necessary to assure that the output current is 0, in order to negate the effects of wiper impedance RW which is typically 400 ohms. For any given setting N for the pot, the expected voltage output at SOUT is:

$$VO = -5 + [10 \times (N/256)] \text{ (in volts)}$$

Absolute linearity is a comparison of the actual measured output voltage versus the expected value given by the equation above, and is given in terms of an LSB, which is the change in expected output when the digital input is incremented by 1. In this case the LSB is 10/256 or 0.03906 volts. The equation for the absolute linearity of the DS1667 is:

$$\frac{V_O(\text{actual}) - V_O(\text{expected})}{LSB} = AL \text{ (in LSBs)}$$

The specification for absolute linearity of the DS1667 is ± 1 LSB typical.

Relative linearity is a comparison of the difference of actual output voltages of two successive taps and the difference of the expected output voltages of two successive taps. The expected difference of output voltages is 1 LSB or 0.03906V for the measurement system of Figure 5. Relative linearity is expressed in terms of an LSB and is given by the equation:

$$\frac{\Delta V_O(\text{actual}) - LSB}{LSB} = RL$$

The specification for relative linerity of the DS1667 is ± 0.5 LSB typical.

Figure 6 is a plot of absolute linearity (AL) and relative linearity (RL) versus wiper setting for a typical DS1667 at 25°C.

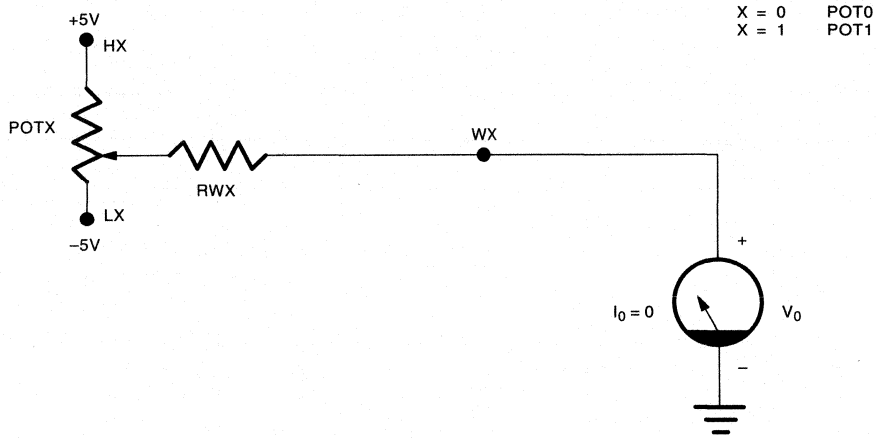
DESCRIPTION AND OPERATION - OP AMP SECTION

The DS1667 contains two operational amplifiers which are ideal for operation from a single 5V supply and ground or from ±5V supplies (see Figure 1). An internal resistor divider defines the internal reference of the op amp to be halfway between the power supplies, i.e.:

$$\frac{V_{DD} + V_B}{2}$$

For optimal performance, choose analog ground to be this value. The operational amplifiers feature rail to rail output swing in addition to an input common mode range that includes the positive rail. Performance features include broad band noise immunity as well as voltage gain into realistic loads specified at both 600 ohms and 2K ohms. High voltage gain is produced with low input offset voltage and low offset voltage drift. Current consumption is less than 1.9 mA per amplifier and the device is virtually immune to latchup.

LINEARITY MEASUREMENT CONFIGURATION Figure 5



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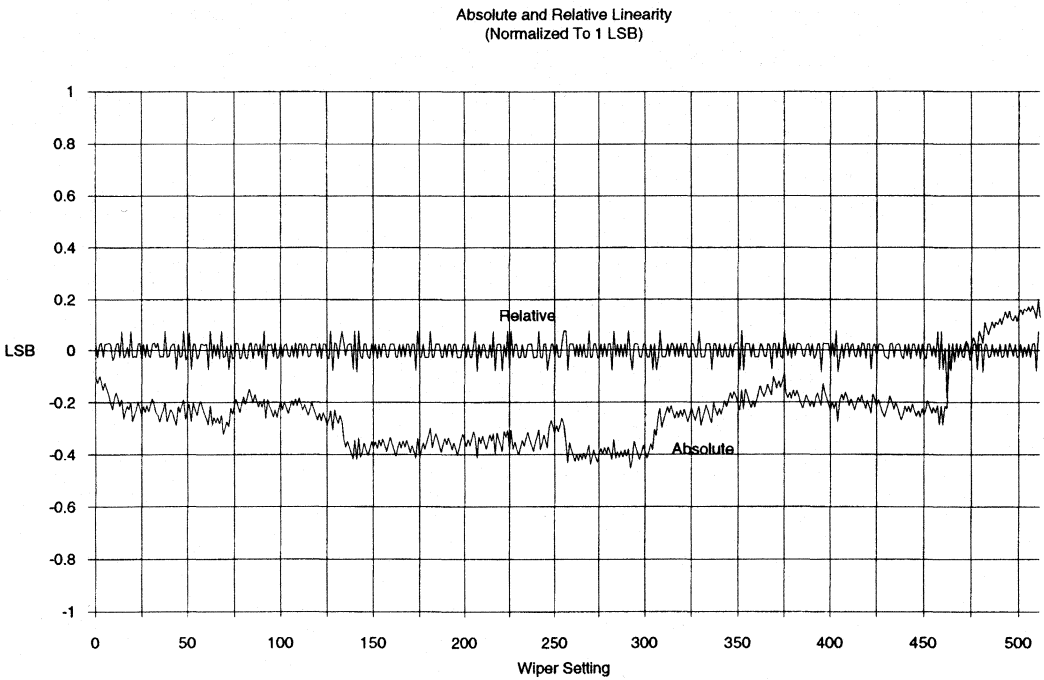
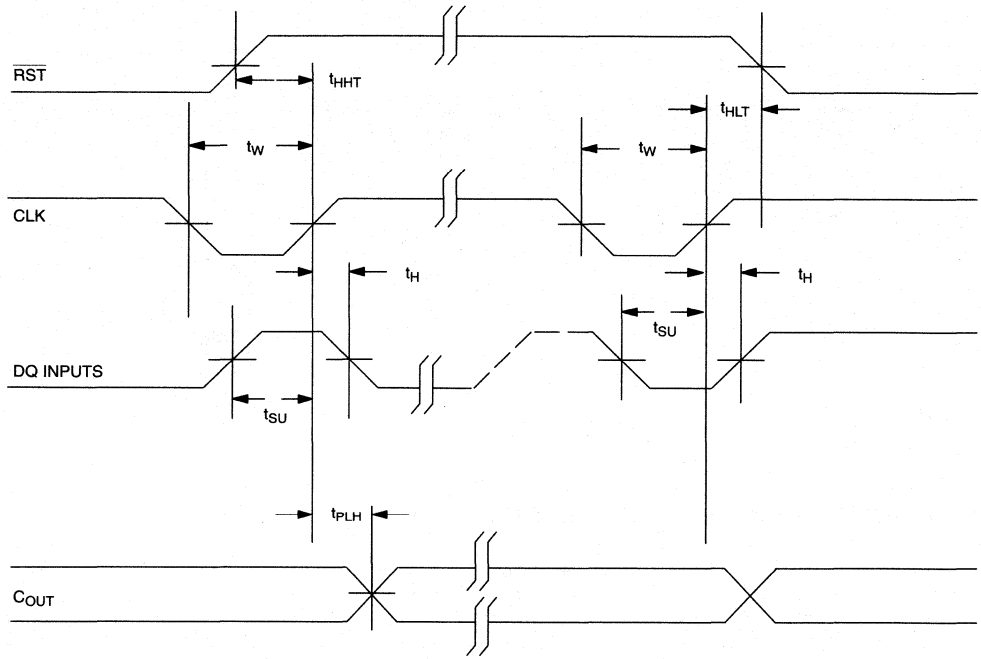
DS1667 ABSOLUTE AND RELATIVE LINEARITY Figure 6



TIMING DIAGRAM: RESISTOR SECTION Figure 7



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground (V_B = GND)	–0.5V to +7.0V
Voltage on Resistor Pins when V_B = -5.5V	-5.5V to +7.0V
Voltage on V_B	-5.5V to GND
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS RESISTOR SECTION

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Positive Supply Voltage	V_{CC}	+4.5	5.0	5.5	V	1
Input Logic 1	V_{IH}	2.0		V_{CC}+0.5	V	1
Input Logic 0	V_{IL}	-0.5		+0.8	V	1
Negative Supply Voltage	V_B	-5.5		GND	V	1
Resistor Inputs	L, H, W	V_B - 0.5		V_{CC} + 0.5	V	2

4

DC ELECTRICAL CHARACTERISTICS RESISTOR SECTION

(0°C to 70°C; V_{CC} = 5.0V ± 10%, V_B = -5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Positive Supply Current	I_{CC}		3	5	mA	
Negative Supply Current	I_B		3	5	mA	
Input Leakage	I_U	–1		+1	µA	
Wiper Resistance	R_W		400	1000	ohms	
Wiper Current	I_W			1	mA	
Output Leakage	I_{LO}	–1		+1	µA	
Logic 1 Output @ 2.4 Volts	I_{OH}	–1.0			mA	
Logic 0 Output @ 0.4 Volts	I_{OL}			4	mA	
End–to–End Resistor Tolerance	TOL_R	–20		+20	%	
Noise (ref: 1V)	N		–120		$\frac{dB}{\sqrt{Hz}}$	
Absolute Linearity	AL		1.0		LSB	
Relative Linearity	RL		0.5		LSB	
Resistor Temperature Coefficient	TC_R			850	$\frac{ppm}{°C}$	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS RESISTOR SECTION

(0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CLK Frequency	f_{CLK}			10	MHz	
Width of CLK Pulse	t_W	50			ns	
Data Setup Time	t_{SU}	30			ns	
Data Hold Time	t_H	10			ns	
Propagation Delay Time Low to High Level Clock to Output	t_{PLH}			50	ns	3
$\overline{RST}$ High to Clock Input High	t_{HHT}	50			ns	
$\overline{RST}$ Low from Clock Input High	t_{HLT}	50			ns	

OPERATIONAL AMPLIFIER SECTION
DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5.0V ± 10%, V_B = -5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Offset Voltage	V_{OS}		5	10	mV	
Input Offset Voltage Drift	V_{OSD}		10		uV/°C	
Common Mode Rejection	CM_R		62		dB	
Positive Power Supply Rejection	$+PS_R$		62		dB	
Negative Power Supply Rejection	$-PS_R$		62		dB	
Input Common Mode Voltage Range	C_{CCM}	V_B+1.5V		V_{CC}	V	
Large Signal Voltage Gain			106		dB	R_L=2KΩ
Large Signal Voltage Gain			96		dB	R_L=600KΩ
Output Swing	V_{SWGH}	4.6	4.7		V	R_L=2KΩ to GND
Output Swing	V_{SWGL}		–4.7	–4.6	V	V_B = –5V
Output Swing	V_{SWGH}	4.5	4.6		V	R_L=600KΩ to GND
Output Swing	V_{SWGL}		–4.6	–4.5	V	V_B = –5V
Output Current	$V_{O,SOURCE}$	13	58		mA	V_O = 0V
Output Current	$V_{O,SINK}$	13	63		mA	V_O = +5V

OPERATIONAL AMPLIFIER SECTION
AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5.0V ± 10%)

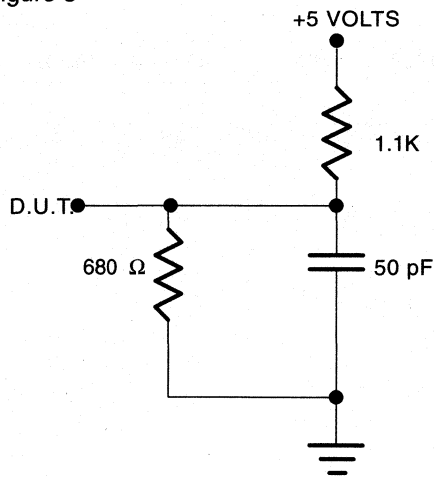
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Slew Rate	V_{SL}	0.7	2		V/µs	6
Gain Bandwidth Product	GBP		2.5		MHz	5
Phase Margin	PM		75		deg	5
Gain Margin	GM		20		dB	5
Amp–to–Amp Isolation	AAI		130		dB	
Input Referred Voltage Noise	IRVF		100		$nV/\sqrt{Hz}$	F=1 KHz
Input Referred Current Noise	IRV1		0.0002		$pA/\sqrt{Hz}$	F=1 KHz
Total Harmonic Distortion	HD		0.1		%	F=10 KHz AV=–10 RL=2KΩ V_O=1V_{PP}

4

NOTES:

1. All voltages are referenced to ground.
2. Resistor inputs cannot exceed the substrate bias voltage in the negative direction
3. Measured with a load as shown in Figure 8.
4. Over a frequency range of 0 - 1 KHz.
5. Load is R_L = 600 Ω C_L = 10 pF
6. V_{DD} = +5.0V V_B = -5.0V connected as voltage follower with 10V step input and R_L = ∞.
7. To achieve best op amp performance, V_{DD} = +5.0V V_B = -5.0V and analog ground = 0V. In general analog ground = $\frac{V_{DD} + V_B}{2}$.
8. OP AMPS idle, no load.

LOAD SCHEMATIC Figure 8



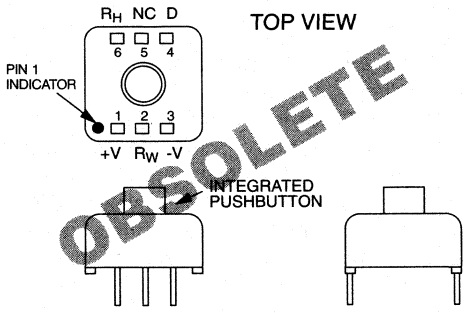
DALLAS SEMICONDUCTOR

DS1668, DS1669, DS1669S
Dallastat™ Electronic Digital Rheostat

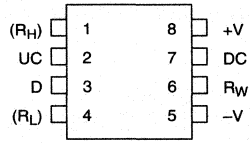
FEATURES

- Replaces mechanical variable resistors
- Available as the DS1668 with manual interface or the DS1669 integrated circuit
- Human engineered interface provides easy control with DS1668
- Electronic interface provided for digital as well as manual control
- Wide differential input voltage range between 4.5 and 8 volts
- Wiper position is maintained in the absence of power
- Low cost alternative to mechanical controls
- Applications include volume, tone, contrast, brightness, and dimmer control
- 8–pin SOIC and 8–pin DIP packages for DS1669
- Standard resistance values for Dallastat
  - DS1668/DS1669–10 ~ 10KΩ
  - DS1668/DS1669–50 ~ 50KΩ
  - DS1668/DS1669–100 ~ 100KΩ
- Operating Temperature Range
  - Commercial: 0°C to 70°C; DS1668, DS1669
  - Industrial: –40°C to +85°C; DS1669

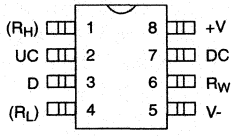
PIN ASSIGNMENT DS1668



PIN ASSIGNMENT DS1669



8-Pin DIP (300 Mil)
See Mech. Drawings Section



8-Pin SOIC (208 Mil)
See Mech. Drawings Section

PIN DESCRIPTION DS1669

R_H	-	Resistor High End
R_W	-	Resistor Wiper
R_L	-	Resistor Low End
-V, +V	-	Voltage Inputs
UC	-	Up Contact Input
D	-	Digital Input
DC	-	Down Contact Input

PIN DESCRIPTION DS1668

+V	-	Positive Voltage Input
-V	-	Negative Voltage
R_W	-	Resistor Wiper
D	-	Digital Input
R_H	-	Resistor High End
NC	-	No Connection - Pin Missing

DESCRIPTION

The DS1668 and DS1669 Dallastats are digital rheostats or potentiometers. These units provide 64 possible uniform tap points over the resistive range and are available in standard versions of 10K, 50K, and 100K ohms. The Dallastats can be controlled by either a mechanical–type contact closure input or a digital source input such as a CPU. Wiper position is maintained in the absence of power which is accomplished through the use of a EEPROM memory cell array. The EEPROM cell array is specified to accept greater than 80,000 writes.

The DS1668 and DS1669 differ in the type packages in which they are offered. The DS1668 is only available in a custom 6–pin package with a single integrated pushbutton as shown in the package drawing. The single integrated pushbutton provides the mechanical control input of the wiper position. In addition, a digital source input, D, allows the potentiometer to be controlled by a microcontroller or processor. Other package pins include the positive voltage input, +V, the negative voltage input, –V, the resistor wiper terminal, R_W, and the high resistor terminal, R_H. The DS1668 is rated for commercial temperature usage only (0°C to 70°C).

The DS1669 is offered in two standard IC packages which include an 8–pin 300 mil DIP and an 8–pin 200 mil SOIC. Like the DS1668, the DS1669 can be configured to operate using a single pushbutton or digital source input. This is illustrated in Figure 1. Additionally, the DS1669 can be configured to operate in a dual pushbutton configuration which is shown in Figure 2. The DS1669 pinouts allow access to both ends of the potentiometer R_L, R_H, and the wiper, R_W. Control inputs include the digital source input, D, the up contact input, UC, and the down contact input, DC. Other package pinouts include the positive,+V, and negative, –V , supply inputs. The DS1669 is available in commercial or industrial temperature versions.

OPERATION

The DS1668/DS1669 Dallastats are controlled through a contact closure input or by a digital source input. The DS1668 is configured to operate from a single contact closure (pushbutton) input which is integrated in the custom 6–pin package or the device can be driven from the digital source input (D). The DS1669 can be controlled using a single pushbutton input, dual pushbutton, or using the digital source input.

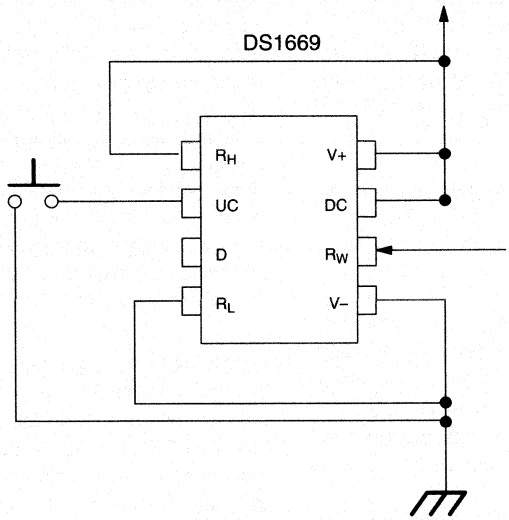
Figure 3 illustrates the single pushbutton configuration of the DS1668. Internally, the low end resistor terminal is connected to the negative supply input terminal. The integrated pushbutton has one side connected to the negative supply input while the other side is connected to the up contact terminal (UC). The digital source input (D) is accessible through pin 4 of the package. The (D) input has an internal pull–up resistor and can be allowed to float when not in use. The down contact input (DC) is not accessible externally. However, this control input is internally connected to the positive input supply.

When powered, the DS1668 assumes a single pushbutton mode of operation. Pressure applied to the integrated pushbutton will cause contact closure which in turn will move the wiper position upward or downward depending on the previous wiper direction. Single pushbutton mode is accomplished in the same manner for the DS1669. However, for the DS1669, all connections must be made by the user since no internal connections exist (see Figure 1). Note that single pushbutton control is accomplished when 1) the (DC) input is connected to the positive supply input and 2) the (D) input is allowed to float. These two conditions must exist from the time of device power–up. The UC input controls both upward and downward movement of the device wiper position in single pushbutton mode of operation.

Dual pushbutton operation is only available when using the DS1669. The DS1668, by design, only supports the single pushbutton mode of operation and digital source input control. Figure 2 provides a typical application example of the dual pushbutton configuration for the DS1669. In dual–pushbutton mode, the up–contact input (UC) is used solely to provide upward movement of the wiper position and the down–contact input (DC) is used to provide downward movement of the wiper position. For dual pushbutton configuration, all control inputs (UC, DC, and D) must remain open on device power–up.

The digital source input, D, was designed for microprocessor or controller applications. This control input manipulates the device in the same manner as the single pushbutton configuration; controlling movement of the wiper position in both upward and downward directions. One added feature over the single pushbutton configuration is the ability to increment or decrement wiper position at a faster rate. Digital source input control is available regardless of the type of pushbutton configuration.

DS1669 SINGLE PUSHBUTTON CONFIGURATION (TYPICAL EXAMPLE) Figure 1



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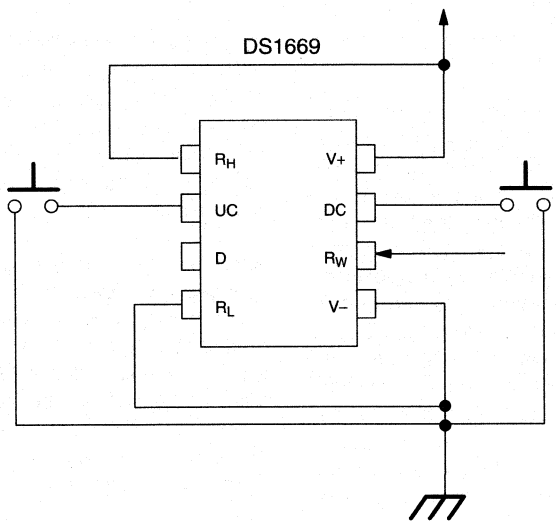
DS1669 DUAL PUSHBUTTON CONFIGURATION (TYPICAL APPLICATION) Figure 2



Dallastats interpret input pulse widths as the means of controlling wiper movement. A single pulse width input over the UC, DC, or D terminals will cause the wiper position to move 1/64th of the total resistance. All inputs, UC, DC, or D, are inactive when in the high state. A transition from a high to low on these inputs is considered the beginning of pulse activity.

A single pulse is defined as being greater than 1 ms but lasting no longer than a second when using the contact closure inputs UC and DC. When using the D input a single pulse is defined as being greater than 1 µs but lasting no longer than 1 second. This is shown in Figures 4a and 6a. Repetitive pulsed inputs can be used to step through each resistive position of the device (see Figures 4a and 6b). The requirement for repetitive pulsed inputs is that pulses must be separated by a minimum time of 1 ms. If not, the Dallastat will interpret repetitive pulses as a single continuous pulse.

Pulse inputs lasting longer than 1 second will cause the wiper to move one position every 100 ms following the initial 1 second hold time. The total time to transcend the entire potentiometer using a continuous input pulse is given in the equation below:

1 (second) + 63 X 100 ms = 7.3 (seconds)

In single pushbutton mode or when using the digital source input, as the wiper reaches the end of the potentiometer its direction of movement reverses. This will occur whether or not the input is a continuous pulse or a sequence of repetitive pulses. Changing the direction of wiper movement in single pushbutton mode or digital source mode is also accomplished by a period of inactivity on the UC or D inputs for (minimum) 1 second or greater. In dual pushbutton mode, the direction is controlled by the UC and DC inputs. No wait states are required to change wiper direction in dual pushbutton mode. Additionally, in dual pushbutton mode as the wiper reaches the end of the potentiometer, the direction of wiper movement will not change. Wiper position will remain at the potentiometers' end until an opposite direction input is given.

All control inputs, UC, DC, and D, are internally pulled up with a 100K ohm resistance. Additionally, the UC and DC inputs are internally debounced and require no external components for input signal conditioning.

The DS1668/DS1669 are provided with two supply inputs –V and +V. The maximum voltage difference between the two supply inputs is + 8.0 volts while the minimum voltage difference is +4.5 volts. All input levels are referenced to the negative supply input, –V. The voltage applied to any Dallastat terminal must not exceed the negative supply voltage (–V) by –0.5 or the positive supply voltage (+V) by + 0.5 volts. The minimum logic high level must be +2.4 volts with reference to the –V supply voltage input. A logic low level with reference to the –V supply voltage has a maximum value of +0.8 volts. Dallastats exhibit a typical wiper resistance of 400 ohms with a maximum wiper resistance of 1000 ohms. The maximum wiper current allowed through the Dallastat is specified at 1 milliamps (see DC Electrical Characteristics).

NONVOLATILE WIPER SETTINGS

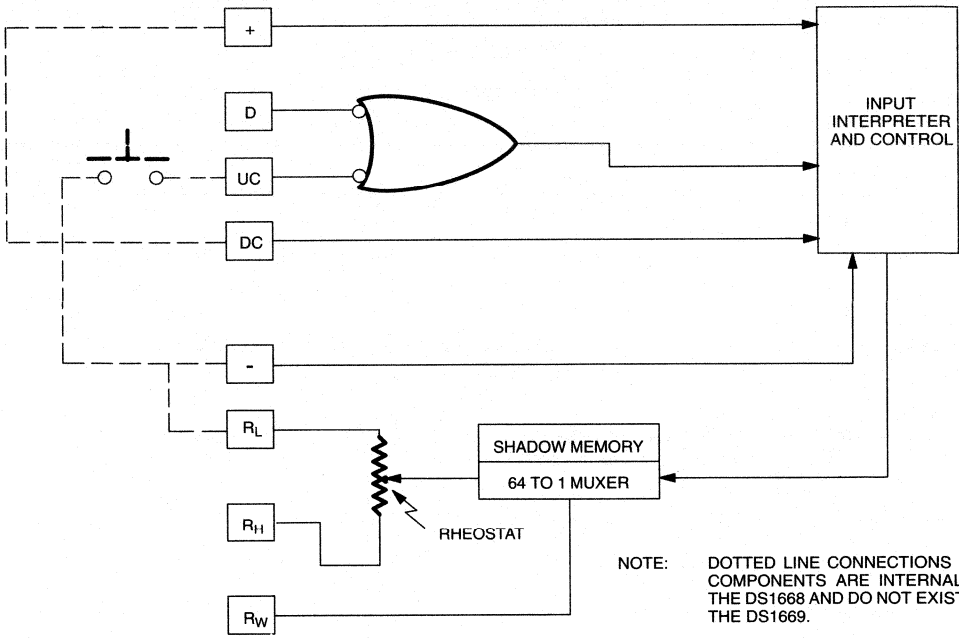
Dallastats maintain the position of the wiper in the absence of power. This feature is provided through the use of EEPROM type memory cell arrays. During normal operation the position of the wiper is determined by the input multiplexer. Periodically, the multiplexer will update the EEPROM memory cells. The manner in which an update occurs has been optimized for reliability, durability, and performance. Additionally, the update operation is totally transparent to the user.

When power is applied to the Dallastat, the wiper setting will be the last recorded in the EEPROM memory cells. If the Dallastat setting is changed after power is applied, the new value will be stored after a delay of 2 seconds. The initial storage of a new value after power–up, occurs when the first change is made, regardless of when this change is made.

After the initial change on power–up, subsequent changes in the Dallastat EEPROM memory cells will occur only if the wiper position of the part is moved greater than 12.5% of the total resistance range. Any wiper movement after initial power–up which is less than 12.5% will not be recorded in the EEPROM memory cells. Since the Dallastat contains a 64–to–1 multiplexer, a change of greater than 12.5% corresponds to a change of the fourth LSB.

Changes or storage to the EEPROM memory cells must allow for a 2 second delay to guarantee that updates will occur. The EEPROM memory cells are specified to accept greater than 80,000 writes before a wear–out condition. If the EEPROM memory cells do reach a wear–out condition, the Dallastat will still function properly while power is applied. However, on power–up the device's wiper position will be that of the position last recorded before memory cell wear out.

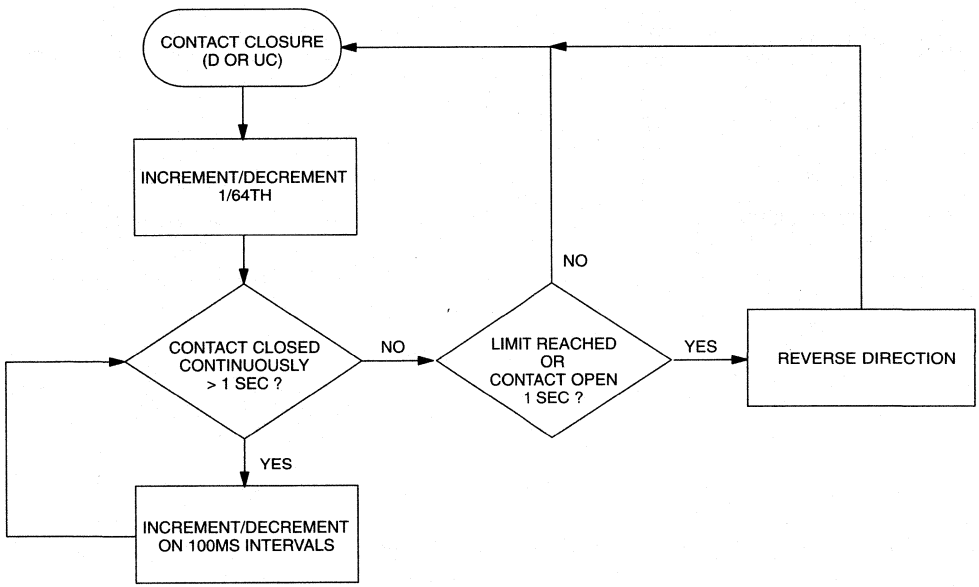
DS1668 DALLASTAT™ BLOCK DIAGRAM Figure 3



NOTE: DOTTED LINE CONNECTIONS AND COMPONENTS ARE INTERNAL TO THE DS1668 AND DO NOT EXIST ON THE DS1669.

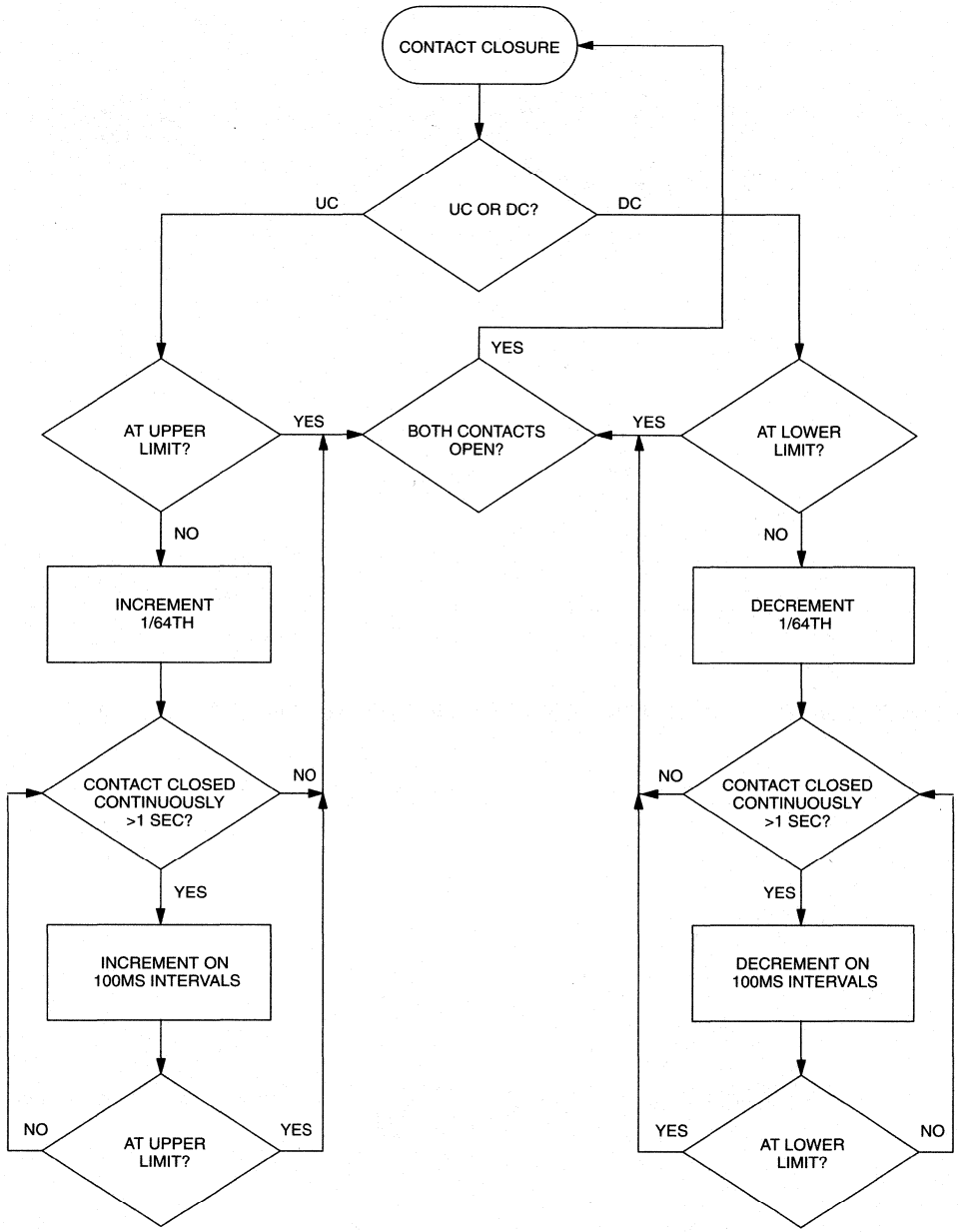
4

FLOWCHART: ONE BUTTON OPERATION AND ELECTRICAL CONTROL Figure 4



CONTACT OPEN AND CONTACT CLOSURE TIMING IS 1s ± 10%

FLOWCHART: TWO BUTTON OPERATION Figure 5



CONTACT OPEN AND CONTACT CLOSURE TIMING IS 1 sec. ± 10%

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to -V	-V –0.5V + 8.0V
Operating Temperature	0°C to 70°C commercial; –40°C to +85°C industrial
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 15 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(-40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
+ Supply Voltage	+V	-V + 4.5		-V + 8.0	V	
- Supply Voltage	-V	+V - 8.0		+V - 4.5	V	
Rheostat Inputs	R_H,R_W,R_L	-V - 0.5		+V + 0.5	V	
Logic Input 1	V_{IH}	+2.4			V	1, 2
Logic Input 0	V_{IL}			+0.8	V	1, 2

4

DC ELECTRICAL CHARACTERISTICS

(-40°C to +85°C; -V to +V = 4.5V to 8.0V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
+, - Supply Current	I_{CC1}		1	2	mA	3
Supply Current, Idle State	I_{CC2}			65	µA	9
Wiper Resistance	R_W		400	1000	Ω	
Wiper Current	I_W			1	mA	5
Rheostat Current	I_H, I_L			1	mA	5
Power–Up Time	t_{PU}			10	µs	10
Input Leakage	I_{LI}	–1		+1	µA	1

AC ELECTRICAL CHARACTERISTICS

(-40°C to +85°C; -V to+V = 4.5V to 8.0V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Digital Input Pulse Width	t_{DPW}	1		DC	µs	1, 7, 8
Contact Pulse Width	t_{CPW}	1		DC	ms	1, 7, 8
Repetitive Input Pulse High Time	t_{HPW}	1		DC	ms	1, 7, 8
Continuous Input Pulse	t_{CCP}	1		DC	s	1, 7, 8

ANALOG RESISTOR CHARACTERISTICS

(-40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
End–to–End Resistor Tolerance		–20		+20	%	
Absolute Linearity		–0.75		+0.75	LSB	11
Relative Linearity		–0.3		+0.3	LSB	12
–3 dB Cutoff Frequency Noise Figure	fcutoff				Hz	13
Temperature Coefficient		–800		+800	ppm/C	

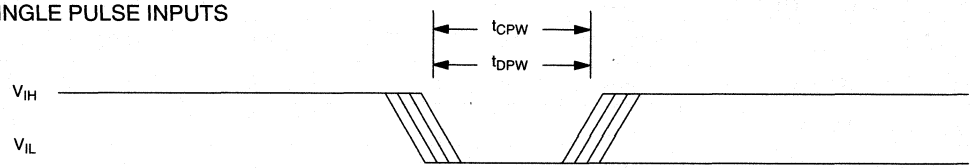
CAPACITANCE

(t_A=25°C)

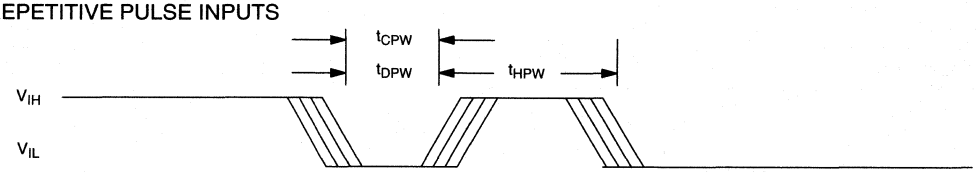
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	6
Output Capacitance	C_{OUT}			7	pF	6

TIMING DIAGRAMS Figure 6

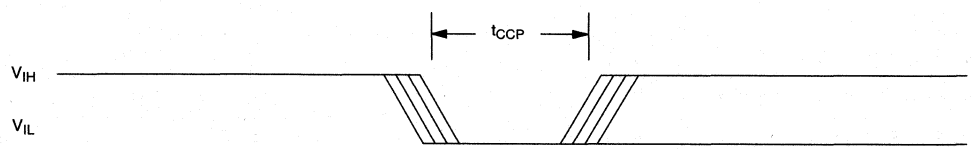
(A) SINGLE PULSE INPUTS



(B) REPETITIVE PULSE INPUTS



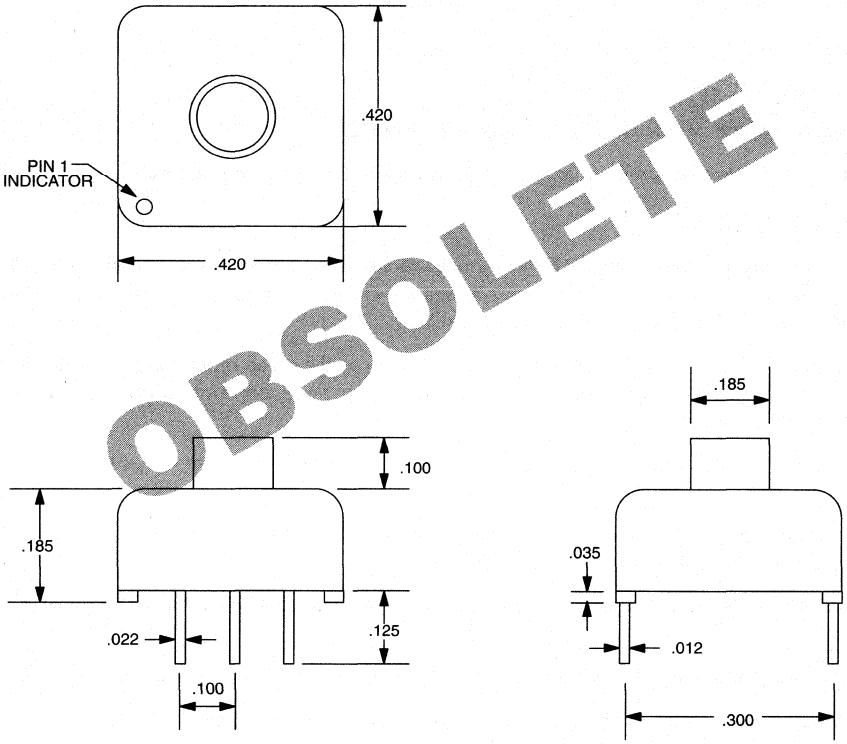
(C) CONTINUOUS PULSE INPUTS



NOTES:

1. All inputs; UV, DC, and D are internally pulled up with a resistance of 100KΩ.
2. Input logic levels are referenced to -V.
3. I_{CC} is the internal current that flows between -V and +V.
4. Input leakage applies to contact inputs UC and DC and digital input (D).
5. Wiper current and rheostat currents are the maximum current which can flow in the resistive elements.
6. Capacitance values apply at 25°C.
7. Input pulse width is the minimum time required for an input to cause an increment or decrement. If the UC, DC or D input is held active for longer than 1 second, subsequent increments or decrements will occur on 100 ms intervals until the inputs UC, DC, and/or D is released to V_{IH}.
8. Repetitive pulsed inputs on UC, DC, or D will be recognized as long as the pulse repetition occurs within 1 second of each other. Pulses occurring faster than 1 ms apart may not be recognized as individual inputs but can be interpreted a constant input.
9. Idle state supply current is measured with no pushbutton depressed and with the wiper. R_W tied to a CMOS load.
10. Maximum time required for the Dallastat to determine single or dual push button operation after input supply has reached 10% recommended supply operating conditions.
11. Aboslute linearity is used to determine wiper voltage versus expected voltage as determined by wiper position.
12. Relative linearity is used to determine the change in voltage between successive tap positions.
13. –3 dB cutoff frequency characteristics for the DS1669 depend on potentiometer total resistance: DS1669–010; 1 MHz, DS1669–050; 200 KHz, DS1669–100; 100 KHz.

DS1668 PUSHBUTTON DIMENSIONS



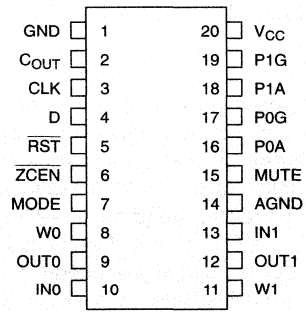
DALLAS SEMICONDUCTOR

DS1800
Dual Inverting Log Gain/Attenuator

FEATURES

- Ultra–low power consumption
- Operates from 3V or 5V supplies
- Two digitally controlled, 128–position potentiometers including mute
- Logarithmic Gain Characteristics
- Zero–crossing detection circuitry eliminates noise caused by discrete wiper position changes
- Two Control Interfaces
  - 3–wire serial CPU control
  - Push–button control
- 20–pin DIP (300 Mil), 20–pin SOIC (300 Mil), and 20–pin (173 Mil) TSSOP packaging available
- Operating Temperature:
  - Commercial: 0°C to 70°C
  - Industrial: –40°C to 85°C
- Software and hardware mute
- Resistance Available: 53KΩ

PIN ASSIGNMENT



20–PIN DIP (300 MIL)
20–PIN SOIC (300 MIL)
20–PIN TSSOP

See Mech. Drawings Section

PIN DESCRIPTION

OUT0,OUT1	–	Low–end of resistor
IN0, IN1	–	High–end of resistor
W0,W1	–	Wiper Terminal
V_{CC}	–	3V or 5V Power Supply Input
$\overline{RST}$	–	Serial Port Reset Input
CLK	–	Serial Port Clock Input
D	–	Serial Port Data Input
C_{OUT}	–	Cascade Data Output
P0G,P1G	–	Gain Input Pot Controls
P0A,P1A	–	Attenuation Input Pot Controls
$\overline{ZCEN}$	–	Zero–Crossing Detect Input
MUTE	–	Hardware Mute Control Input
AGND	–	Analog Ground
GND	–	Ground

DESCRIPTION

The DS1800 is a dual audio–taper potentiometer designed specifically for use in the feedback path of the inverting configuration of an operational amplifier (see Figure 2). In this configuration, the DS1800 provides a V_O/V_I relationship of $-20\log(R_F/R_I)$ giving a gain/attenuation range covering +20 dB to –63 dB. Each potentiometer has a total of 129 positions including mute. The DS1800 provides five areas of resolution which include 0.25 dB per step from +20 dB to +3 dB, 0.5 dB per step from +3 dB to –12 dB, 1 dB from –12 dB to –27 dB, and from –27 dB to –47 dB; 2 dB per step, and from –47 dB to –63 dB; 4 dB per step. The mute position provides 100 dB of attenuation.

The DS1800 has two control interfaces (see Figure 1). The first is a 3–wire serial CPU interface consisting of $\overline{RST}$, CLK, and D. The second interface is a contact–closure interface, allowing easy push–button control

without the need for external debounce or timing circuitry. The device also provides for software muting (via CPU) or hardware muting (MUTE control input). The hardware mute is a toggle type which returns the wiper positions to their prior states. Additional information on CPU and push–button control is described under the section entitled "OPERATION".

The DS1800 is available in 20–pin DIPs, SOICs, and TSSOPs. One standard resistance grade of 53KΩ is available for the device.

OPERATION

The DS1800 provides two 129–position 45KΩ potentiometers. These potentiometers are specifically designed to operate in the configuration shown in Figure 2. Under this configuration the V0/VI relationship provides the gain/attenuation function of $-20\log(R_F/R_I)$ over a range of +20 dB to –63 dB. This function is illustrated in Figure 3 as a graph of gain/attenuation versus position. Figure 4 provides the relationship between R_F and R_I as a function of position.

The DS1800 has a total of 129 positions including a mute position. Five areas of resolution are provided over the gain/attenuation range and are illustrated in Figure 3. From position 0 to position 68, a resolution of 0.25 dB per step is attained covering a gain/attenuation range of +20 dB to +3 dB. From position 68 to position 98, 0.5 dB per step of resolution is attained covering +3 dB to –12 dB of gain/attenuation. Positions 98 to 113 have 1 dB per step resolution and cover a gain/attenuation range of –12 to –27 dB. Positions 113 to 123 provide 2 dB per step and cover a gain/attenuation range of –27 dB to –47 dB. Positions 123 to 127 provide 4 dB per step and cover a gain/attenuation range of –47 dB to 63 dB. Position 128 is the mute position and typically provides 100 dB of attenuation.

PIN DESCRIPTIONS

The DS1800 has a total of 20 pins which provide various functions for the device. This section provides a description of each pin's operation.

V_{CC} – Power Supply Voltage Input. The DS1800 will support 3V or 5V power supply operation.

GND – Ground. The DS1800 has two ground pins. The GND supports the digital ground for the device.

AGND – Analog Ground. The DS1800 has two ground pins. The AGND supports analog ground for the device.

IN0, IN1 – Input terminals for the two respective potentiometers as shown in Figure 2. These terminals should be connected to the analog signal,VI, to provide the gain/attenuation characteristics stated. These terminals are referenced as INx in the Figure 2 drawing.

OUT0, OUT1 – Analog Outputs. These pins should be connected to the output terminal of the operational amplifier as shown in Figure 2. These inputs are referenced as OUTx in the Figure 2 drawing.

W0, W1 – Wiper Terminals. The wiper terminals of each pot are connected to the inverting terminal of the operational amplifier. The position of the wiper terminal is selected either through CPU control or push–button control.

P0A, P1A – Attenuation Push–button Inputs. These push–button inputs are used to control wiper position of the part . Activity on these inputs will cause the position of the wiper to move towards the OUT0, and OUT1 terminals, respectively.

P0G, P1G – Gain Push–button Inputs. These push–button inputs control wiper position and are used to move the position of the wiper towards the IN0 and IN1 terminals, respectively.

$\overline{RST}$ – Serial Port Reset. The $\overline{RST}$ input deactivates the 3–wire serial interface. This input is active when in the low–state. All 3–wire communications must take place when this input is in a high state.

CLK – Serial Clock Input. The CLK input is the positive–edge clock signal input used for 3–wire timing synchronization.

D – Serial Data Input. The D input is used to input serial data for wiper position changes.

C_{OUT} – Serial Cascade Output. The C_{OUT} is an output signal used to read the contents of the current settings of the wiper positions. As data is clocked into the D input, data corresponding to the wipers are shifted out of the C_{OUT} pin.

MODE – Push–button Debounce Control. The MODE pin is used to choose between a fast and slow mode of push–button debouncing. When in a high state, push–button debounce is slow. When in a low–state, push–button debounce is faster. These timing differences are discussed in the section entitled "Push–button Interface Control". The state of this pin is determined only at device power–up.

POWER–UP CONDITIONS

The position of the wipers of the DS1800 on power up are internally set to position 127, which is the last position before mute. The user then has the responsibility of changing the wiper position to the desired attenuation/gain levels.

Additionally, the serial port is stable and active within 10 microseconds. The contact closure control interface inputs are active after 50 ms.

INTERFACE CONTROL OPTIONS

Control of the DS1800 is provided via two types of interface ports. A 3–wire CPU control interface allows the exact wiper positions of the potentiometers to be written using two 8–bit words. A cascade output, C_{OUT}, is provided when controlling multiple devices via one CPU or when reading the wiper positions of each potentiometer.

The second interface is a contact closure interface that allows push–buttons to control movement of the wiper positions. Under push–button control no external debounce or timing circuitry is needed. A block diagram of the DS1800 is shown in Figure 1.

3–WIRE SERIAL INTERFACE CONTROL

CPU control of the DS1800 is accomplished using the 3–Wire serial port of the device. This interface drives an internal control logic unit. Direct wiper positioning is accomplished by using this port which consist of three input signals: $\overline{RST}$, CLK, and D.

The $\overline{RST}$ control signal is used to enable 3–wire serial port write operations. The CLK terminal is an input that provides synchronization for data I/O. Data is input bit by bit via the D input signal pin.

The 3–Wire serial timing diagrams are provided in Figure 5. Serial port operation or activity begins with the transition of the $\overline{RST}$ signal from a low–state to a high–state. Once activated, data is clocked into the part on the low to high transition of the CLK signal input. Data input via the D terminal is transferred in order of the desired potentiometer–0 wiper value, followed by the potentiometer–1 wiper position value.

Two 8–bit values are used to store wiper position for each potentiometer during powered conditions. These 8–bit values are written to a 16–bit I/O shift register. A detailed diagram of the 16–bit I/O shift register is shown in Figure 6.

Bits 0 through 7 are reserved for the positioning of wiper–0 while bits 8 through 15 are reserved for control of wiper–1. Bits 0 through 6 are used for actual wiper positioning of potentiometer–0. Bit 7 is used to mute potentiometer–0. If this bit is set to a "1", the potentiometer–0 wiper will be connected to the OUT0 end of the resistor array regardless of the settings of bits 0 through 6.

Bits 8 through 15 are used for positioning the wiper of potentiometer–1. Bits 8 through 14 control wiper position on the resistor array. Bit 15 is used for muting potentiometer–1. Bit 15, like bit 7, when set to "1" will mute potentiometer 1, regardless of the settings of bits 8 through 14.

Data is transmitted LSB first starting with bit–0. A complete transmission of 16 bits of data is required to insure proper setting of each potentiometer's wiper. An incomplete transmission may result in undesired wiper settings.

Once the 16 bits of information has been transmitted and the $\overline{RST}$ signal input transitions to a low–state, the new wiper positions are loaded into the part.

PUSH–BUTTON INTERFACE CONTROL

The DS1800 can be configured to operate from contact closure or push–button inputs. The push–button inputs consist of signals P0A, P0G, P1A, P1G and MUTE. P0A and P0G allow attenuation and gain control of the input signal to potentiometer–0, while P1A and P1G provide the same control for potentiometer–1. The MUTE input provides a toggle control for muting the potentiometers via pushbutton.

The P0A and P1A control inputs, based on the recommended circuit configuration, are used to attenuate the incoming signal by moving the wiper position towards the OUTx terminals. The P0G and P1G control inputs

provide the opposite function; positioning the wiper(s) closer to the INx terminals, thus providing gain.

Each of these control inputs are internally pulled–up via a 50KΩ resistance. Additionally, these inputs require no external components for debouncing or timing which are provided internal to the part.

Contact closure is defined as the transition from a high level to a low level on these input terminals. The DS1800 interprets input pulse widths as the means of controlling wiper movement. A single pulse input over the PxA or PxG input terminals will cause the wiper to move one position. A transition from high to low on these inputs is considered the beginning of pulse activity or contact closure. The DS1800 has two timing modes for controlling the speed at which pushbuttons will operate. These modes are termed fast mode operation and slow mode operation.

In slow mode operation, a single pulse is defined as being greater than 1 ms but lasting no longer than 0.8 seconds. Correspondingly, in fast mode operation, a single pulse is defined as being greater than 50 µs but lasting no longer than 0.8 second.

Repetitive pulsed inputs can be used to step through each resistive position of the device in a relatively fast manner. The timing requirements for repetitive pulsed inputs is that pulses must be separated by a minimum time of 1 ms for slow mode operation and 50 µs for fast mode operation.

Pulse inputs lasting longer than 0.8 seconds will cause the wiper to move one position every 25 ms seconds after the initial 0.8 second hold time. This is true regardless of the mode input. The total time required to transcend the entire potentiometer using a continuous input pulse is given by the following formula:

0.8(seconds) + 127 x 25 ms = 3.975(seconds)

SLOW MODE AND FAST MODE OPERATION

Pushbutton operation, as mentioned. can be operated at two distinct speeds or modes; fast and slow. The mode or speed of pushbutton debounce is determined at device power–up by the state of the MODE pin. When MODE powers to a high–state, pushbutton debounce timing will operate at the slow mode rate. When powered and in the low–state, debounce timing operates at the fast rate. Timing specifications for pushbutton operation can be found in the AC Electrical Specification Table for pushbutton operation. Timing diagrams for push–button operation can be found in Figure 7.

ZERO CROSSING DETECTION

The DS1800 provides a zero–crossing detection capability when using the 3–Wire serial interface. Zero–crossing detection provides a means for minimizing unwanted audible noise that may result from sizable discrete wiper transitions when using the part in audio applications. The zero crossing detect feature allows independent wiper changes only when the two terminals of the potentiometer(s) have equal potentials and within a 50 ms time window from the fall of the $\overline{RST}$ signal. If at 50 ms the DS1800 has not detected a zero crossing, the wiper position of the potentiometer(s) will change regardless of the state of the input signal. Zero–crossing detection is activated when the $\overline{ZCEN}$ input is in a low–state. When high, the $\overline{ZCEN}$ input deactivates both the 50 ms time requirement and zero–detection crossing.

Zero crossing detection is also available when using the part in push–button operation. When a push–button is activated, the part will change wiper position during the first detected zero–crossing or at the end of a 50 ms time window.

When operating in push–button operation with a continuous input pulse, the wiper position will change once during the initial 0.8 second time period. This change is dictated by a detected zero–crossing or 50 ms time window. Subsequent changes when operating with a continuous input pulse occur on 25 ms time intervals and are dependent on zero crossings or 50 ms time–outs.

MUTE CONTROL

The DS1800 provides a mute control feature which can be accessed by the user through hardware or software. Hardware control of the device is achieved through the MUTE input pin. This pin is internally pulled up through a 50K resistor and functions like the PxG and PxA push-button controls. When this input is driven low, the wiper outputs of both potentiometers will be internally connected to the OUTx terminal of their respective potentiometers. This input performs as a toggle input, with the first activity on this pin connecting the wiper terminals to the OUTx terminals (position 128) of the potentiometer. The next input activity on this pin will return the wiper position to the previous state before muting occurred.

Also, if operating in push–button mode, MUTE will be deactivated if an input is received over any push–button input. This input, like the push–button inputs, is internally debounced and requires no external circuitry. When the device powers up, the first activity on the mute pin will move the wipers to position 128 or the OUTx end of the potentiometer(s).

Software muting was discussed in the 3–wire serial control section. Bits 7 and 15 are reserved for muting each respective potentiometer. If these bits have value "1", the wiper positions of the pot will be transferred to the mute position. Unlike hardware mute control, software muting allows the user individual control of each potentiometer. Additionally, the software mute requires that the complete wiper position setting be rewritten to establish a non muted position. Note that bits 7 and 15 of the I/O shift register must have value "0" to release the software mute position.

CASCADE OPERATION

A feature of the DS1800 is the ability to control multiple devices from a single processor. Multiple DS1800's can be linked or daisy chained as shown in Figure 8. As a data bit is entered into the I/O shift register of the DS1800, a data bit will appear at the C_{OUT} output after a maximum delay of 50 nanoseconds.

The C_{OUT} output of the DS1800 can be used to drive the D input of another DS1800. When connecting multiple devices, the total number of bits sent is always 16 times the number of DS1800's is the daisy chain.

An optional feedback resistor can be placed between the C_{OUT} terminal of the last device and the D input of the first DS1800, thus allowing the controlling processor to circularly clock data through the daisy chain. The value of the feedback or isolation resistor should be in the range from 2K to 20KΩ.

When reading data via the C_{OUT} pin and the isolation resistor, the D input is left floating by the reading device. When $\overline{RST}$ is driven high, bit–0 is present on the C_{OUT} pin, which is fed back to the D pin through the isolation resistor. When the CLK input transitions low to high, bit–0 is loaded into the first position of the I/O shift register and bit 1 becomes present on C_{OUT} and D of the next device. After 16 bits (or 16 times the number of DS1800s in the daisy chain), the data has shifted completely around and back to its original position. When $\overline{RST}$ transitions to the low state to end data transfer, the value (the same as before the read occurred is loaded into the wiper–0 and wiper–1 registers.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–1.0V to +7.0V
Operating Temperature	0°C to 70°C; commercial –40°C to +85°C; industrial
Storage Temperature	–55°C to 125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(–40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	2.7		5.5	V	1
Input Logic 1	V_{IH}	2.0		V_{CC}+0.5	V	1, 2
Input Logic 0	V_{IL}	–0.5		+0.8	V	1, 2
Analog Ground	AGND	GND–0.5		GND+0.5		14
Resistor Inputs	L,H,W	GND–0.5		GND+0.5	V	1

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC}=2.7V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}			2000	µA	10
Input Leakage	I_{LI}	–1		+1	µA	
Wiper Resistance	R_W		400	1000	Ω	
Wiper Current	I_W			1	mA	
Logic 1 Output Current @ 2.4V	I_{OH}	–1			mA	
Logic 0 Output Current @ 0.4V	I_{OL}			4	mA	
Standby Current: 3 Volts 5 Volts	I_{STBY}		12 20	 40	µA µA	12
Power Up Time	t_{PU}		50		ms	8

ANALOG RESISTOR CHARACTERISTICS

(–40°C to +85°C; V_{CC}=2.7V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Total Resistance			53		KΩ	
End–to–End Resistor Tolerance		–20		+20	%	
Absolute Tolerance		–0.5 –1.0		+0.5 +1.0	dB dB	9
Tap–to–Tap Tolerance		–0.5		+0.5	dB	7
Interchannel Matching		–0.25 –0.5		+0.25 +0.5	dB dB	6
–3 dB Cutoff Frequency	f_{cutoff}		1		MHz	13
Temperature Coefficient			650		ppm/°C	
Total Harmonic Distortion (V_{IN}=1Vrms, 20 Hz to 20 KHz, Tap=0 dB)	THD		0.002		%	13
Output Noise (20 Hz to 20 KHz, Grounded Input, Tap=0 dB)			2.2		µVrms	13
Digital Feedthrough (20 Hz to 20 KHz, Tap=0 dB)			–90		dB	13
Interchannel Isolation (1 KHz, Tap=0 dB)			–100		dB	13
Mute Control Active	MUTE		–100		dB	

CAPACITANCE

(–40°C to +85°C; V_{CC}=2.7V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC}=2.7V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CLK Frequency	f_{CLK}	DC		10	MHz	
Width of CLK Pulse	t_{CH}	50			ns	
Data Setup Time	t_{DC}	30			ns	
Data Hold Time	t_{CDH}	10			ns	
Propagation Delay Time Low to High Level High to Low Level	t_{PLH}			50	ns	
$\overline{RST}$ High to Clock Input High	t_{CC}	50			ns	
$\overline{RST}$ Low from Clock Input High	t_{HLT}	50			ns	
CLK Rise Time	t_{CB}			50	ns	
$\overline{RST}$ Inactive	t_{BLT}	200			ns	

AC ELECTRICAL CHARACTERISTICS PUSHBUTTON INPUTS

(–40°C to +85°C; V_{CC}=2.7V to 5.5V)

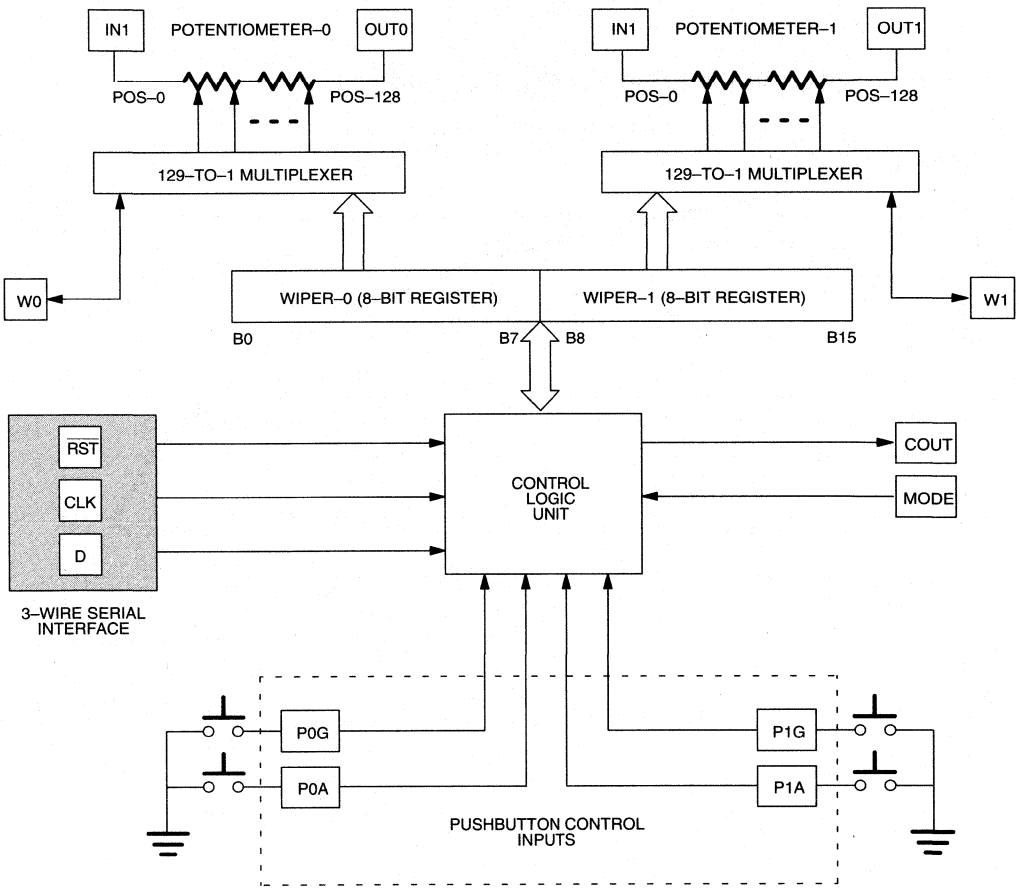
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Single Pulse Input Slow Mode Fast Mode	t_{CPW}	 1 50		800	 ms µs	3, 5, 11
Repetitive Input Pulse High Time Slow Mode Fast Mode	t_{HPW}	 1 50		800	 ms µs	3, 5, 11
Continuous Input Pulse	t_{CCP}	0.8		DC	s	3, 5, 11

NOTES:

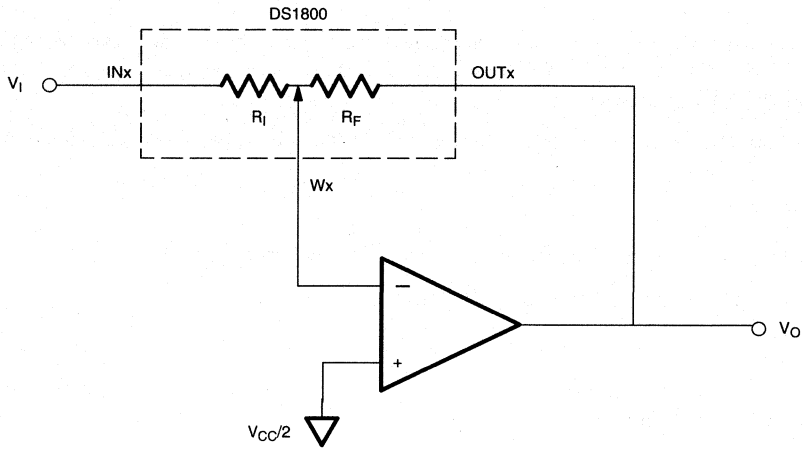
1. All voltages are referenced to ground
2. Valid for V_{CC} = 5V only.
3. Both PxA and PxG inputs are internally pulled up with a 50KΩ resistance.
4. Capacitance values apply at 25°C.
5. Input pulse width is the minimum time required for an input to cause an increment or decrement of wiper position. If the PxA or PxG inputs are held active for longer than 0.8 seconds, subsequent increments or decrements will occur at intervals of 25 ms. Timing tolerances for pushbutton control are specified at 35%.
6. Inter–Channel Matching is used to determine the relative voltage difference in dB between the same position on each potentiometer. The DS1800 is specified for ±0.25 dB inter channel matching from position 0 to position 112 (+20 dB to –27 dB) and ±0.5 dB from position 113 to position 127.
7. Tap–to–Tap tolerance is used to determine the change in voltage between successive tap positions. The DS1800 is specified for ±0.5 dB tap–to–tap tolerance. From position 0 to position 112 (+20 dB to –27 dB). From position 113 to position 127, the DS1800 is specified for ±1 dB tap–to–tap tolerance.

8. Power–up time is the time for all push–button inputs to be stable and active once power has reached a valid level, 2.7V min.
9. Absolute tolerance is used to determine wiper voltage versus expected wiper voltage as determined by wiper position. The DS1800 is bounded by a ±0.5 dB absolute tolerance from position 0 to position 112 and ±1 dB tolerance from position 113 to position 127.
10. Maximum current specifications are based on clock rate, active zero–crossing detection, and push–button activation.
11. Valid for V_{CC} =3V or 5V.
12. Standby current levels apply when all inputs are driven to appropriate supply levels.
13. These parameters are characterized and not 100% tested.
14. See Figure 9.

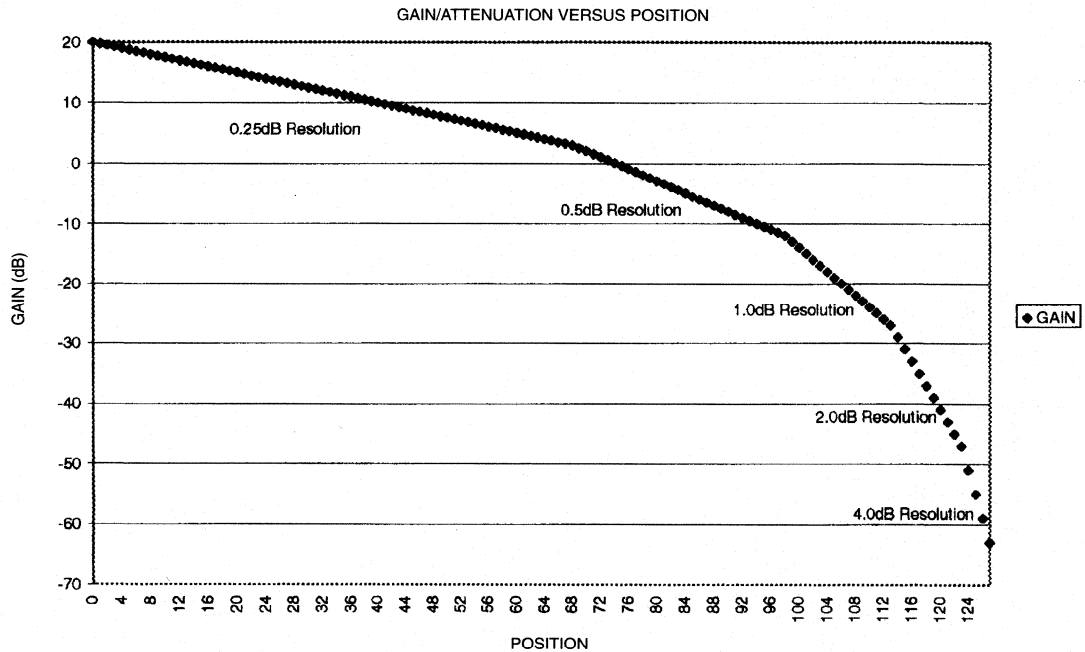
DS1800 BLOCK DIAGRAM Figure 1



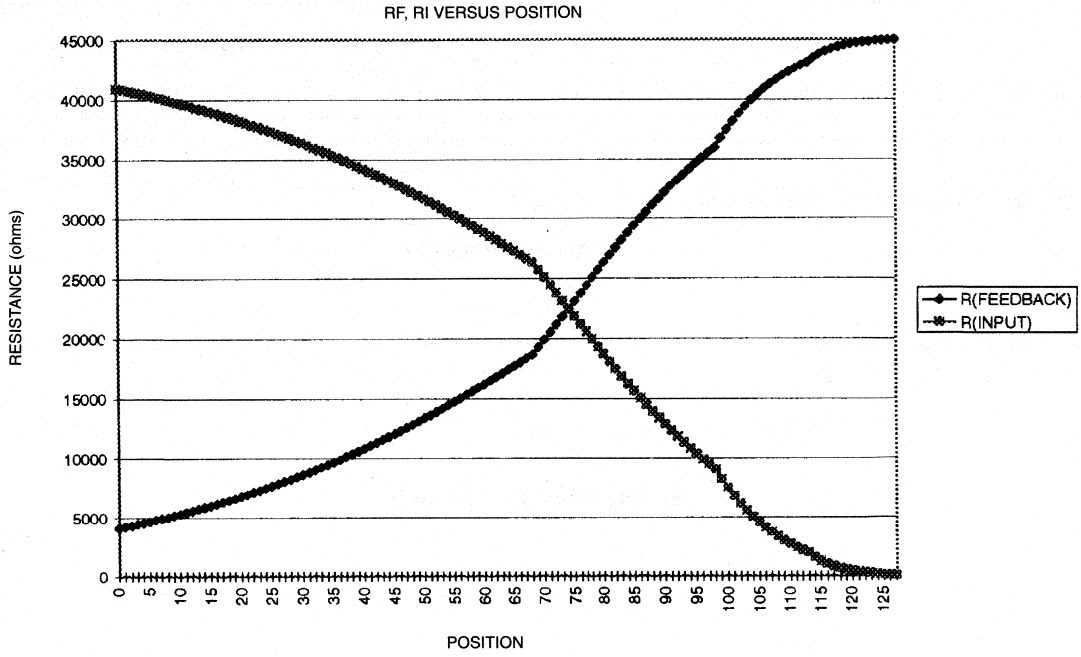
RECOMMENDED CIRCUIT CONFIGURATION Figure 2



V_O/V_I GAIN/ATTENUATION VS. POSITION RELATIONSHIP Figure 3



R_F/R_I RELATIONSHIP VS. POSITION Figure 4



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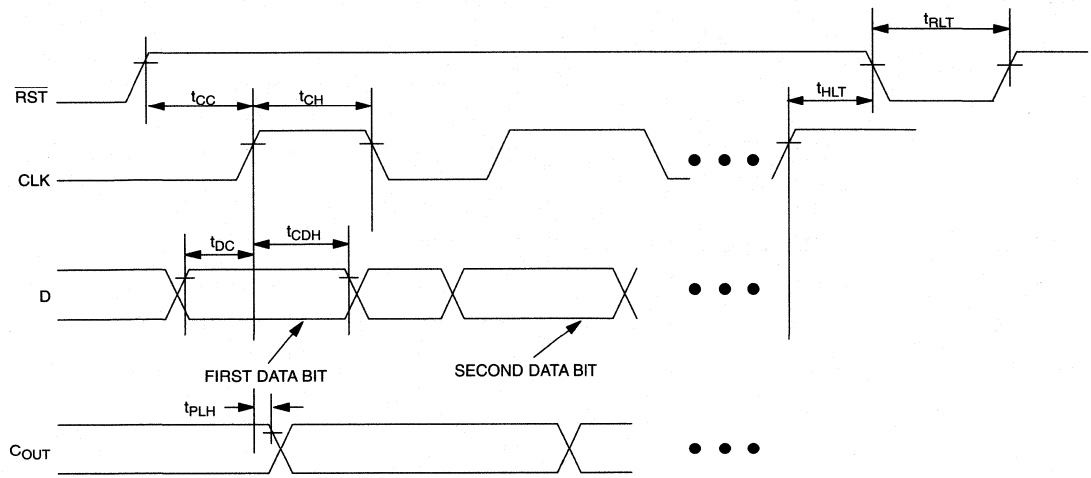
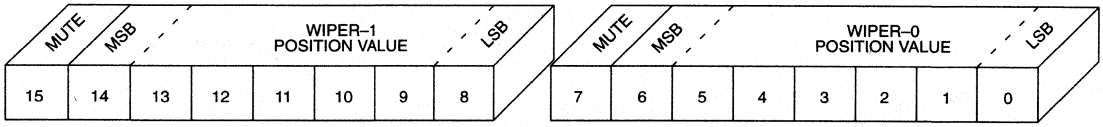
3–WIRE SERIAL TIMING DIAGRAM Figure 5

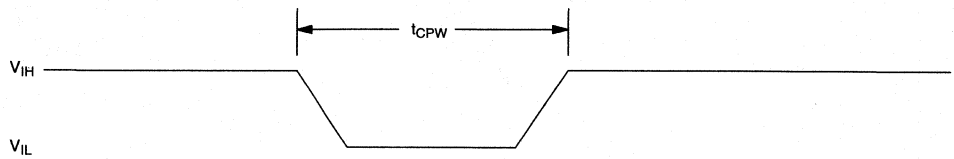


16–BIT I/O SHIFT REGISTER Figure 6

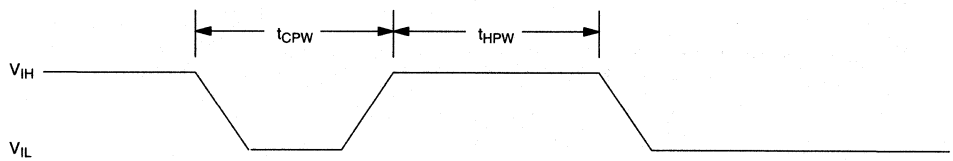


CONTACT CLOSURE TIMING DIAGRAMS Figure 7

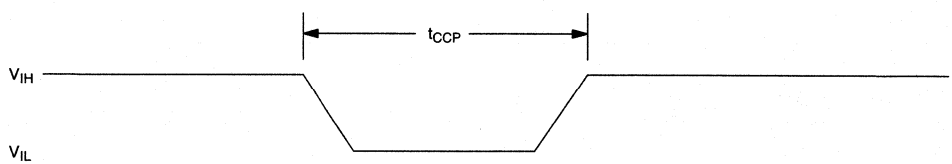
(a) Single Pulse Inputs



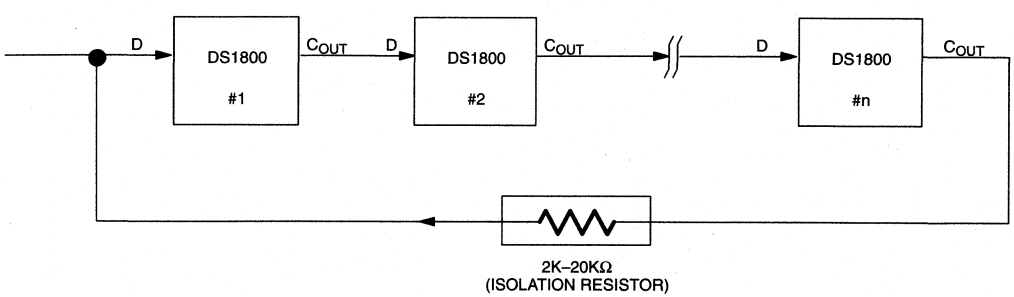
(b) Repetitive Pulse Inputs



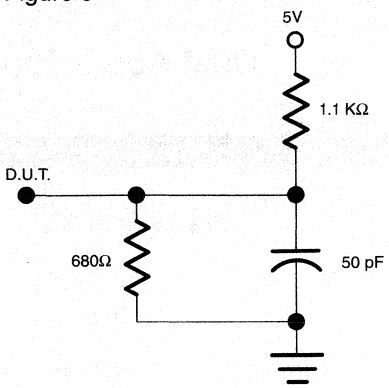
(c) Continuous Pulse Inputs



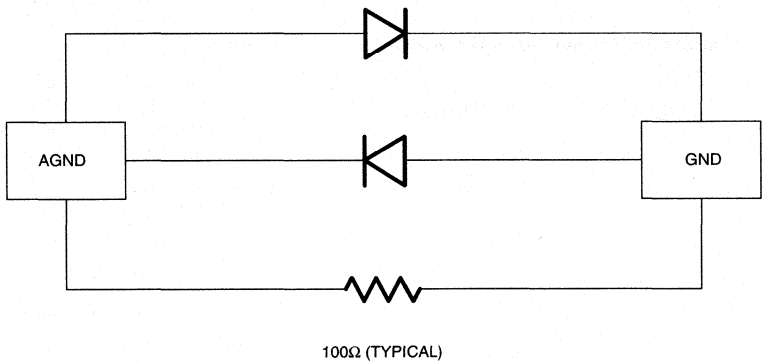
CASCADING OPERATION Figure 8



DIGITAL OUTPUT LOAD Figure 9



INTERNAL GROUND CONNECTIONS Figure 10



NOTE: GND and AGND must be tied to the same voltage level.

PRODUCT PREVIEW

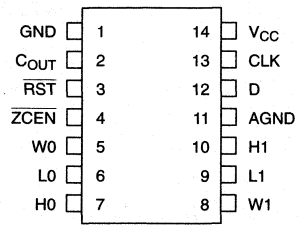
DALLAS SEMICONDUCTOR

DS1801
Dual Audio Taper Potentiometer

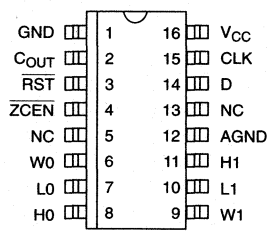
FEATURES

- Ultra–low power consumption
- Operates from 3V or 5V supplies
- Two digitally controlled, 65–position potentiometers including mute
- Logarithmic resistive characteristics (1 dB per step)
- Zero–crossing detection eliminates noise caused by wiper movement
- Serial port provides means for setting and reading both potentiometer wipers
- 14–pin PDIP, 16–pin SOIC, and 14–pin TSSOP packages
- Temperature:
  - Commercial: –20°C to +70°C
- Software mute

PIN ASSIGNMENT



14–PIN PDIP, TSSOP



16–PIN SOIC (300 MIL)
See Mech. Drawings Section

DESCRIPTION

The DS1801 is a dual audio taper potentiometer having logarithmic resistive characteristics over the device range. Each potentiometer provides 65 wiper positions with a 1 dB increment per step and device mute. The 3–wire serial interface, using a CPU, provides the user the ability of reading or writing exact wiper positions of the two potentiometers. Additionally, the part contains a zero–crossing detection feature that minimizes noise resulting from wiper transitions. Packages for the part include a 14–pin PDIP, 16–pin SOIC, and 14–pin TSSOP.

PIN DESCRIPTION

L0, L1	–	Low End of Resistor
H0, H1	–	High End or Resistor
W1, W2	–	Wiper End of Resistor
V_{CC}	–	3V/5V Power Supply Input
$\overline{RST}$	–	Serial Port Reset Input
D	–	Serial Port Data Input
CLK	–	Serial Port Clock Input
GND	–	Digital Ground
AGND	–	Analog Ground
$\overline{ZCEN}$	–	Zero Crossing Detect
C_{OUT}	–	Cascade Output
NC	–	No Connect

OPERATION

The DS1801 provides two 65–position potentiometers per package; each having a logarithmic resistive characteristic as shown in Table 1. The DS1801 is controlled by a 3–wire serial interface. The 3–wire serial interface is designed for CPU controlled applications and allows the potentiometer's exact wiper position to be read or written. The DS1801 design supports daisy chaining for multi–device environments.

Figure 1 presents a block diagram of the DS1801. As shown, the inputs from the 3–wire serial interface drive a command/control unit. The command/control unit interprets these inputs for control of the two potentiometers.

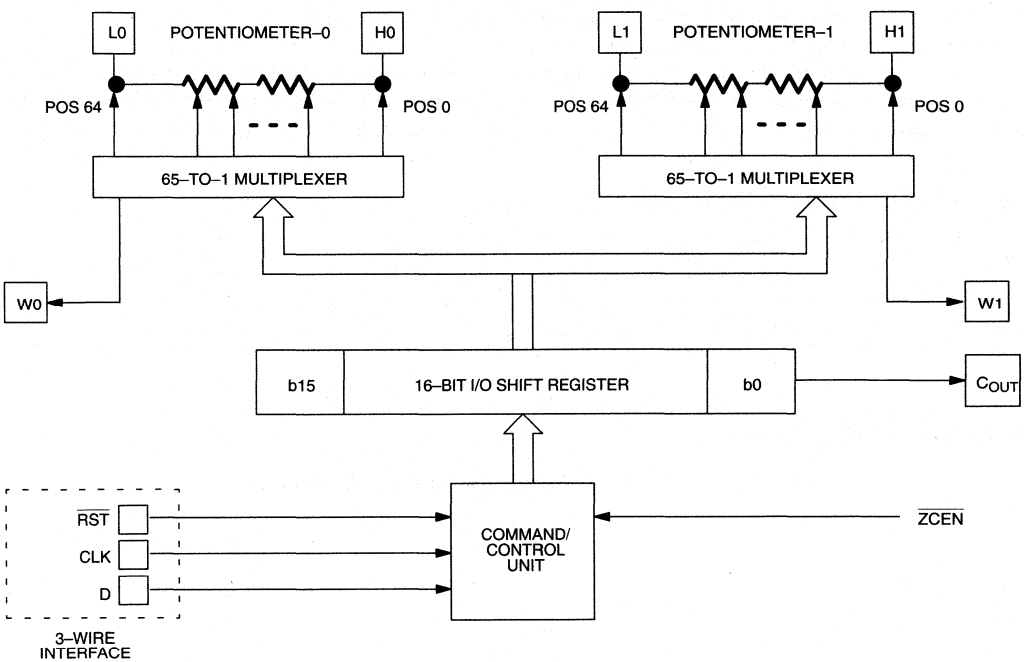
On power–up the serial port is stable and active within 10 microseconds. The wiper position on power–up will be at position 63, the low end of the potentiometer. Position 64 is the mute level.

RESISTANCE CHARACTERISTICS Table 1

POSITION	OUTPUT LEVEL (dB)
0	0
1	–1
2	–2
3	–3
4	–4
5	–5
•	•
•	•
•	•
63	–63
64 (mute)	< –90

4

DS1801 BLOCK DIAGRAM Figure 1



3–WIRE SERIAL INTERFACE CONTROL

Communication and control of the DS1801 is accomplished through a 3–wire serial port interface that drives an internal control logic unit. The 3–wire serial interface is designed for microprocessor or microcontroller applications. The interface consists of three input signals which include $\overline{RST}$, CLK and D.

The $\overline{RST}$ control signal is used to enable 3–wire serial port write operations. The CLK terminal is a clock signal input that provides synchronization for data I/O while the D signal input serves to transfer potentiometer wiper position settings to the device.

As shown in Figure 3, a 3–wire serial port operation begins with a transition of the $\overline{RST}$ signal input to a high state. Once the 3–wire port has been activated, data is clocked into the part on the low to high transition of the CLK signal input. Data input via the D line is transferred in order of the desired potentiometer–0 value followed by the potentiometer–1 value.

The DS1801 contains two 65–position potentiometers whose wiper positions are set by an 8–bit value. These two 8–bit values are written to the 16–bit I/O shift register which is used to store wiper position during powered conditions. Because the potentiometer has 65–positions, only seven bits of data are needed to set wiper position. A detailed diagram of the 16–bit I/O shift register is shown in Figure 2. Bits 0 through 7 are reserved for the potentiometer–0 control while bits 8 through 15 are reserved for control of potentiometer–1.

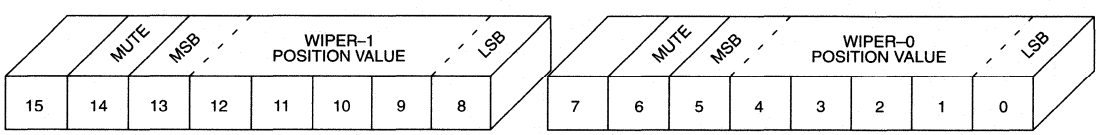
Bits 0 through 5 are used for actual wiper positioning for potentiometer–0. Bit 6 is used to mute potentiometer–0. If this bit has value "1", the potentiometer–0 wiper will be connected to the low end of the resistive array the mute position. The value of bit 7 is a don't care and will not affect operation of the DS1801 or potentiometer–0.

Bits 8 through 13 are used for wiper positioning of potentiometer–1. Bit 14 is used for muting of the potentiometer–1 wiper output. Bit 15, like bit 7, is a don't care and will not affect operation of the DS1801.

Data for the DS1801 is transmitted LSB first starting with bit 0. A complete transmission of 16 bits of data is required to insure proper setting of each potentiometer's wiper. An incomplete transmission may result in undesired wiper settings.

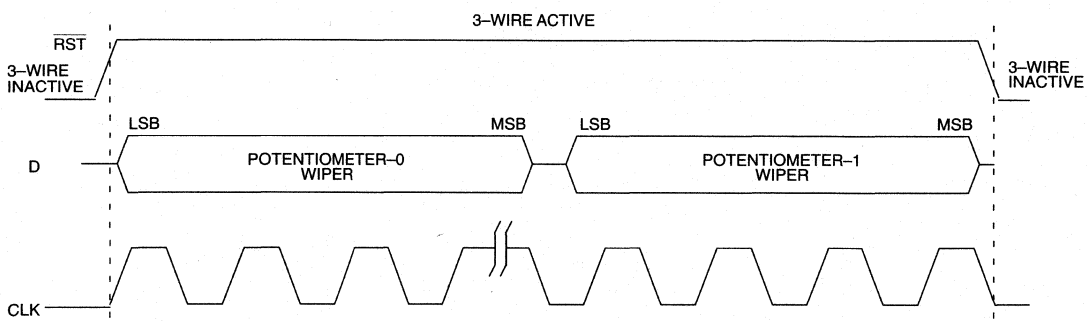
Once the complete 16 bits of information has been transmitted and the $\overline{RST}$ signal input transitions to a low state, the new wiper positions are loaded into the part.

16–BIT I/O SHIFT REGISTER Figure 2



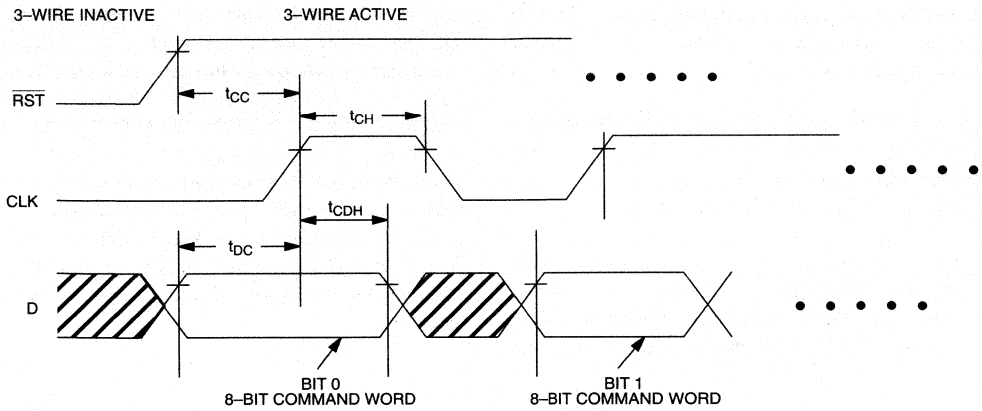
TIMING DIAGRAMS Figure 3

(a) 3–Wire Serial Interface General Overview

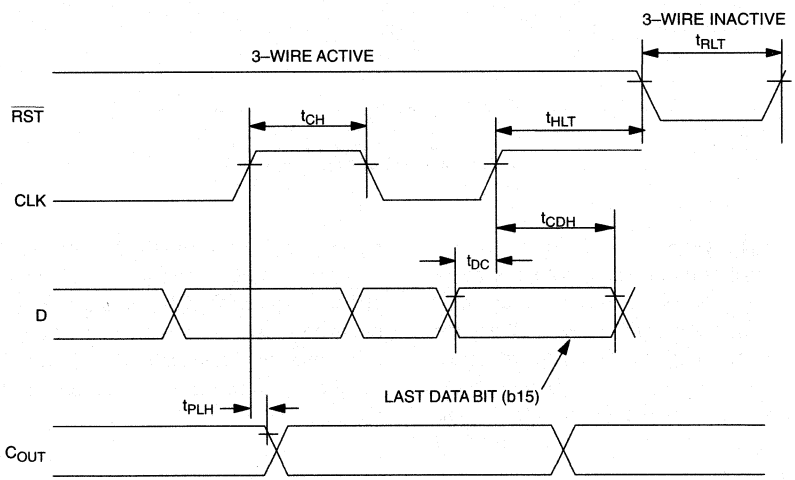


TIMING DIAGRAMS Figure 3 (cont'd)

(b) Start of Communication Transaction



(c) End of Communication Transaction



CASCADE OPERATION

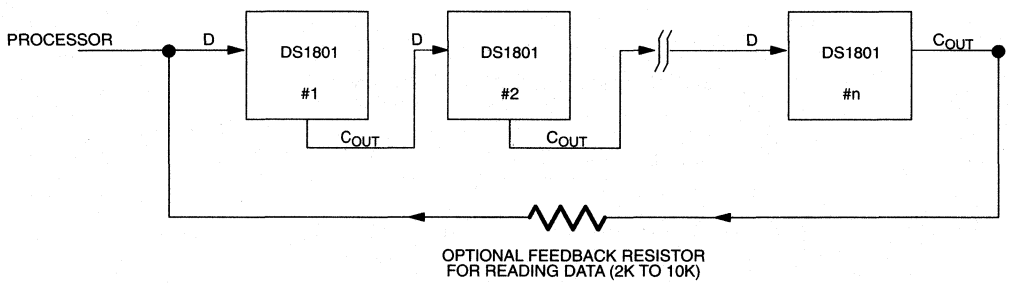
A feature of the DS1801 is the ability to control multiple devices from a single processor. Multiple DS1801's can be linked or daisy chained as shown in Figure 4. As a data bit is entered into the I/O shift register of the DS1801 it will appear at the C_{OUT} output after a maximum delay of 50 nanoseconds.

The C_{OUT} output of the DS1801 can be used to drive the D input of another DS1801. When connecting multiple devices, the total number of bits sent is always 16 times the number of DS1801s in the daisy chain.

An optional feedback resistor can be placed between the C_{OUT} terminal of the last device and the D input of the first DS1801 thus allowing the controlling processor to read, as well as write data, or circularly clock data through the daisy chain. The value of the feedback or isolation resistor should be in the range from 2K to 10K ohms.

When reading data via the C_{OUT} pin and isolation resistor, the D line is left floating by the reading device. When $\overline{RST}$ is driven high, bit 0 is present on the C_{OUT} pin, which is fed back to the input D pin through the isolation resistor. When the CLK input transitions low to high, bit 0 is loaded into the first position of the I/O shift register and bit 1 becomes present on C_{OUT} and D of the next device. After 16 bits (or 16 times the number of DS1801s in the daisy chain), the data has shifted completely around and back to its original position. When $\overline{RST}$ transitions to the low state to end data transfer, the value (the same as before the read occurred) is loaded into the wiper–0 and wiper–1.

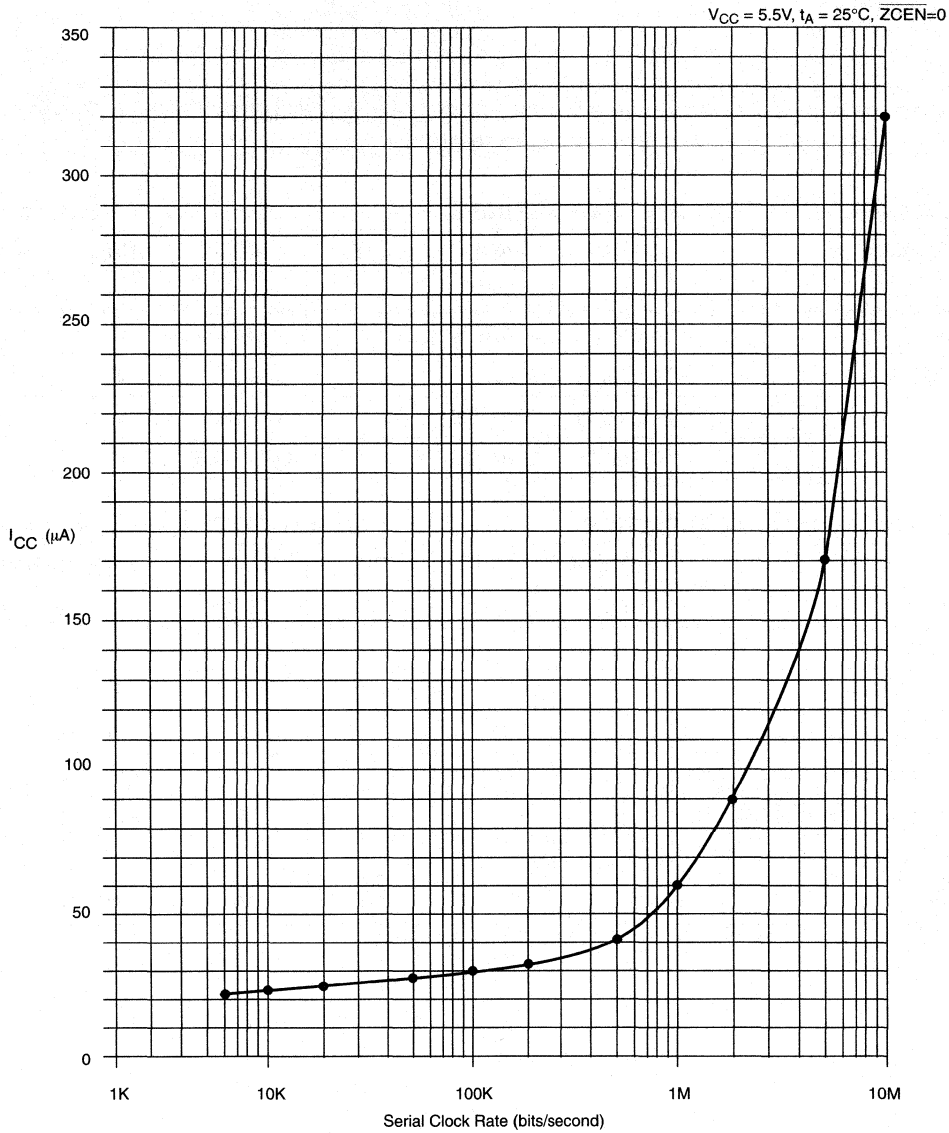
CASCADING MULTIPLE DEVICES Figure 4



Zero Crossing Detection

The DS1801 provides a zero–crossing detection capability that minimizes any audible noise that may result from sizable discrete wiper transitions when using the part in audio applications. The zero crossing detect feature allows independent wiper changes only when the two terminals of the potentiometer have equal potentials and within a 50 ms time window from the fall of the $\overline{RST}$ signal. If at 50 ms the DS1801 has not detected a zero crossing, the wiper position of the potentiometer(s) will change regardless of the state of the input signal. Zero–crossing detection is activated when the $\overline{ZCEN}$ input level is in a low–state. When high, the $\overline{ZCEN}$ input deactivates both the 50 ms time requirement and zero–detection crossing.

TYPICAL SUPPLY CURRENT VS. SERIAL CLOCK RATE Figure 5



4

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground and AGND	–0.7V to +7.0V
Operating Temperature	–20°C to +70°C commercial
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(–20°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	+2.7		5.5	V	
Input Logic 1	V_{IH}	2.0		V_{CC}+0.5	V	1, 2
Input Logic 0	V_{IL}	–0.5		+0.8	V	1, 2
Resistor Inputs	L, H, W	GND–0.5		V_{CC}+0.5	V	2
Analog Ground	AGND	GND–0.5		GND +0.5	V	10

DC ELECTRICAL CHARACTERISTICS

(–20°C to +70°C; V_{CC}=3V and 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}			2000	µA	9
Input Leakage	I_{LI}	–1		+1	µA	
Wiper Resistance	R_W		400	1000	Ω	
Wiper Current	I_W			1	mA	
Logic 1 Output Current @ 2.4 Volts	I_{OH}	–1.0			mA	2
Logic 0 Output Current @ 0.4 Volts	I_{OL}			4	mA	2
Standby Current 3 Volts 5 Volts			 12 20	 40	 µA µA	11

ANALOG RESISTOR CHARACTERISTICS

(–20°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Total Resistance			45		KΩ	
Absolute Tolerance		–1		+1	dB	8
Inter–Channel Matching		–0.5		+0.5	dB	4
Tap–to–Tap Tolerance		–0.25		+0.25	dB	5, 12
–3 dB Cutoff Frequency	f_{CUTOFF}		700		KHz	
Temperature Coefficient			650		ppm/°C	
Total Harmonic Distortion (V_{IN}=1V_{RMS}, 1 KHz, Tap= –6 dB)	THD		0.002		%	12
Output Noise (20 Hz to 20 KHz, Grounded Input, Tap= –6 dB)			2.2		μV_{RMS}	
Digital Feedthrough (20 Hz to 20 KHz, Tap= –6 dB)			–90		dB	12
Interchannel Isolation (20 Hz to 20 KHz, Tap= –6 dB)			–100		dB	12
Mute Control Active	Mute		–90		dB	

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CAPACITANCE

(–20°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	6
Output Capacitance	C_{OUT}			7	pF	6

AC ELECTRICAL CHARACTERISTICS

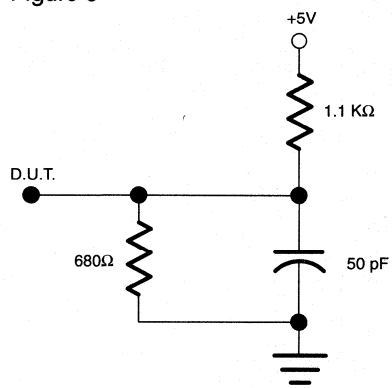
(–20°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CLK Frequency	f_{CLK}	DC		10	MHz	7
Width of CLK Pulse	t_{CH}	50			ns	7
Data Setup Time	t_{DC}	30			ns	7
Data Hold Time	t_{CDH}	10			ns	7
Propagation Delay Time Low to High Level Clock to Output	t_{PLH}			50	ns	7
Propagation Delay Time High to Low Level	t_{PLH}			50	ns	7
$\overline{RST}$ High to Clock Input High	t_{CC}	50			ns	7
$\overline{RST}$ Low from Clock Input High	t_{HLT}	50			ns	7
CLK Rise Time	t_{CR}			50	ns	7
$\overline{RST}$ Inactive	t_{RLT}	200			ns	7

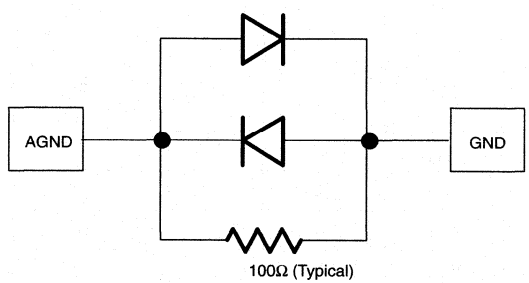
NOTES:

1. All voltages are referenced to ground.
2. Valid for V_{CC}=5V only.
3. Capacitance values apply at 25°C.
4. Inter–Channel Matching is used to determine the relative voltage difference in dB between the same tap position on each potentiometer. The DS1801 is specified for ±0.5 dB inter–channel matching.
5. Tap–to–Tap tolerance is used to determine the change in voltage between successive tap positions. The DS1801 is specified for ±0.25 dB tap–to–tap tolerance.
6. Typical values are for t_A=25°C and nominal supply voltage.
7. See Figure 3.
8. Absolute tolerance is used to determine measured wiper voltage vs. expected wiper voltage as determined by wiper position. The DS1801 is bounded by a ±1 dB absolute tolerance.
9. Maximum current specifications are based on clock rate and active zero–crossing detection. See Figure 5 for clock rate vs. current specification.
10. See Figure 7.
11. Standby current levels apply when all inputs are driven to appropriate supply levels.
12. These parameters are characterized and not 100% tested.

DIGITAL OUTPUT LOAD Figure 6



INTERNAL GROUND CONNECTIONS Figure 7



NOTE: GND and AGND must be tied to the same voltage level.

PRODUCT PREVIEW

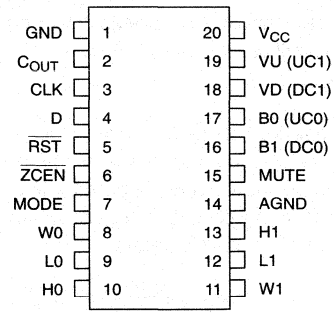
DALLAS SEMICONDUCTOR

DS1802
Dual Audio Taper Potentiometer with Pushbutton Control

FEATURES

- Ultra–low power consumption
- Operates from 3V or 5V supplies
- Two digitally controlled, 65–position potentiometers including mute
- Logarithmic resistive characteristics (1 dB per step)
- Zero–crossing detection eliminates noise caused by wiper movement
- Digital or mechanical push–button wiper control
- Serial port provides means for setting and reading both potentiometer wipers
- 20–pin SOIC and 20–pin TSSOP for surface mount applications
- Temperature:
  - Commercial: 0°C to 70°C
- Software and hardware mute

PIN ASSIGNMENT



20–PIN DIP (300 MIL)
20–PIN SOIC (300 MIL)
20–PIN TSSOP (173 MIL)
See Mech. Drawings Section

PIN DESCRIPTION

L0, L1	–	Low End of Resistor
H0, H1	–	High End or Resistor
W1, W2	–	Wiper End of Resistor
V_{CC}	–	3V/5V Power Supply Input
$\overline{RST}$	–	Serial Port Reset Input
D	–	Serial Port Data Input
CLK	–	Serial Port Clock Input
MODE	–	Mode Select Input
UC0, UC1	–	Up Control Pushbutton Inputs
DC0, DC1	–	Down Control Pushbutton Inputs
VU, VD	–	Volume Up/Volume Down Inputs
B0, B1	–	Balance Pot–0, Pot–1 Inputs
GND	–	Digital Ground
MUTE	–	Mute
AGND	–	Analog Ground
$\overline{ZCEN}$	–	Zero Crossing Detect
C_{OUT}	–	Cascade Output

DESCRIPTION

The DS1802 is a dual audio taper–potentiometer having logarithmic resistive characteristics over the device range. Each potentiometer provides 65 wiper positions with a 1 dB increment per step and device mute. The DS1802 has two methods of device control which include contact closure (push–button) inputs and a 3–wire serial interface for wiper positioning. The push–button control inputs provide a simple interface for device control without the need for a CPU. While the 3–wire serial interface, using a CPU, provides the user the ability of reading or writing exact wiper positions of the two potentiometers. The DS1802 can also be configured to operate in either independent or "stereo" modes, when using pushbutton control. Independent mode of operation allows for independent wiper control and stereo mode of operation provides single input control over both potentiometer wiper positions. The DS1802 is offered in commercial temperature versions. Packages for the part include a 20–pin DIP, 20–pin SOIC, and 20–pin TSSOP.

OPERATION

The DS1802 provides two 65–position potentiometers per package; each having a logarithmic resistive characteristic as shown in Table 1. The DS1802 can be controlled either digitally, or mechanically using a 3–wire serial interface or contact closure input, respectively. The push–button interface allows for a simple mechanical control method for incrementing or decrementing wiper position. The 3–wire serial interface is designed for CPU controlled applications and allows the potentiometer's exact wiper position to be read or written. Additionally, the DS1802 can be daisy chained for multi–device environments.

Figure 1 presents a block diagram of the DS1802. As shown, the inputs from the 3–wire serial interface and contact closure inputs drive a command/control unit. The command/control unit interprets these inputs for control of the two potentiometers.

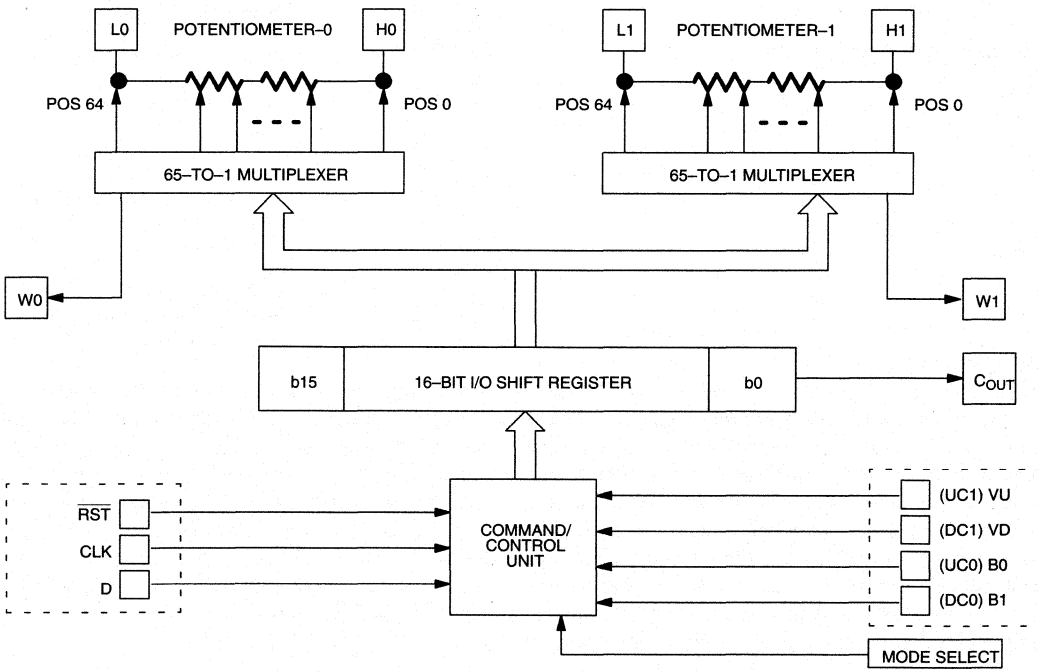
The MODE input is used for contact closure operation. This input allows the user to choose between independent mode control and stereo mode control. The MODE input is discussed in detail under the contact closure interface control.

On power–up the serial port is stable and active within 10 microseconds. The contact closure control interface inputs are active after 50 ms. The wiper position on power–up will be at position 63, the low end of the potentiometer. Position 64 is the mute level.

RESISTANCE CHARACTERISTICS Table 1

POSITION	OUTPUT LEVEL (dB)
0	0
1	–1
2	–2
3	–3
4	–4
5	–5
•	•
•	•
•	•
63	–63
64 (Mute)	< –90

DS1802 BLOCK DIAGRAM Figure 1



CONTACT CLOSURE INTERFACE CONTROL

The DS1802 can be configured to operate from contact closure inputs sometimes referred to as push–button control. There exist a total of four physical contact closure terminals on the device package. When combined with the MODE input, these contact closure inputs provide a total of eight different contact closure functions. These eight contact closure functions are listed in Table 2.

CONTACT CLOSURE INPUTS Table 2

CONTACT INPUT	DESCRIPTION
UC0*	Up contact potentiometer–0
UC1*	Up contact potentiometer–1
DC0*	Down contact potentiometer–0
DC1*	Down contact potentiometer–1
VU**	Volume up
VD**	Volume down
B0**	Balance Pot–0
B1**	Balance Pot–1

* independent mode control
** stereo mode control

The MODE input terminal is used to select the mode of wiper control using contact closure. There exist two modes of wiper control which include independent mode control and stereo mode control. As shown in the pin assignment diagram, the contact closure inputs share pins. Input functionality is determined by the state of the MODE input at power–up.

Independent mode control allows the user to independently control each potentiometers wiper position. For independent mode control, the MODE input should be in a high state. For stereo mode control, the MODE input should be in a low state. The input should always be tied to a well defined logic state.

The contact closure inputs which affect independent mode control include UC0, UC1, DC0, and DC1. As outlined in Table 2, the UC0 and UC1 inputs are used to move the potentiometers wipers towards the high–end of the potentiometer (H0, H1) terminals. And the DC0 and DC1 inputs control movement towards the low–end terminals (L0, L1). Note that UC0 and DC0 control potentiometer–0 wiper movement while UC1 and DC1 control potentiometer–1 movement.

An additional feature of the contact closure interface is the ability to control both directions of wiper movement with only the UC0 and UC1 contact closure inputs. This feature is referred to as single pushbutton operation. Figure 2(a) and (b) illustrates both configurations for single pushbutton and dual pushbutton operation.

Stereo Mode Control

Stereo mode control allows for the simultaneous positioning of both potentiometer wipers from a single control input. Stereo mode control is entered when the MODE select input is in a low state at power–up. The functionality available when operating in stereo mode control includes: 1) volume–up, 2) volume–down, 3) balance–0, and 4) balance–1.

4

Volume Control Inputs

Volume–up and volume–down allow the user to move both wipers either up or down the resistor array without changing the relative balance or distance between the wipers. For example, if potentiometer–0's wiper is set at position 28 and potentiometer–1's wiper is set at position 20, the position distance of eight is maintained when using either of these functions. Additionally, the balance between both wipers is preserved if either reaches the end of its resistor array.

Balance Control Inputs

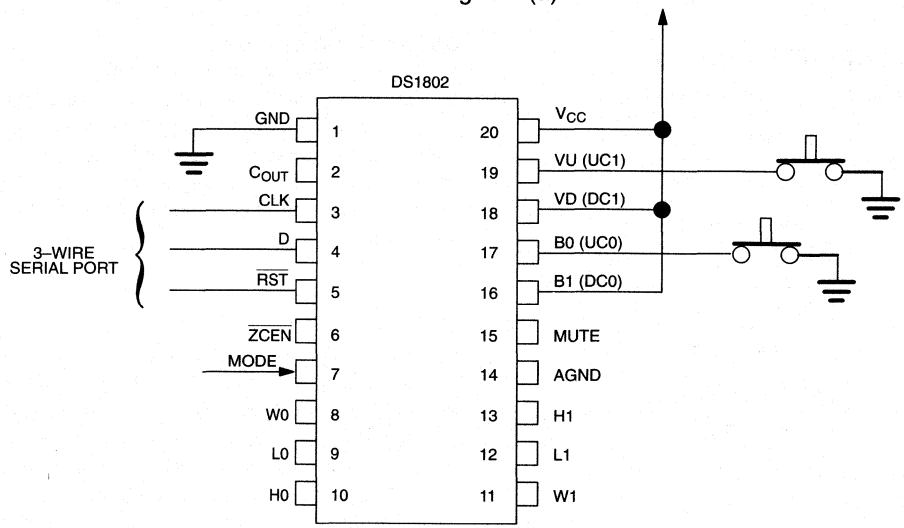
Balance control inputs allow the user to control the distance or offset between potentiometer–0 and potentiometer–1 wiper position settings. The two input controls for balance include B0 and B1. The balance control inputs attempt to minimize their respective wiper's attenuation. When the DS1802 first receives a balance control input, the position of the wiper closest to the high end terminal, H_X, is stored. Wiper position movement is then governed by this stored value.

For example, if the B0 input is used, the attenuation of potentiometer–0 will change only if it is greater than the attenuation of potentiometer–1. The direction of movement for the potentiometer–0 wiper will be towards the high end of the resistor array. Movement of wiper–0 will only stop once its value is equal to that of wiper–1. At this point, continued input activity on the B0 input will cause an increase in attenuation of potentiometer–1. Note that if the wiper of potentiometer–1 peaks at the bottom of its

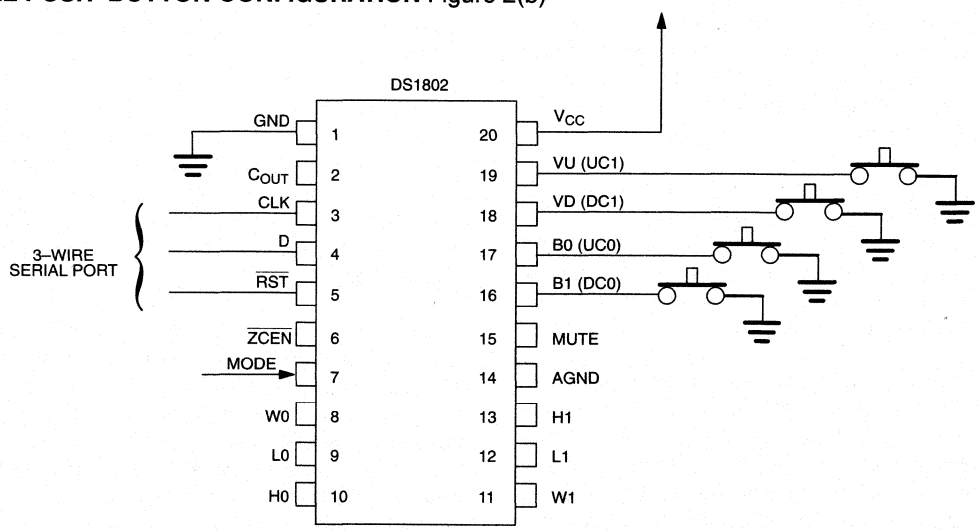
array, continued B0 input activity will cause no change in the wiper positions of the device. A B1 input will be required to change the balance of the two wipers if the potentiometer wiper peaks in this case.

In the case where both wiper positions are at position 63, no movement of the wipers will take place when using the balance controlled inputs. A volume–up control input is required to move the wiper positions from the bottom of the resistor arrays. Balance control operation is presented in Figure 3.

SINGLE PUSH–BUTTON CONFIGURATION Figure 2(a)



DUAL PUSH–BUTTON CONFIGURATION Figure 2(b)



Contact closure is defined as the transition from a high level to a low level on the contact closure input terminals. The DS1802 interprets input pulse widths as the means of controlling wiper movement. A single pulse input over the UCx or DCx input terminals will cause the wiper to move one position. A transition from high to low on these inputs is considered the beginning of pulse activity or contact closure. A single pulse is defined as being greater than 1 ms but lasting no longer than a second. This is shown is Figure 4(a).

Repetitive pulsed inputs can be used to step through each resistive position of the device in a relatively fast manner (see Figure 4(b)). The requirement for repetitive pulsed inputs is that pulses must be separated by a minimum time of 1 ms. If not, the DS1802 will interpret repetitive pulses as a single pulse.

Pulse inputs lasting longer than 1 second will cause the wiper to move one position every 100 ms following the initial 1 second hold time. The total time to transcend the entire potentiometer using a continuous input pulse is given by the formula below:

1 (second) + 63 X 100 ms =7.3 (seconds)

Single Contact Closure

Single contact closure operation allows the user to control wiper movement in either direction from a single push–button input. Figure 2(a), as mentioned, presents a typical single push–button configuration.

In independent mode control, the UC0 and UC1 inputs are used to increment and decrement each respective wiper position for single push–button mode of operation. The DC0 and DC1 inputs provide no functionality in the single push–button configuration but must be connected to the positive supply voltage (V_{CC}). In stereo mode control, the VU and B0 inputs are used to control volume and balance. The VD and B1 inputs provide no functionality in the single push–button configuration but must be connected to the positive supply voltage (V_{CC}). The 3–wire serial port inputs ($\overline{RST}$, CLK, and D) must be grounded when not used.

On device power–up, the configuration shown in Figure 2(a) must exist in order to enter the single contact closure mode of operation; especially and specifically, the (DC0, DC1, VD, and B1) input's connection to the positive supply voltage (V_{CC}).

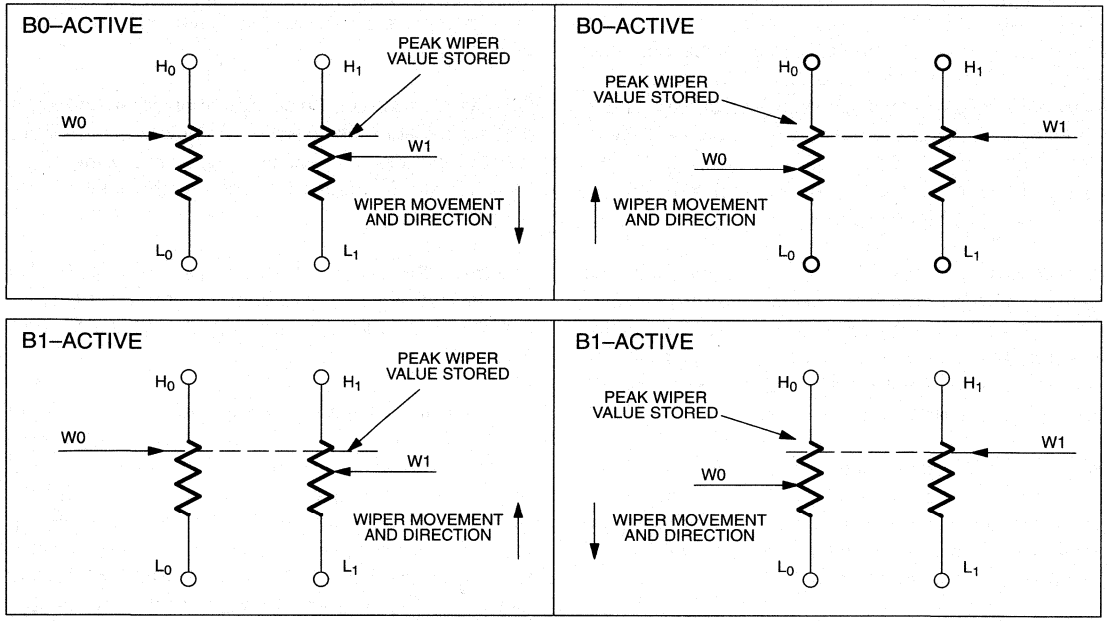
The direction of wiper movement, in single push–button operation, is determined by prior activity; with the direction of wiper movement being opposite to that of the previous activity.

Changing the direction of wiper movement in single push–button configuration is accomplish by a period of inactivity on the controlling input of a (minimum) 1 second or greater. For example, when operating from independent mode control, an inactivity of 1 second or greater on the UC0 input will cause the direction of the potentiometer–0 wiper to reverse. The same is true for the UC1 input. Also, in independent mode control and single push–button configuration, as the wiper reaches the end of the potentiometer range its direction of movement reverses. This will occur regardless if the input is a continuous pulse, a sequence of repetitive pulses or a single pulse.

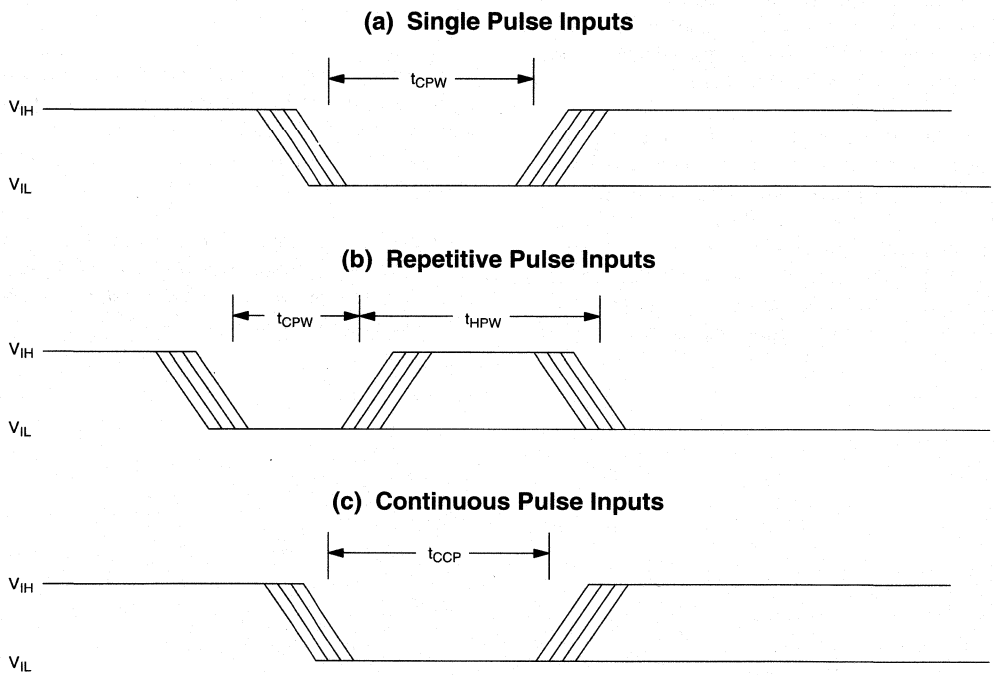
In stereo mode control, the VU input is responsible for both directions of wiper movement. Again, a period of inactivity will allow the direction of volume to be reversed. Additionally, if either wiper reaches a peak position, the direction of movement will automatically reverse.

For balance mode control, the B0 input will be responsible for wiper movement. A period of inactivity lasting 1 second or more will cause a switch in balance movement (i.e. balance–0 to balance–1).

DS1802 BALANCING EXAMPLE Figure 3



CONTACT CLOSURE TIMING (UC, DC) Figure 4



Dual Contact Closure

In dual push–button mode, each direction is controlled by the respective control inputs. No wait states are required to change wiper direction, balance, or volume in dual push–button mode. Additionally, in dual push–button mode as the wiper position reaches the end of the potentiometer, the direction of wiper movement will not change. Wiper position will remain at the potentiometers' end until an opposite direction input is given.

All contact closure control inputs, UC0, UC1, DC0, DC1, VU, VD, B0 and B1 are internally pulled–up by a 50KΩ resistance. The UC0, UC1, DC0 DC1, VU, VD, B0, and B1 inputs are internally debounced and require no external components for input signal conditioning.

3–WIRE SERIAL INTERFACE CONTROL

One method of communication and control of the DS1802 is accomplished through a 3–wire serial port interface that drives an internal control logic unit. The 3–wire serial interface is designed for microprocessor or microcontroller applications. The interface consists of three input signals which include $\overline{RST}$, CLK and D.

The $\overline{RST}$ control signal is used to enable 3–wire serial port write operations. The CLK terminal is a clock signal input that provides synchronization for data I/O while the D signal input serves to transfer potentiometer wiper position settings to the device.

As shown in Figure 5, a 3–wire serial port operation begins with a transition of the $\overline{RST}$ signal input to a high state. Once the 3–wire port has been activated, data is clocked into the part on the low to high transition of the CLK signal input. Data input via the D line is transferred in order of the desired potentiometer–0 value followed by the potentiometer–1 value.

The DS1802 contains two 65–position potentiometers whose wiper positions are set by an 8–bit value. These two 8–bit values are written to the 16–bit I/O shift register which is used to store wiper position during powered conditions. Because the potentiometer has 65–positions, only seven bits of data are needed to set wiper position. A detailed diagram of the 16–bit I/O shift register is shown in Figure 5. Bits 0 through 7 are reserved for the potentiometer–0 control while bits 8 through 15 are reserved for control of potentiometer–1.

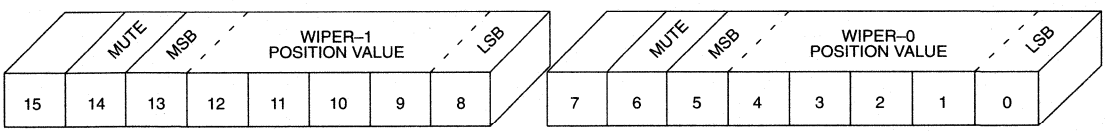
Bits 0 through 5 are used for actual wiper positioning for potentiometer–0. Bit 6 is used to mute potentiometer–0. If this bit has value "1", the potentiometer–0 wiper will be connected to the low end of the resistive array. The mute feature of the DS1802 will be discussed in the section entitled "Mute Operation of DS1802". The value of bit 7 is a don't care and will not affect operation of the DS1802 or potentiometer–0.

Bits 8 through 13 are used for wiper positioning of potentiometer–1. Bit 14 is used for muting of the potentiometer–1 wiper output. Bit 15, like bit 7, is a don't care and will not affect operation of the DS1802.

Data for the DS1802 is transmitted LSB first starting with bit 0. A complete transmission of 16 bits of data is required to insure proper setting of each potentiometer's wiper. An incomplete transmission may result in undesired wiper settings.

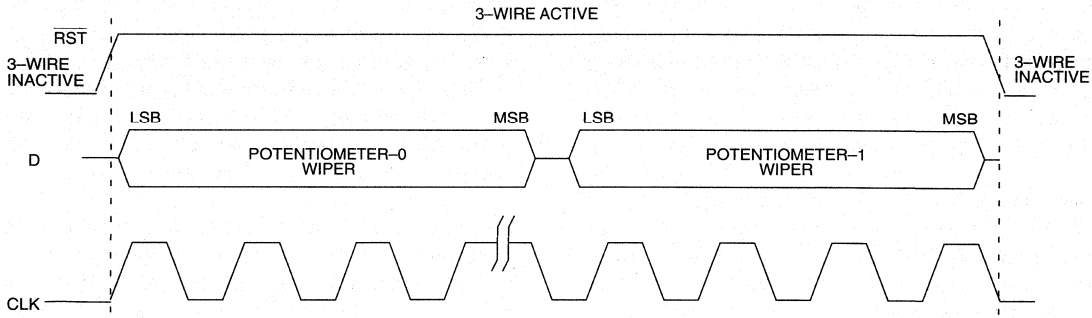
Once the complete 16 bits of information has been transmitted and the $\overline{RST}$ signal input transitions to a low state, the new wiper positions are loaded into the part.

16–BIT I/O SHIFT REGISTER Figure 5

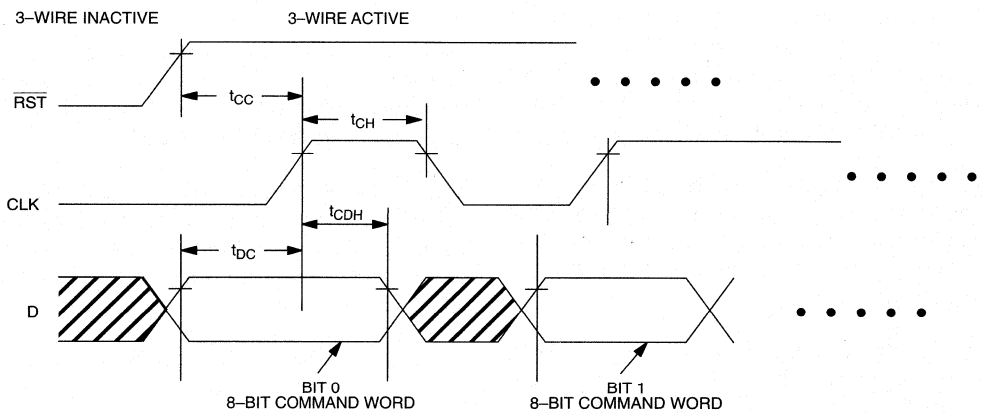


TIMING DIAGRAMS Figure 6

(a) 3–Wire Serial Interface General Overview

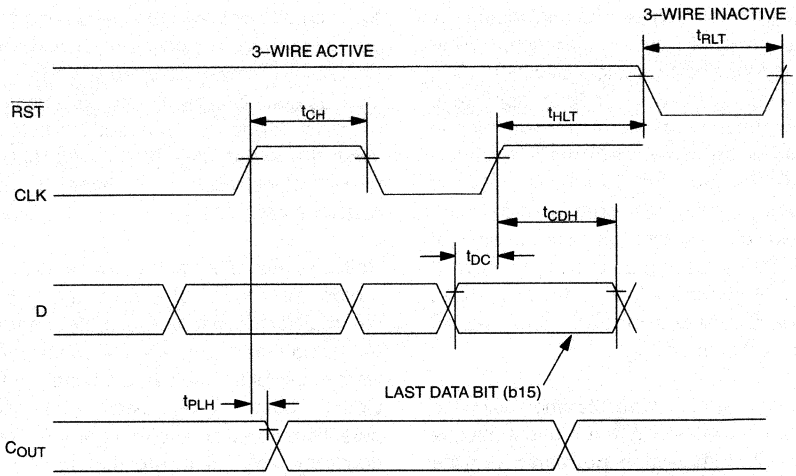


(b) Start of Communication Transaction



TIMING DIAGRAMS Figure 3 (cont'd)

(c) End of Communication Transaction



CASCADE OPERATION

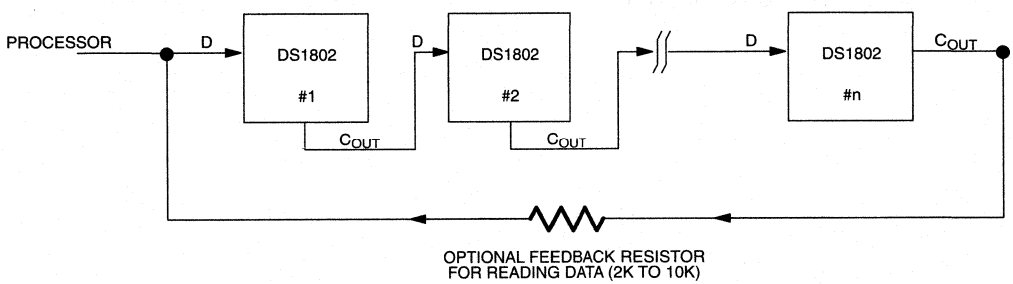
A feature of the DS1802 is the ability to control multiple devices from a single processor. Multiple DS1802's can be linked or daisy chained as shown in Figure 7. As a data bit is entered into the I/O shift register of the DS1802 it will appear at the C_{OUT} output after a maximum delay of 50 nanoseconds.

The C_{OUT} output of the DS1802 can be used to drive the D input of another DS1802. When connecting multiple devices, the total number of bits sent is always 16 times the number of DS1802s in the daisy chain.

An optional feedback resistor can be placed between the C_{OUT} terminal of the last device and the D input of the first DS1802, thus allowing the controlling processor to circularly clock data through the daisy chain. The value of the feedback or isolation resistor should be in the range from 2K to 10K ohms.

When reading data via the C_{OUT} pin and isolation resistor, the D line is left floating by the reading device. When $\overline{RST}$ is driven high, bit 0 is present on the C_{OUT} pin, which is fed back to the input D pin through the isolation resistor. When the CLK input transitions low to high, bit 0 is loaded into the first position of the I/O shift register and bit 1 becomes present on C_{OUT} and D of the next device. After 16 bits (or 16 times the number of DS1802's in the daisy chain), the data has shifted completely around and back to its original position. When $\overline{RST}$ transitions to the low state to end data transfer, the value (the same as before the read occurred) is loaded into the wiper–0 and wiper–1.

CASCADING MULTIPLE DEVICES Figure 7



Zero Crossing Detection

The DS1802 provides a zero–crossing detection capability when using the 3–Wire Serial interface. Zero–crossing detection provides a means for minimizing any audible noise that may result from sizable discrete wiper transitions when using the part in audio applications. The zero crossing detect feature allows independent wiper changes only when the two terminals of the potentiometer have equal potentials and within a 50 ms time window from the fall of the $\overline{RST}$ signal. If at 50 ms the DS1802 has not detected a zero crossing, the wiper position of the potentiometer(s) will change regardless of the state of the input signal. Zero–crossing detection is activated when the $\overline{ZCEN}$ input level is in a low–state. When high, the $\overline{ZCEN}$ input deactivates both the 50 ms time requirement and zero–detection crossing.

Zero crossing detection is also available when using the part in push–button operation. When a pushbutton is activated, the part will change wiper position during the first detected zero–crossing or at the end of a 50 ms time window.

When operating in push–button operation with a continuous input pulse, the wiper position will change once during the initial 1 second time period. This change is dictated by a detected zero–crossing or 50 ms time window. Subsequent changes when operating with continuous input pulse occur on 100 ms time intervals and are dependent on zero crossing or 50 ms timeouts.

MUTE CONTROL

The DS1802 provides a mute control feature which can be accessed by the user through hardware or software. Hardware control of the device is achieved through the MUTE input pin. This pin is internally pulled–up through a 50KΩ resistor. When this input is driven low, the wiper outputs of both potentiometers will be internally connected to the low terminal of their respective potentiometers. This input performs as a toggle input, with the first activity on this pin connecting the wiper outputs to the low end of the resistive array on each potentiometer. The next input activity on this pin will return the wiper position to the previous state before the muting occurred. Also, if operating in pushbutton mode, mute will be deactivated if an input is received over the VU, VD, UC0, UC1, DC0, DC1 inputs. This input, like the pushbutton inputs, is internally debounced and requires no external circuitry. When the device powers up, the first activity on the mute pin will internally connect the wipers to the low end of the resistor array.

Software mute control was briefly discussed in 3–wire protocol and operation. Bits 6 and 14 of the 16–bit I/O shift register are reserved for mute control of potentiometer–0 and potentiometer–1, respectively. Unlike hardware mute control, software muting allows the user individual control of each potentiometer (i.e., potentiometer–0 and potentiometer–1 can be independently muted). Software muting of potentiometer–0 would require bit 6 to have a value of 1 while for potentiometer–1, bit 14 should have a value 1. When the user desires to release the mute of any potentiometer through software the complete 16–bit I/O shift register must be rewritten with the desired potentiometer wiper settings and bits 6 and 14 having zero value.

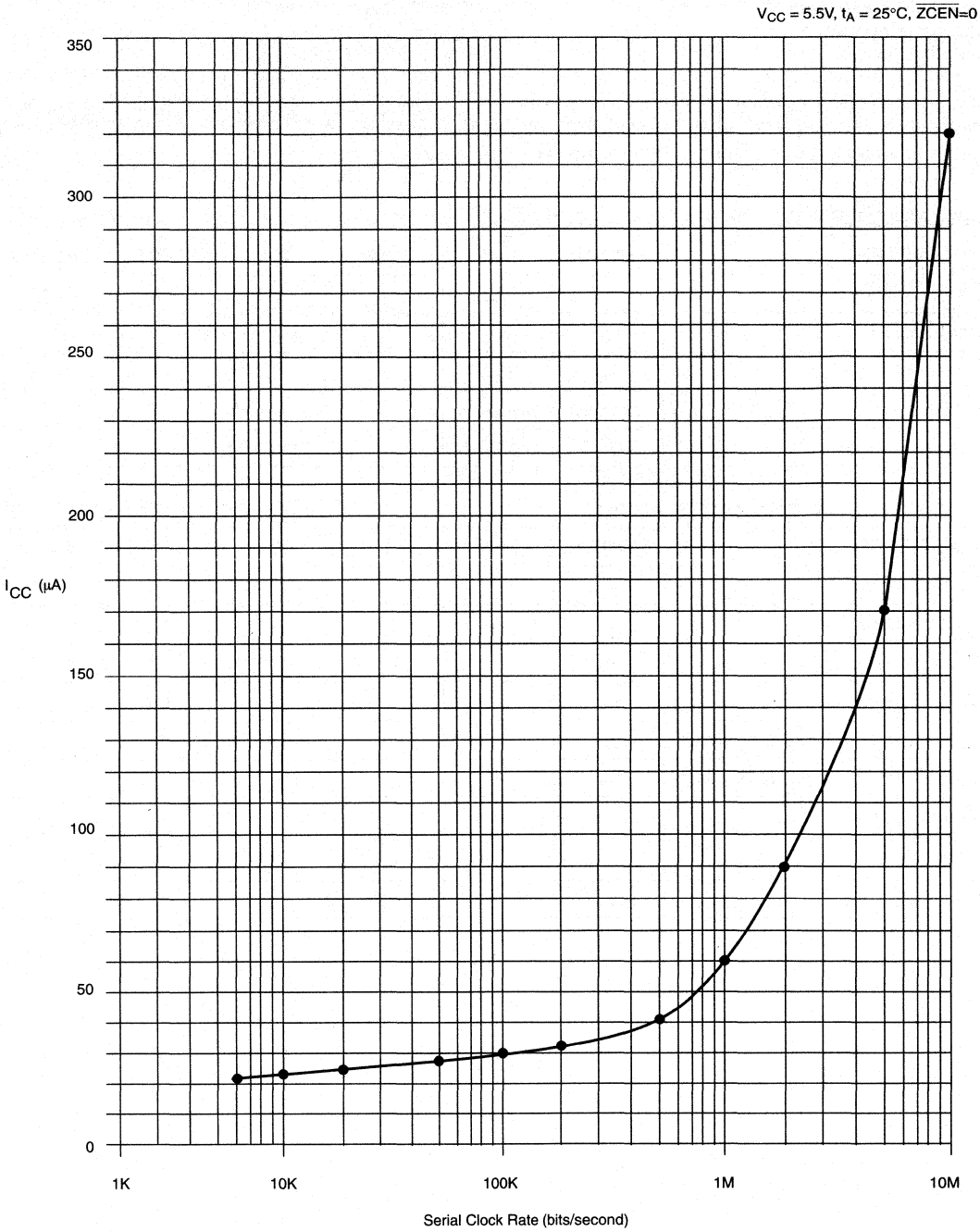
3–Wire Serial Port Vs Pushbutton Operation

In applications where both the 3–Wire Serial port and the pushbutton inputs will be used to control the part, there may exist times when activity is present on both control interfaces simultaneously. This section describes how the DS1802 handles these situations.

In all instances, the DS1802 3–Wire serial port takes precedence over pushbutton input control.

The DS1802 will not allow pushbutton inputs to change wiper position during 3–Wire serial port activity.

TYPICAL SUPPLY CURRENT VS. SERIAL CLOCK RATE Figure 8



4

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground and AGND	–0.7V to +7.0V
Operating Temperature	0°C to 70°C commercial
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	+2.7		5.5	V	1
Input Logic 1	V_{IH}	2.0		V_{CC}+0.5	V	1, 2
Input Logic 0	V_{IL}	–0.5		+0.8	V	1, 2
Resistor Inputs	L, H, W	GND–0.5		V_{CC}+0.5	V	1
Analog Ground	AGND	GND–0.5		GND +0.5	V	14

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=3V and 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}			2000	µA	12
Input Leakage	I_{LI}	–1		+1	µA	3
Wiper Resistance	R_W		400	1000	Ω	
Wiper Current	I_W			1	mA	
Logic 1 Output Current @ 2.4 Volts	I_{OH}	–1.0			mA	2
Logic 0 Output Current @ 0.4 Volts	I_{OL}			4	mA	2
Standby Current 3 Volts 5 Volts			 22 42	 80	 µA µA	15
Power–Up Time	t_{PU}		50		ms	9

ANALOG RESISTOR CHARACTERISTICS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Total Resistance			45		KΩ	
Absolute Tolerance		–1		+1	dB	11
Inter–Channel Matching		–0.5		+0.5	dB	6
Tap–to–Tap Tolerance		–0.25		+0.25	dB	7, 16
–3 dB Cutoff Frequency	f_{CUTOFF}		700 KHz		KHz	
Temperature Coefficient			±800		ppm/°C	
Total Harmonic Distortion (V_{IN}=1V_{RMS}, 1 KHz, Tap= –6 dB)	THD		0.002		%	16
Output Noise (20 Hz to 20 KHz, Grounded Input, Tap= –6 dB)			2.2		μV_{RMS}	
Digital Feedthrough (20 Hz to 20 KHz, Tap= –6 dB)			–90		dB	16
Interchannel Isolation (20 Hz to 20 KHz, Tap= –6 dB)			–100		dB	16
Mute Control Active	Mute		–90		dB	

CAPACITANCE (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	8
Output Capacitance	C_{OUT}			7	pF	8

AC ELECTRICAL CHARACTERISTICS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CLK Frequency	f_{CLK}	DC		10	MHz	10, 13
Width of CLK Pulse	t_{CH}	50			ns	10, 13
Data Setup Time	t_{DC}	30			ns	10, 13
Data Hold Time	t_{CDH}	10			ns	10, 13
Propagation Delay Time Low to High Level Clock to Output	t_{PLH}			50	ns	10, 13
Propagation Delay Time High to Low Level	t_{PLH}			50	ns	10, 13
$\overline{RST}$ High to Clock Input High	t_{CC}	50			ns	10, 13
$\overline{RST}$ Low from Clock Input High	t_{HLT}	50			ns	10, 13
CLK Rise Time	t_{CR}			50	ns	10, 13
$\overline{RST}$ Inactive	t_{RLT}	200			ns	10, 13

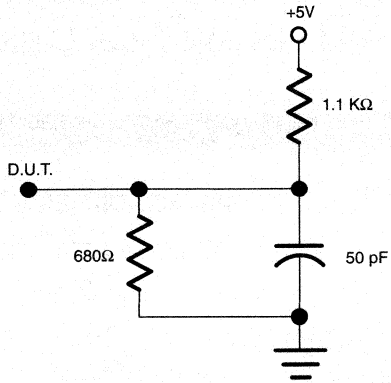
AC ELECTRICAL CHARACTERISTICS (PUSHBUTTON INPUTS) (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Single Pulse Input	t_{CPW}	1		DC	ms	3, 5, 13
Repetitive Input Pulse High Time	t_{HPW}	1		DC	ms	3, 5, 13
Continuous Input Pulse	t_{CCP}	1		DC	s	3, 5, 13

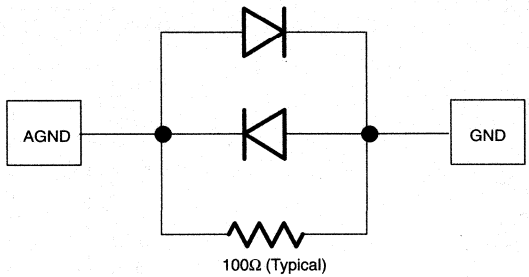
NOTES:

1. All voltages are referenced to ground.
2. Valid for V_{CC}=5V only.
3. Both UCx and DCx inputs are internally pulled up with a 50KΩ resistance.
4. Capacitance values apply at 25°C.
5. Input pulse width is the minimum time required for an input to cause an increment or decrement. If the UCx or DCx inputs is held active for longer than 1 second, subsequent increments or decrements will occur on 100 ms intervals until the inputs UCx, DCx are released to V_{IH}. Timing tolerances for pushbutton control is ±30%.
6. Inter–Channel Matching is used to determine the relative voltage difference in dB between the same tap position on each potentiometer. The DS1802 is specified for ±0.5 dB inter–channel matching.
7. Tap–to–Tap tolerance is used to determine the change in voltage between successive tap positions. The DS1802 is specified for ±0.25 dB tap–to–tap tolerance.
8. Typical values are for t_A=25°C and nominal supply voltage.
9. Power–up time is the time for all pushbutton inputs to be stable and active once power has reached a valid level, 2.7V min.
10. See Figure 6.
11. Absolute tolerance is used to determine measured wiper voltage vs. expected wiper voltage as determined by wiper position. The DS1802 is bounded by a ±1 dB absolute tolerance.
12. Maximum current specifications are based on clock rate, active zero–crossing detection, and push–button activation. See Figure 8 for clock rate vs. current specification.
13. Valid for V_{CC}=3V or 5V.
14. See Figure 10.
15. Standby current levels apply when all inputs are driven to appropriate supply levels.
16. These parameters are characterized and not 100% tested.

DIGITAL OUTPUT LOAD Figure 9



INTERNAL GROUND CONNECTIONS Figure 10



NOTE: GND and AGND must be tied to the same voltage level.

PRODUCT PREVIEW

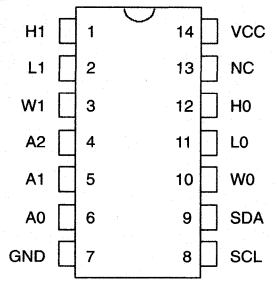
DALLAS SEMICONDUCTOR

DS1803
Addressable Dual Digital Potentiometer

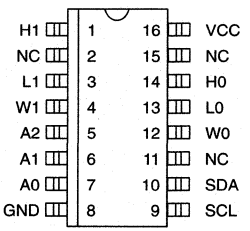
FEATURES

- 3V or 5V Power Supplies
- Ultra–low power consumption
- Two digitally controlled, 256–position potentiometers
- 14–Pin TSSOP (173 mil) and 16–Pin SOIC (150 mil) packaging available for surface mount applications
- Addressable using 3–Chip Select Inputs
- Serial/Synchronous Bus Interface
- Operating Temperature
  - Commercial: 0°C to 70°C
  - Industrial: –40°C to +85°C
- Standard Resistance Values:
  - DS1803–010 10Kohm
  - DS1803–050 50Kohm
  - DS1803–100 100Kohm

PIN ASSIGNMENT



DS1803E 14–PIN TSSOP (173 MIL)



DS1803Z 16–PIN SOIC (150 MIL)
DS1803 16–PIN DIP (300 MIL)
See Mech. Drawings Section

PIN DESCRIPTION

L0,L1	– Low End of Resistor
H0,H1	– High End of Resistor
W0,W1	– Wiper Terminal of Resistor
V_{CC}	– 3V/5V Power Supply Input
A0 ..A2	– Chip Select Inputs
SDA	– Serial Data I/O
SCL	– Serial Clock Input
GND	– Ground
NC	– No connection

DESCRIPTION

The DS1803 is an addressable device having two independently controlled potentiometers. Each potentiometer's wiper can be set to one of 256 positions. Device control is achieved via a two–wire serial interface having a data I/O terminal and a clock input terminal. Device addressing is provided through three chip select input terminals and correct communication protocol. Addressing capability, when operating in a bus topology, allows up to eight devices to be controlled by the serial interface. The exact wiper position of each potentiometer can be written or read. The DS1803 is available in a 16–pin DIP, 16–pin SOIC and 14–pin TSSOP package. The device is available in commercial or industrial grade temperature versions and three standard resistance values: 10Kohm, 50Kohm, and 100Kohm.

DEVICE OPERATION

The DS1803 is an addressable, digitally controlled device which has two 256–position potentiometers. A functional block diagram of the part is shown in Figure 1. Communication and control of the device is accomplished via a 2–Wire serial interface having signals SDA and SDL. Device addressing is attained using the device chip select inputs A0, A1, A2 and correct communication protocol over the 2–wire serial interface.

Each potentiometer is composed of a 256 position resistor array. Two 8–bit registers, each assigned to a respective potentiometer, are used to set wiper position on the resistor array. The wiper terminal is multiplexed to one of 256 positions on the resistor array based on its corresponding 8–bit register value. For example, the high–end terminals, H0 and H1, have wiper position values FF(Hex) while the low–end terminals, L0 and L1, have wiper position values 00(Hex).

The DS1803 is a volatile device that does not maintain the position of the wiper during power–down or loss of power. On power–up, the DS1803 wipers' position will be set to position 00(Hex) — the low–end terminals. The user may then reset the wiper value to a desired position.

Communication with the DS1803 takes place over the 2–Wire serial interface consisting of the bi–directional data terminal, SDA, and the serial clock input, SCL. Complete details of the 2–Wire interface are discussed in the section entitled "2–Wire Serial Bus".

The 2–Wire interface and chip select inputs A0, A1, and A2 allow operation of up to eight devices in a bus topology; with A0, A1, and A2 being the address of the device.

Application Considerations

The DS1803 is offered in three standard resistor values which include the 10Kohm, 50Kohm, and 100Kohm. The resolution of the potentiometer is defined as $R_{TOT}/256$, where R_{TOT} is the total resistor value of the potentiometer. The DS1803 is designed to operate using 3V or 5V power supplies and over the commercial (0°C to 70°C) and industrial (–40°C to +85°C) temperature ranges. Maximum input signal levels across the potentiometer cannot exceed the operating power supply of the device.

2–WIRE SERIAL DATA BUS

The DS1803 supports a bi–directional two–wire bus and data transmission protocol. A device that sends data on the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a "master". The devices that are controlled by the master are "slaves". The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS1803 operates as a slave on the two–wire bus. Connections to the bus are made via the open–drain I/O lines SDA and SCL.

The following bus protocol has been defined (see Figure 2).

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data. Figure 2 details how data transfer is accomplished on the two–wire bus. Depending upon the state of the R/$\overline{W}$* bit, two types of data transfer are possible.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte–wise and each receiver acknowledges with a ninth bit.

Within the bus specifications a regular mode (100KHZ clock rate) and a fast mode (400KHz clock rate) are defined. The DS1803 works in both modes.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case , the slave must leave the data line HIGH to enable the master to generate the STOP condition.

1. Data transfer from a master transmitter to a slave receiver. The first byte transmitted by the master is the control by (or slave address). Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.
2. Data transfer from a slave transmitter to a master receiver. The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit . Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a 'not acknowledge' is returned.

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

The DS1803 may operate in the following two modes:

1. Slave receiver mode: Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.
2. Slave transmitter mode: The first byte is received and handled as in the slave receiver mode. However, in this mode the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1803 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

SLAVE ADDRESS

A control byte is the first byte received following the START condition from the master device. The control byte consist of a four bit control code; for the DS1803, this is set as 0101 binary for read/write operations. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used by the master device to select which of eight devices are to be accessed. The select bits are in effect the three least significant bits of the slave address. Additionally, A2, A1 and A0 can be changed anytime during a powered condition of the part. The last bit of the control byte ($R/\overline{W}$*) defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. Figure 3 shows the control byte structure for the DS1803.

Following the START condition, the DS1803 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving the 0101 address code and appropriate device select bits, the slave device outputs an acknowledge signal on the SDA line.

COMMAND AND PROTOCOL

The command and protocol structure of the DS1803 allows the user to read or write the potentiometer(s). The command structures for the part are presented in Figures 4 and 5. Potentiometer data values and control and command values are always transmitted most significant bit (MSB) first. During communications the receiving unit always generates the acknowledge.

Reading the DS1803

As shown in Figure 4 the DS1803 provides one read command operation. This operation allows the user to read both potentiometers. Specifically, the R/W bit of the control byte is set equal to a 1 for a read operation. Communication to read the DS1803 begins with a START condition which is issued by the master device. The control byte from the master device will follow the START condition. Once the control byte has been received by the DS1803, the part will respond with an ACKNOWLEDGE. The read/write bit of the control byte as stated should be set equal to '1' for reading the DS1803.

When the master has received the ACKNOWLEDGE from the DS1803, the master can then begin to receive potentiometer wiper data. The value of the potentiometer–0 wiper position will be the first returned from the DS1803. Once the eight bits of the potentiometer–0 wiper position has been transmitted, the master will need to issue an ACKNOWLEDGE, unless it is the only byte to be read, in which case the master issues a NOT ACKNOWLEDGE. If desired the master may stop the communication transfer at this point by issuing the STOP condition. However, if the value of the potentiometer–1 wiper position value is needed communication transfer can continue by clocking the remaining eight bits of the potentiometer–1 value, followed by an NOT ACKNOWLEDGE. Final communication transfer is terminated by issuing the STOP command. Again the flow of the read operation is presented in Figure 4.

Writing the DS1803

A data flow diagram for writing the DS1803 is shown in Figure 5. The DS1803 has three write command operations. These include write pot–0, write pot–1, and write pot–0/1. The write pot–0 command allows the user to write the value of potentiometer–0 and as an option the the value of potentiometer–1. The write–1 command allows the user to write the value of potentiometer–1 only. The last write command, write–0/1, allows the user to write both potentiometers to the same value with one command and one data value being issued.

All the write operations begin with a START condition. Following the START condition, the master device will issue the control byte. The read/write bit of the control byte will be set to '0' for writing the DS1803. Once the control byte has been issued and the master receives the acknowledgment from the DS1803, the command byte is transmitted to the DS1803. As mentioned above, there exist three write operations that can be used with the DS1803. The binary value of each write command is shown in Figure 5 and also in the Table 1.

2–WIRE COMMAND WORDS Table 1

COMMAND	COMMAND VALUE
Write Potentiometer–0	101010 01
Write Potentiometer–1	101010 10
Write Both Pots	101011 11

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–1.0V to 7.0V
Operating Temperature	0°C to 70°C; commercial –40°C to +85°C; industrial
Storage Temperature	–55°C to 125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(–40°C to+85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	+2.7		5.5	V	1
Resistor Inputs	L, H, W	GND–0.5		V_{CC}+0.5	V	1
GND	GND	GND		GND		

DC ELECTRICAL CONDITIONS

(–40°C to+85°C; V_{CC}=2.7V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Current Active	I_{CC}				100	µA	
Input Leakage	I_{LI}		–1		+1	µA	
Wiper Resistance	R_W			400	1000	Ω	
Wiper Current	I_W				1	mA	
Input Logic 1	V_{IH}		0.7V_{CC}		V_{CC}+0.5	V	1, 2
Input Logic 0	V_{IL}		GND–0.5		0.3V_{CC}	V	1, 2
Input Logic Levels A0, A1, A2		Input Logic 1 Input Logic 0	0.7V_{CC} GND–0.5		V_{CC}+0.5 0.3V_{CC}	V	14
Input Current each I/O Pin		0.4<$V_{I/O}$<0.9 V_{DD}	–10		10	µA	
Standby Current	I_{STBY}			20		µA	4
Low Level Output Voltage	V_{OL1}	3 mA sink current	0.0		0.4	V	
	V_{OL2}	6 mA sink current	0.0		0.6	V	
I/O Capacitance	$C_{I/O}$				10	pF	
Pulse Width of Spikes which must be suppressed by the input filter	t_{SP}	Fast Mode	0		50	ns	

ANALOG RESISTOR CHARACTERISTICS

(–40°C to+85°C; V_{CC}=2.7V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
End–to–End Resistor Tolerance		–20		+20	%	
Absolute Linearity			±0.75		LSB	15
Relative Linearity			±0.3		LSB	16
–3 dB Cutoff Frequency	f_{cutoff}				Hz	13
Temperature Coefficient			650		ppm/C	
Capacitance	C_I			5	pF	

AC ELECTRICAL CHARACTERISTICS

(–40°C to+85°C; V_{CC}=2.7V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
SCL Clock Frequency	f_{SCI}	0 0		400 100	KHz	17 18
Bus Free Time Between STOP and START Condition	t_{BUF}	1.3 4.7			µs	17 18
Hold Time (Repeated) START Condition	$t_{HD:STA}$	0.6 4.0			µs	5
Low Period of SCL Clock	t_{LOW}	1.3 4.7			µs	
High Period of SCL Clock	t_{HIGH}	0.6 4.0			µs	
Data Hold Time	$t_{HD:DAT}$	0 0		0.9	µs	6, 7
Data Setup Time	$t_{SU:DAT}$	100 250			ns	8
Rise Time of both SDA and SCL Signals	t_R	$20+0.1C_R$		300 1000	ns	9
Fall Time of both SDA and SCL Signals	t_F	$20+0.1C_R$		300 300	ns	9
Setup Time for STOP Condition	$t_{SU:STO}$	0.6 4.0			µs	
Capacitive Load for each Bus Line	C_R			400	pF	

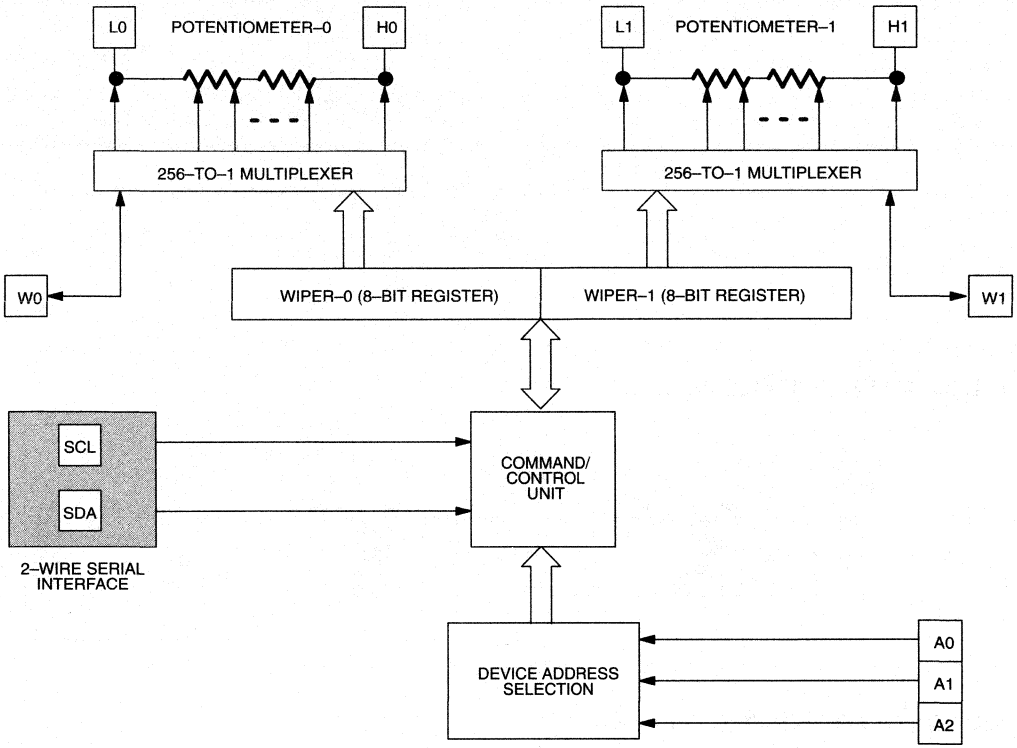
4

NOTES:

1. All voltages are referenced to ground.
2. I/O pins of fast mode devices must not obstruct the SDA and SCL lines if V_{DD} is switched off.
3. I_{CC} specified with SDA pin open.
4. I_{CC} specified with V_{CC} at 5.0V and SDA, SCL = 5.0V, 0°C to +70°C
5. After this period, the first clock pulse is generated.

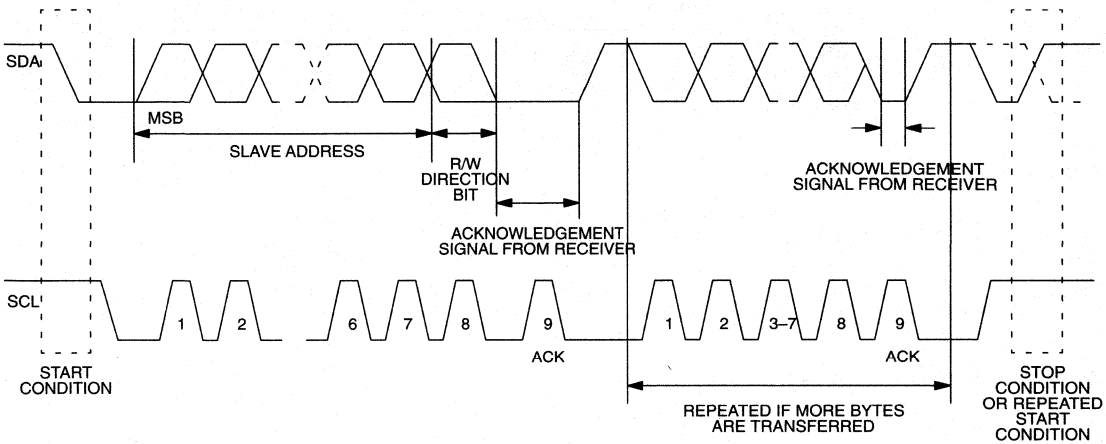
6. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
7. The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
8. A fast mode device can be used in a standard mode system, but the requirement $t_{SU:DAT} > 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{RMAX} + t_{SU:DAT} = 1000 + 250 = 1250$ ns before the SCL line is released.
9. CB – total capacitance of one bus line in picofarads, timing referenced to $(0.9(V_{CC})$ and $(0.1)(V_{CC})$
10. Absolute linearity is used to determine wiper voltage versus expected voltage as determined by wiper position.
11. Relative linearity is used to determined the change in voltage between successive tap positions.
12. Typical values are for $t_A = 25°C$ and nominal supply voltage.
13. –3 dB cutoff frequency characteristics for the DS1803 depend on potentiometer total resistance: DS1803–010; 1 MHz, DS1803–50; 200 KHz, DS1803–100; 100 KHz
14. Address Inputs, A0, A1, and A2, should be tied to either V_{CC} or GND depending on the desired address selections.
15. Absolute linearity is used to determine wiper voltage versus expected voltage as determined by wiper position. Device test limits are ±1.6 LSB.
16. Relative linearity is used to determine the change in voltage between successive tap positions. Device test limits ±0.5 LSB.
17. Fast mode.
18. Standard mode.

DS1803 BLOCK DIAGRAM Figure 1

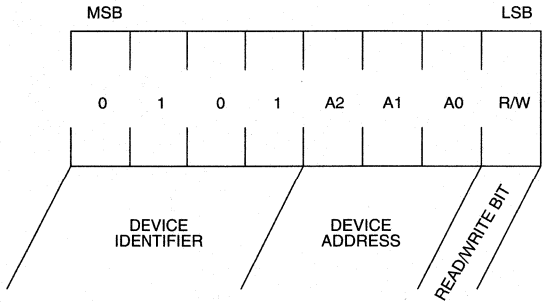


4

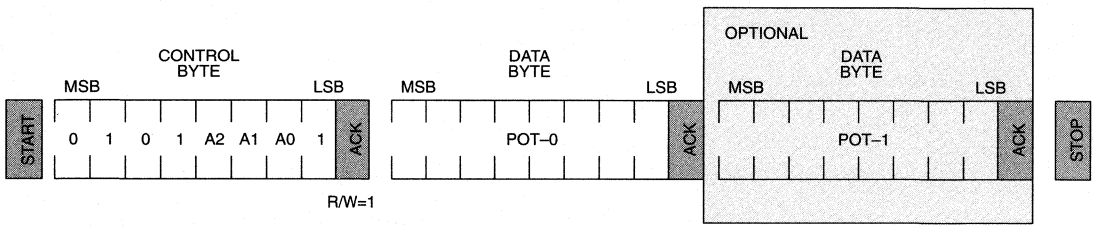
2–WIRE DATA TRANSFER OVERVIEW Figure 2



CONTROL BYTE Figure 3

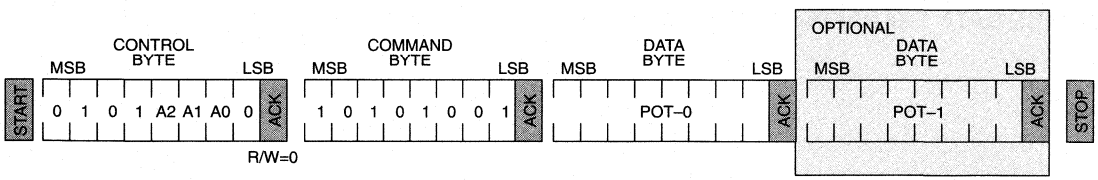


2–WIRE READ PROTOCOLS Figure 4

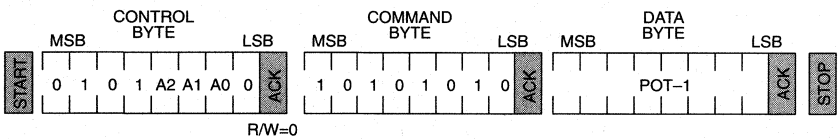


2–WIRE WRITE PROTOCOLS Figure 5

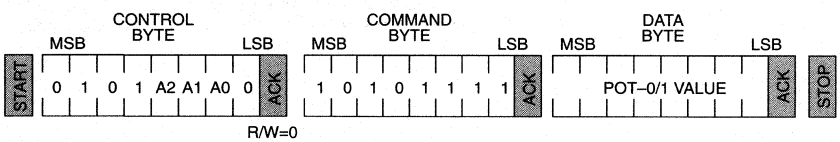
Write Pot–0



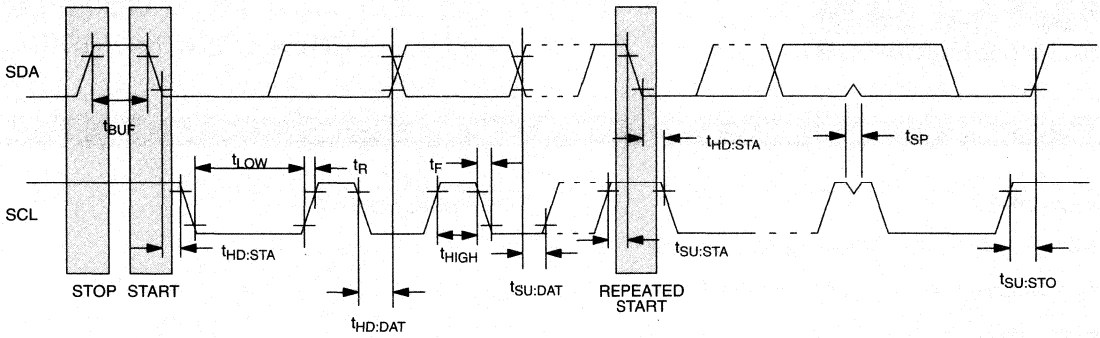
Write Pot–1



Write Pot–0/1 (same value)



TIMING DIAGRAM Figure 6



PRODUCT PREVIEW

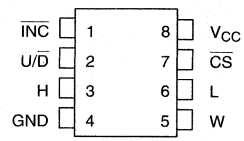
DALLAS SEMICONDUCTOR

DS1804
NV Trimmer Potentiometer

FEATURES

- Single 100–Position Linear Taper Potentiometer
- Nonvolatile "On–Demand" Wiper Storage
- Operates from 3V or 5V supplies
- Up/Down, Increment Controlled Interface
- Resistance Values: 10KΩ, 50KΩ, and 100KΩ
- Available in 8–Pin (300 Mil) DIP, 8–Pin (150 Mil) SOIC packages
- Operating Temperature:
  - Commercial: 0°C to 70°C
  - Industrial: –40°C to 85°C

PIN ASSIGNMENT



8–PIN DIP (300 MIL)
8–PIN SOIC (150 MIL)

See Mech. Drawings Section

PIN DESCRIPTION

H	–	High–End of Resistor
L	–	Low–End of Resistor
W	–	Wiper Terminal
V_{CC}	–	3V or 5V Power Supply Input
$\overline{CS}$	–	Chip Select
$U/\overline{D}$	–	Up/Down Control Input
$\overline{INC}$	–	Increment/Decrement Counter Input
GND	–	Ground

DESCRIPTION

The DS1804 is a nonvolatile digital potentiometer having 100 positions. The device provides an ideal method for low–cost trimming applications using a CPU or manual control input with minimal external circuitry. Wiper position of the DS1804 can be stored in EEPROM memory on demand. The device's wiper position is manipulated by a 3–terminal port that provides an increment/decrement counter controlled interface. This port consist of the control inputs $\overline{CS}$, $\overline{INC}$, and $U/\overline{D}$.

The DS1804 is available in three resistor grades which include a 10KΩ, 50KΩ, and 100KΩ. Commercial and industrial versions of the device are available. Additionally, the DS1804 will operate from 3V or 5V supplies and is ideal for portable application requirements. Two packaging options are available and include the 8–pin (300 mil) DIP and 8–Pin (150 mil) SOIC.

OPERATION

The DS1804 is a single nonvolatile potentiometer. The device has a total of 100 tap–points including the L– and H– terminals. A total of 99 resistive segments exist between the L– and H– terminals. These tap–points are accessible to the W–terminal whose position is controlled via a 3–terminal control port. A block diagram of the DS1804 is shown in Figure 1.

The 3–terminal port of the DS1804 provides an increment/decrement interface which is activated via a chip select input. This interface consists of the input signals $\overline{CS}$, $\overline{INC}$, and U/$\overline{D}$. These input signals control a 7–bit up/down counter. The output of the 7–bit up/down counter controls a 1 of 100 decoder to select wiper position. Additionally, this interface provides for a wiper storage operation using the $\overline{CS}$ and $\overline{INC}$ input control pins. The timing diagram for the 3–terminal interface control is shown in Figure 2.

PIN DESCRIPTIONS

V_{CC} – Power Supply Terminal. The DS1804 will support supply voltages ranging from +2.7 to +5.5 volts.

GND – Ground Terminal.

H – High–end of Resistor. This is the high–end terminal of the potentiometer. It is not required that this terminal be connected to a potential greater than the L–terminal. Voltage applied to the H–terminal can not exceed the power–supply voltage, V_{CC}, or go below ground.

L – Low–end of Resistor –This is the low–end terminal of the potentiometer. It is not required that this terminal be connected to a potential less than the H–terminal. Voltage applied to the L–terminal cannot exceed the power–supply voltage, V_{CC}, or go below ground.

W – Wiper of the Potentiometer. This pin is the wiper terminal of the potentiometer. Its position on the resistor array is controlled by the 3–terminal control port. Voltage applied to the W–terminal cannot exceed the power–supply voltage, V_{CC}, or go below ground.

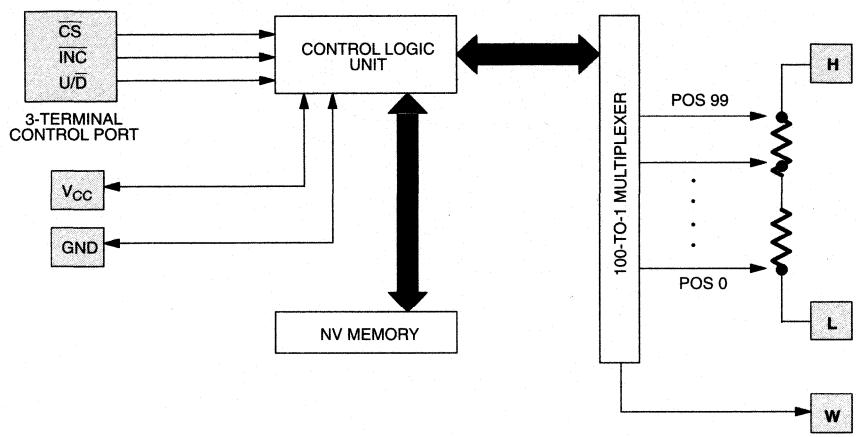
$\overline{CS}$ – Chip Select. The $\overline{CS}$ input is used to activate the control port of the DS1804. This input is active low. When in a high–state, activity on the $\overline{INC}$ and U/$\overline{D}$ port pins will not affect or change wiper position.

$\overline{INC}$ – Wiper Movement Control. This input provides for wiper position changes when the $\overline{CS}$ pin is low. Wiper position changes of the W–terminal will occur one position per high–to–low transition of this input signal. Position changes will not occur if the $\overline{CS}$ pin is in a high–state.

U/$\overline{D}$ – Up/Down Control. This input sets the direction of wiper movement. When in a high–state and $\overline{CS}$ is low, any high–to–low transition on $\overline{INC}$ will cause a one position movement of the wiper towards the H–terminal. When in a low–state and $\overline{CS}$ is low, any high–to–low transitions on $\overline{INC}$ will cause the position of the wiper to move towards the L–terminal.

4

DS1804 BLOCK DIAGRAM Figure 1



POWER–UP/POWER–DOWN CONDITIONS

On power–up the DS1804 will load the value of EEPROM memory into the wiper position register (or 1 of 100 decoder). The value of this register can then be set to another wiper position if desired, by using the 3–terminal control port. On power–up, wiper position will be loaded within a maximum time period of 500 µs once the power–supply is stable. Additionally, the 3–terminal interface port will be active after 50 ms.

On power–down, the wiper position register data will be lost. On the next device power–up, the value of EEPROM memory will be loaded into the wiper position register.

On shipment from the factory, Dallas Semiconductor does not guarantee a specified EEPROM memory value. This value should be set by the customer as needed. The next section discusses wiper storage operation for the DS1804.

NONVOLATILE WIPER STORAGE

Wiper position of the DS1804 can be stored using the $\overline{INC}$ and $\overline{CS}$ inputs. Storage of the wiper position takes place, whenever the $\overline{CS}$ input transitions from low–to–high while the $\overline{INC}$ is high. Once this condition has occurred the value of the current wiper position will be written to EEPROM memory.

The DS1804 is specified to accept 50,000 writes to EEPROM before a wear–out condition. After wearout the DS1804 will still function and wiper position can be changed during powered conditions using the 3–terminal control port. However, on power–up the wiper–position will be indeterminate.

ONE TIME PROGRAMMABILITY (OTP)

The DS1804 can be easily used as an OTP device. The user of the DS1804 can trim the desired value of the wiper position and set this position for storage as described above. Any activity through the 3–terminal port can then be prevented by connecting the $\overline{CS}$ input pin to V_{CC}. Also, an OTP application does not adversely affect the number of times EEPROM is written, since EEPROM will only be loaded and ***not written*** during a power–up or power–down condition.

On power–up the DS1804 will load the current value of EEPROM memory into the wiper position register.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–1.0V to +7.0V
Operating Temperature	0°C to 70°C; commercial –40°C to +85°C; industrial
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(–40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	+2.7		5.5	V	1
Input Logic 1	V_{IH}	2.0		V_{CC}+0.5	V	1, 2
Input Logic 0	V_{IL}	–0.5		+0.8 +0.6	V	1, 15
Resistor Inputs	L, H, W	GND–0.5		V_{CC}+0.5	V	1, 3

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC}=2.7V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}			400	µA	4
Input Leakage	I_{LI}	–1		+1	µA	
Wiper Resistance	R_W		400	1000	Ω	
Wiper Current	I_W			1	mA	
Standby Current 3 Volts 5 Volts	I_{STBY}		 10 20	 40	 µA µA	5
Wiper Load Time	t_{WLT}		500		µs	6
Power–Up Time	t_{PU}		50		ms	14

ANALOG RESISTOR CHARACTERISTICS

(–40°C to +85°C; V_{CC}=2.7V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Total Resistance			10 50 100		KΩ	7
End–to–End Resistor Tolerance		–20		+20	%	8
Absolute Linearity			±0.6		LSB	9
Relative Linearity			±0.25		LSB	10
–3 dB Cutoff Frequency	f_{cutoff}				MHz	11
Temperature Coefficient			650		ppm/°C	

CAPACITANCE

(25°C; V_{CC}=2.7V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	12
Output Capacitance	C_{OUT}			7	pF	12

AC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC}=2.7V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CS}$ to $\overline{INC}$ Setup	t_{CI}	50			ns	13
U/$\overline{D}$ to $\overline{INC}$ Setup	t_{DI}	100			ns	13
$\overline{INC}$ Low Period	t_{IL}	50			ns	13
$\overline{INC}$ High Period	t_{IH}	100			ns	13
INC Inactive to $\overline{CS}$ Inactive	t_{IC}	500			ns	13
$\overline{CS}$ Deselect Time	t_{CPH}	100			ns	13
Wiper Change to $\overline{INC}$ Low	t_{IW}			200	ns	13
$\overline{INC}$ Rise and Fall Times	t_R, t_F			500	µs	13
$\overline{INC}$ Low to $\overline{CS}$ Inactive	t_{IK}	50			ns	16
Wiper Storage Time	t_{WST}			10	ms	13, 17

NOTES:

1. All voltages are referenced to ground.
2. Valid for V_{CC} = 5V only.
3. Resistor input voltages cannot go below ground or exceed V_{CC} by the amounts as shown in the table.
4. Maximum current specifications are based on the clock rate of $\overline{INC}$ input. This specification represents the current required when changing the wiper position.
5. Standby current levels apply when all inputs are driven to appropriate supply levels. $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ = V_{CC}.
6. Wiper load time is specified as the time required for the DS1804 to load the wiper position with the contents of nonvolatile memory once V_{CC} has reached a stable operating voltage equal to or greater than 2.7V.
7. The DS1804 is available in three resistor values. These include the DS1804–010; 10KΩ , the DS1804–050 50KΩ; and the DS1804–100 100KΩ.
8. The end–to–end resistance tolerance of the DS1804 can be expected to shift with temperature. However, this change will not exceed ±20% of the nominal resistor value of the part.
9. Absolute linearity is used to compare measured wiper voltage versus expected wiper voltage as determined by wiper position. The DS1804 is specified to provide an absolute linearity of ±0.60 LSB
10. Relative linearity is used to determined the change in voltage between successive tap positions. The DS1804 is specified to provide a relative linearity specification of ±0.25 LSB.
11. –3 dB cutoff frequency characteristics for the DS1804 depend on potentiometer total resistance. DS1804–010, 1 MHz, DS1804–050; 200 KHz, and DS1804–100; 100 KHz.

12. Capacitance values apply at 25°C.

13. See Figure 2.

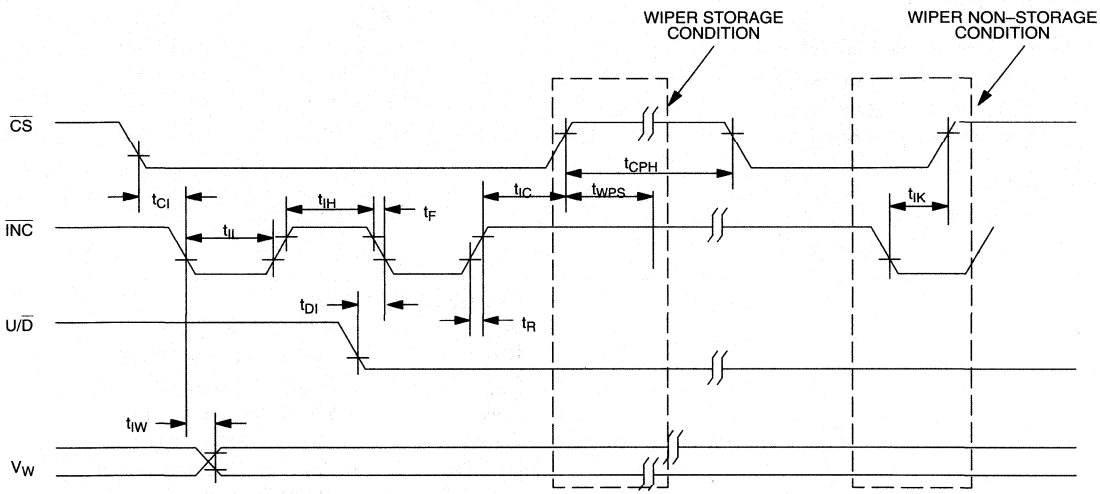
14. Power–up time is specified as the time required before the 3–terminal control becomes active after a stable power supply level has been reached.

15. At V_{CC} = 2.7V, V_{IL} = 0.8V

16. The $\overline{INC}$ low to $\overline{CS}$ inactive is specified to be 50 ns minimum. This is the transition condition which allows the DS1804 3–terminal port to become inactive without writing the EEPROM memory of the part.

17. Wiper Storage Time, t_{WST}, is the time require for the DS1804 to write EEPROM memory for storage of a new wiper position. The maximum time required to accomplish this task is specified at 10 ms.

3–TERMINAL INTERFACE TIMING DIAGRAM Figure 2



PRELIMINARY

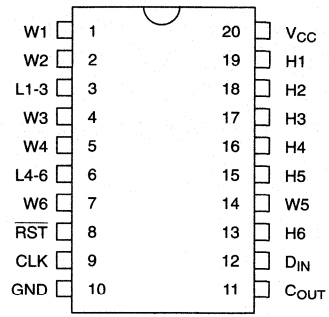
DALLAS SEMICONDUCTOR

DS1806
Digital Sextet Potentiometer

FEATURES

- Six digitally controlled 64–position potentiometers
- 3–Wire Serial Port provides for reading and setting each potentiometer
- Devices can be cascaded for single processor multi–device control
- Standard Resistance Values
  - DS1806–010 – 10K ohm
  - DS1806–050 – 50K ohm
  - DS1806–100 – 100K ohm
- Temperature:
  - Industrial: –40°C to +85° C
  - Commercial: 0°C to 70°C

PIN ASSIGNMENT



DS1806 20–PIN DIP (300 MIL)
DS1806S 20–PIN SOIC (300 MIL)
DS1806E 20–PIN TSSOP (173 MIL)
See Mech. Drawings Section

PIN DESCRIPTION

V_{CC}	–	3V or 5V Supply
$\overline{RST}$	–	Serial Port Reset Input
D_{IN}	–	Serial Port Data Input
CLK	–	Serial Port Clock Input
C_{OUT}	–	Cascade Data Output
H1 – H6	–	High End Terminal of Pot
W1 – W6	–	Wiper Terminal of Pot
GND	–	Ground
L1–3	–	Low Terminal Pots 1 thru 3
L4–6	–	Low Terminal Pots 4 thru 6

DESCRIPTION

The DS1806 is a six–channel digitally controlled solid–state linear potentiometer. Each potentiometer is comprised of 63 equiresistive sections as illustrated in the block diagram of Figure 1. Each potentiometer has three terminals accessible to the user. These include the high side terminals, H_X, the wiper terminals, W_X, and the low–end terminals, L1–3 and L4–6. Potentiometers 1 through 3 share the same low–end terminal L1–3. And likewise, potentiometers 4 through 6 share the low–end terminal L4–6.

Each wiper's position is selected via an 8–bit register value. Communication and control of the device is accomplished via a 3–wire serial port interface. This interface in conjunction with a cascade output allows the value of the device wiper settings to be read.

For multiple device and single processor environments, the DS1806 can be cascaded or daisy chained. This feature allows a single processor to control multiple devices.

The DS1806 is available in 10K, 50K and 100K ohm versions. The DS1806 is available in commercial and industrial temperature versions. Packages for the device include 20–lead DIPs, SOICs, and TSSOPs.

OPERATION

A block diagram of the device is provided in Figure 1. As shown, the DS1806 contains six 64–position potentiometers whose wiper positions are set by an 8–bit value. The DS1806 contains a 48–bit I/O shift register which is used to store the respective wiper position data for each of the six potentiometers.

Each potentiometer has three terminals accessible to the user. These include the high side terminals, H_X, the wiper terminals, W_X, and the low–end terminals, L1–3 and L4–6. Potentiometers 1 through 3 share the same low–end terminal L1–3. And likewise, potentiometers 4 through 6 share the low–end terminal L4–6.

Control of the DS1806 is accomplished via a 3–wire serial communication interface which allows the user to set the wiper position value for each potentiometer. The 3–wire serial interface consists of the control signals $\overline{RST}$, D_{IN}, and CLK. On power–up, the wiper positions of each potentiometer are set to the low–end terminal L_X. (00000000)

The $\overline{RST}$ control signal is used to enable 3–wire serial port operation. The $\overline{RST}$ signal (3–wire serial port) is active when in a high state. Any communication intended to change wiper settings must begin with the transition of the $\overline{RST}$ from the low–state to the high–state.

The CLK signal input is used to provide timing synchronization for data input and output. Wiper position data is loaded into the DS1806 through the D_{IN} input terminal. This data is shifted one–bit at a time into the 48–bit I/O shift register of the part, LSB first. Figure 3 provides an illustration of the 48–bit shift register.

Figure 4 provides 3–wire serial port protocol and timing diagrams. As shown, the 3–wire port is inactive when the $\overline{RST}$ signal input is low. Once $\overline{RST}$ has transitioned from the low to the high state, the serial port becomes active. When active, data is loaded into the I/O shift register on the low–to–high transition of the CLK.

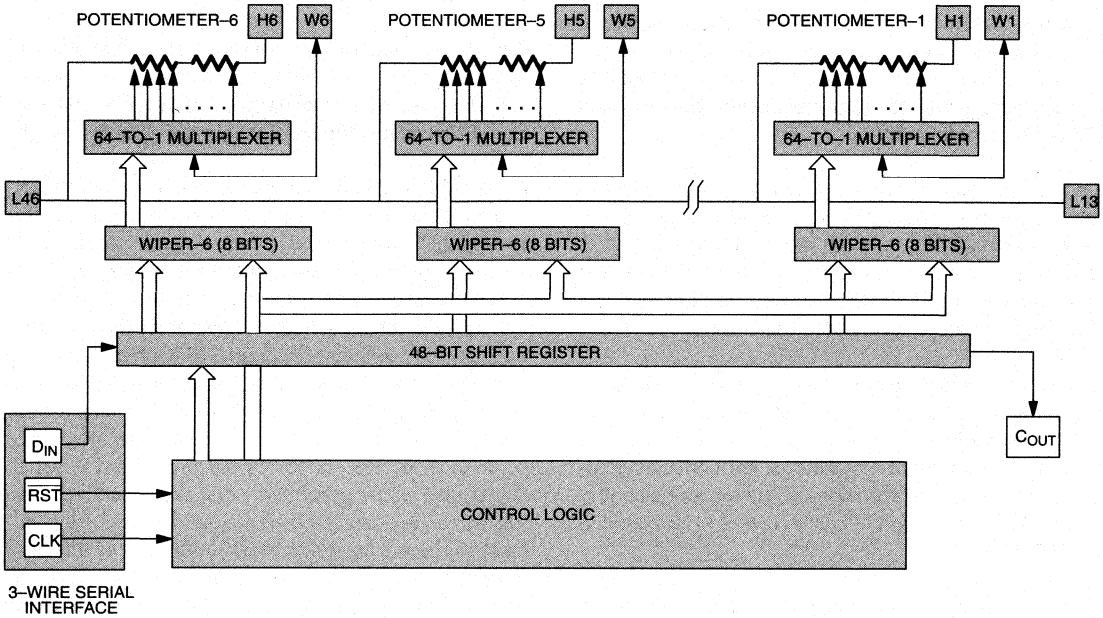
Data is transmitted in order of LSB first. Potentiometers are designated from 1 through 6 and the value for potentiometer–1 will be the first data entered into the shift register, followed by that of potentiometer–2 and so forth.

Each wiper has an 8–bit register which is used for setting the position of the wiper on the resistor array. Because the DS1806 is a 64–position potentiometer, only six bits of information are needed to set wiper position. The remaining two bits of information are used to provide a "don't change" feature. Wiper position is controlled by bit positions 0 through 5 of each register. The don't change feature is controlled by bits 6 and 7 of each register. When bits 6 and 7 have value "11 xxxxxx", wiper position will not change regardless of the states of bits 0 through 5. If bits 6 and 7 are set to any other value, bits 0 through 5 will be used as the new wiper position. The "don't change" feature allows the user to change the value of any potentiometer of the DS1806 without affecting or having to remember the remaining positions of the potentiometer wipers. Figure 2 provides the format for a wiper's register.

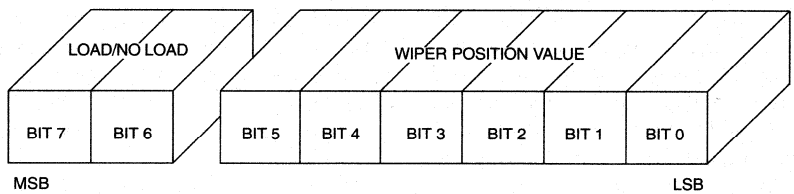
Wiper placement for each potentiometer is such that position–63 corresponds to the H_X terminal of the device while position–0 corresponds to the ground terminal. For example, to set a potentiometer's wiper position to 15 (decimal), the binary value shifted into the wiper register should be 00001111. This will place the wiper tap at the 15th step above the low end terminal, L_X.

All communication transactions should provide the total 48 bits of information when writing or reading from the part. This is especially true for applications using all six potentiometers. If a complete set of 48 bits is not transmitted to the part, undesired wiper position settings may occur.

DS1806 BLOCK DIAGRAM Figure 1



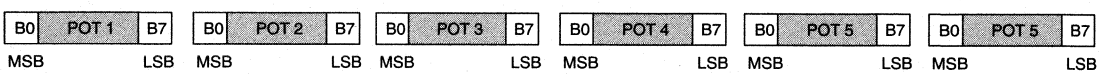
WIPER REGISTER CONFIGURATION Figure 2



Bits 6 and 7 Functionality

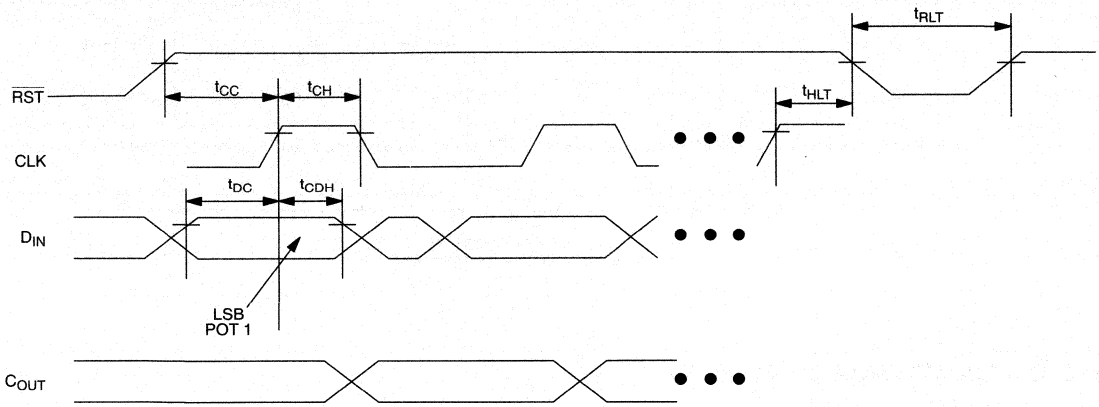
11 – Do not load wiper value
10– Load wiper value
01 – Load wiper value
00 – Load wiper value

48–BIT I/O SHIFT REGISTER Figure 3



Data entered LSB first.

3–WIRE SERIAL PORT TIMING Figure 4



CASCADE OPERATION

A feature of the DS1806 is the ability to control multiple devices from a single processor. Multiple DS1806s can be linked or daisy chained as shown in Figure 5. As a data bit is entered into the I/O shift register of the DS1806, a bit will appear at the C_{OUT} terminal before a maximum delay of 50 nanoseconds. The LSB of potentiometer–1 will always be the first out of the part at the beginning of a transaction. Additionally, the C_{OUT} terminal is always active regardless of the state $\overline{RST}$. However, D_{IN} and CLK inputs are ignored when $\overline{RST}$ is in the low state.

The C_{OUT} output of the DS1806 can be used to drive the D_{IN} input of another DS1806. When cascading multiple devices, the total number of bits transmitted is always 48 times the total number of DS1806s being cascaded.

An optional feedback resistor can be placed between the C_{OUT} terminal of the last device and the first DS1806 D_{IN} input, which allows the controlling processor to read, as well as, write data, or circularly clock data through the daisy chain. The value of the feedback or isolation resistor should be in the range from 1KΩ to 10KΩ.

To read data, the reading device configures itself as an input and monitors the state of the D_{IN} line, which is driven by C_{OUT} through the isolation resistor. When $\overline{RST}$ is driven high, bit 48 is present on the C_{OUT} pin, which is fed back to the input D_{IN} pin through the isolation resistor. When the CLK input transitions low to high, bit 48 is loaded into the first position of the I/O shift register and bit 47 becomes present on C_{OUT} and D_{IN} of the next device. After 48 bits (or 48 times the number of the DS1806s in the daisy chain), the data has shifted completely around and back to its original position. When $\overline{RST}$ transitions to the low state to end data transfer, the value (the same as before the read occurred) is loaded in the shift register.

ABSOLUTE AND RELATIVE LINEARITY

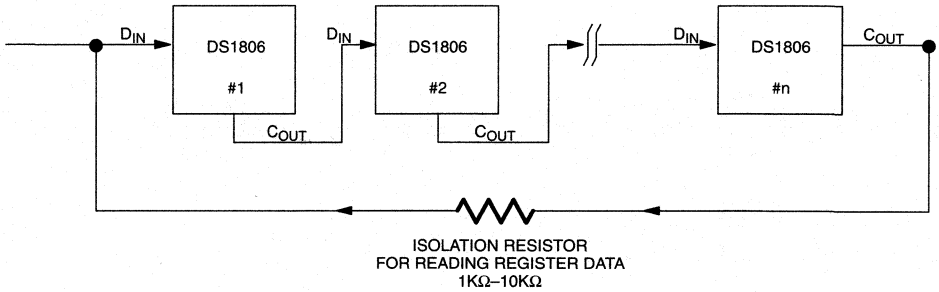
Absolute linearity is defined as the difference between the actual measured output voltage and the expected output voltage. Absolute linearity is given in terms of a minimum increment or expected output when the wiper is moved one position. The DS1806 is specified to have an absolute linearity of ±0.50 LSB.

Relative linearity is a measure of error between two adjacent wiper position points. The DS1806 is specified to have a relative linearity of ±0.25 LSB.

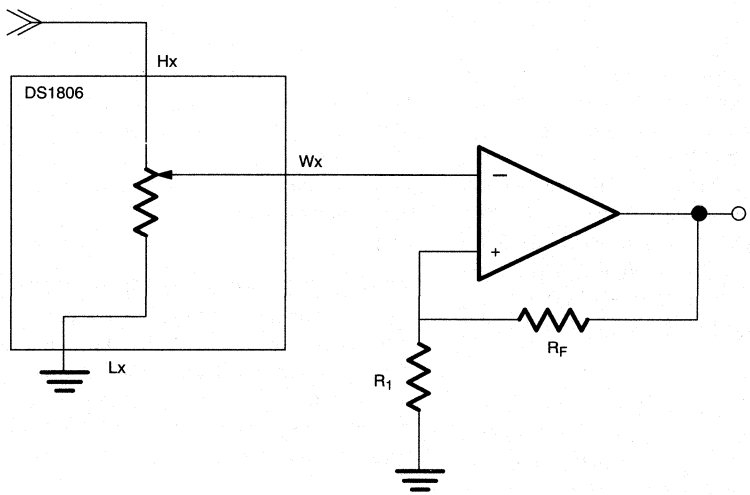
TYPICAL APPLICATION CONFIGURATIONS

Figure 6 shows the typical application configuration of the DS1806 as a fixed gain attenuator. In this configuration, the DS1806 adjusts the attenuation level of the incoming signal. Variations in wiper resistance are minimized by connecting the wiper terminal of the part to a high impedance load. Depending on voltage across the wiper, its resistance may vary from 400 ohms to 1000 ohms. Note that the resistance R1 in Figure 6 should be chosen to be much greater than the wiper resistance R_W.

CASCADING MULTIPLE DEVICES Figure 5



FIXED GAIN ATTENUATOR Figure 6



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	–40°C to +85°C; industrial
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(-40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	+2.7		5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(-40°C to +85°C; V_{CC} = 2.7 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current Active	I_{CC}		1.3	2	mA	
Input Leakage	I_{IL}	-1		+1	µA	
Wiper Resistance	R_W		400	1000	Ω	
Wiper Current	I_W			1	mA	
Input Logic 1	V_{IH}	2.0		V_{CC}+0.5	V	1
Input Logic 0	V_{IL}	-0.5		+0.8 +0.6	V	1, 6
Logic 1 Output @ 2.4 Volts	I_{OH}	–1			mA	
Logic 0 Output @ 0.4 Volt	I_{OL}			4	mA	6
Standby Current	I_{STBY}		50		µA	
Resistor Inputs	H_X, L_X, W_X	GND -0.5		V_{CC} +0.5	µA	2

ANALOG RESISTOR CHARACTERISTICS

(-40°C to +85°C; V_{CC} = 2.7 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
End-to-End Resistor Tolerance		-20		+20	%	
Absolute Linearity		-0.5		+0.5	LSB	7
Relative Linearity		-0.25		+0.25	LSB	8
-3 dB Cutoff Frequency	I_{cutoff}				Hz	4
Temperature Coefficient			650		PPM/°C	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	3
Output Capacitance	C_{OUT}			7	pF	3

AC ELECTRICAL CHARACTERISTICS

(-40°C to +85°C; V_{CC} = 2.7 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock Frequency	f_{CLK}	DC		10	MHZ	5
Width of CLK Pulse	t_{CH}	50			ns	5
Data Setup Time	t_{DC}	30			ns	5
Data Hold Time	t_{CDH}	0			ns	5
Propagation Delay Time Low to High Level Clock to Output	t_{PLH}			50	ns	5
$\overline{RST}$ High to Clock Input High	t_{CC}	50			ns	5
$\overline{RST}$ Low from lock Input High	t_{HLT}	50			ns	5
$\overline{RST}$ Inactive	t_{RLT}	125			ns	5
CLK Rise Time, CLK Fall Time	t_{CR}			50	ns	5

NOTES:

1. All voltages are referenced to ground.
2. Resistor inputs cannot go below GND by more than 0.5 Volts or above V_{CC} by 0.5 Volts in the positive direction by more than V_{CC}+0.5 volts.
3. Capacitance values apply at 25°C.
4. –3 dB cutoff frequency characteristics for the DS1806 depend on potentiometer total resistance: DS1806–010; 1MHz; DS1806–050; 200 KHz, DS1806–100; 100 KHz.
5. See Figure 4.
6. For V_{CC} = 5V ± 10% maximum V_{IL} = +0.8V. For V_{CC} = 3.0 ± 10% V_{IL} = +0.6V.
7. Absolute Linearity is to used measure expected wiper voltage versus measured wiper voltage as determined by wiper position. The DS1806 is specified to provide an Absolute Linearity of +0.5 LSB.
8. Relative Linearity is used to determine the change in wiper voltage between two adjacent wiper positions. The DS1806 is specified to provide a relative linearity of +0.25 LSB.

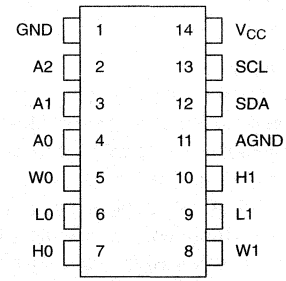
DALLAS SEMICONDUCTOR

DS1807
Addressable Dual Audio Taper Potentiometer

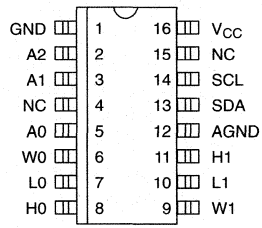
FEATURES

- Operates from 3V or 5V Power Supplies
- Ultra–low power consumption
- Two digitally controlled, 65–position potentiometers
- Logarithmic resistor characteristics (1 dB per step)
- Zero–crossing detection eliminates noise caused by discrete wiper changes
- Addressable using 3–Chip Select Inputs
- Serial/Synchronous Bus Interface
- Operating Temperature
  - Commercial: 0°C to 70°C
  - Industrial: –40°C to +85°C
- Resistance Value: 45KΩ

PIN ASSIGNMENT



DS1807 14–PIN DIP (300 MIL)
DS1807E 14–PIN TSSOP (173 MIL)



DS1807S 16–PIN SOIC (300 MIL)
See Mech. Drawings Section

PIN DESCRIPTION

L0,L1	–	Low End of Resistor
H0,H1	–	High End of Resistor
W0,W1	–	Wiper Terminal of Resistor
V_{CC}	–	3V/5V Power Supply Input
A0 . . . A2	–	Chip Select Inputs
SDA	–	Serial Data I/O
SCL	–	Serial Clock Input
GND	–	Digital Ground
AGND	–	Analog Ground
NC	–	No connection

DESCRIPTION

The DS1807 is a dual audio taper potentiometer having a logarithmic resistive characteristic. Each potentiometer has a total of 65 wiper positions including the mute position. Adjacent wiper positions are separated by 1 dB giving a total attenuation range of 64 dB. When the wipers are in the mute position, attenuation in excess of 90 dB is achieved. The DS1807 also provides a zero–crossing detection capability. This capability eliminates noise caused by discrete wiper position changes. The DS1807 is controlled via a two input, serial synchronous interface that provides the capability of addressing up to eight different DS1807s. Addressability is obtained via communication protocol and three (3) address select inputs A0, A1, and A2. Communication protocol allows

for the exact positioning of the DS1807 wiper's position. Additionally, communication protocol allows for independent or simultaneous setting of the two potentiometers wipers. Wiper positions can also be read via the 2–wire serial interface.

The DS1807 is available in 14–pin DIP, SOIC, and TSSOP packages. The DS1807 is offered in commercial and industrial temperature grades. The standard resistance of the DS1807 is 45KΩ.

DEVICE OPERATION

The DS1807 is an addressable, digitally controlled device that has two 65–position potentiometers. The DS1807 potentiometers are logarithmic tapers providing a resolution or step size of 1 dB per step from positions 0 through 63. The 64th position is the mute position and provides attenuation in excess of 90 dB. Moving the potentiometer's wiper from position 63 (or 63 dB of attenuation) to position 64 will provide a step size in excess of 30 dB. A functional block diagram of the part is shown in Figure 1.

As stated, each potentiometer is composed of a 65 position resistor array. Two 8–bit registers, each assigned to a respective potentiometer, are used to set wiper position on the resistor array. The wiper terminal is multiplexed to one of 65 positions on the resistor array based on its corresponding 8–bit register value.

Because the DS1807 has 65 positions, only seven bits of data are needed to set a wiper's position. Bits 0 through 5 of the register are used to set the position on the resistor array. Bit 6 is used to set the wiper position to the mute position and bit 7 is a don't care. *If the value of bit 6 is set equal to '1', regardless of all other bit values, the wiper position of the respective potentiometer will be set to the mute position.* An example diagram of the wiper register and associated bit function is provided in Figure 2.

The DS1807 is designed to operate as an attenuator. (see Figure 3) As such, wiper position values are set with respect to the amount of attenuation desired. For example, if the user wishes to attenuate an incoming signal by 6 dB, the wiper position register value(s) should be set to binary (0000 0110).

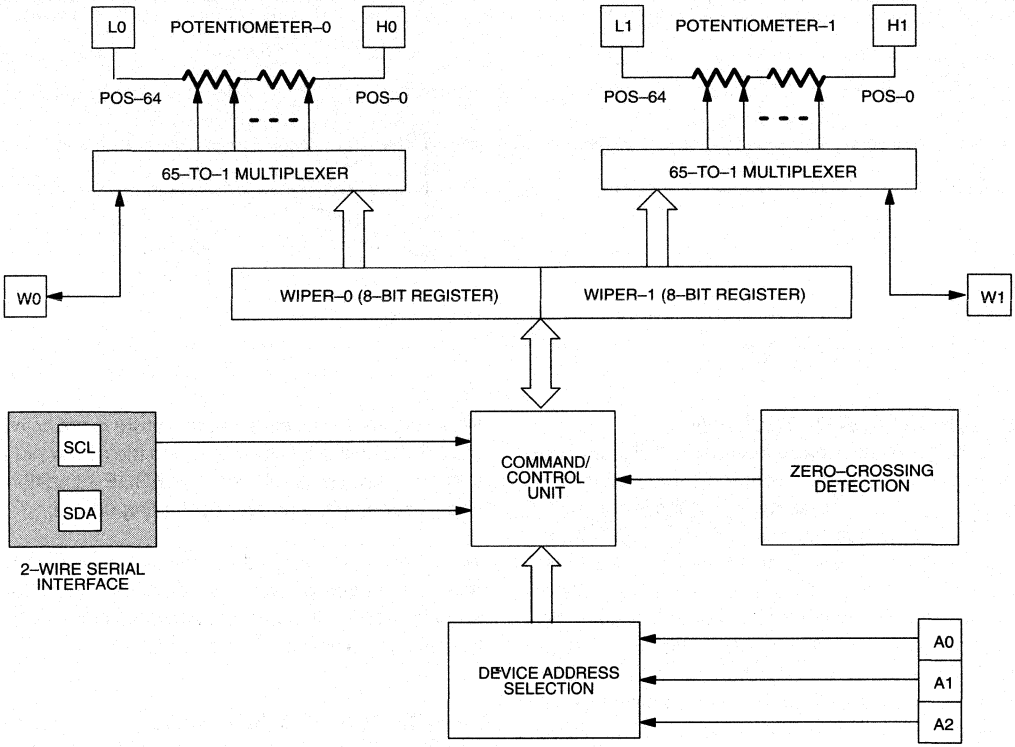
The H0 and H1 terminals of the DS1807 have wiper position values (binary) 0000 0000. These terminals provide 0 dB of attenuation for the input signal.

The L0 and L1 terminals provide the greatest attenuation of the input signal. They represent the mute positions for the DS1807 and have wiper position values (binary) 0100 0000 or greater.

On power–up, the serial port is stable and active within 10 microseconds. Additionally, DS1807 wiper positions will be set to position 63 or (binary) 0011 1111; one position above mute. The user may then set the wiper register to a desired value.

Communication with the DS1807 takes place over the 2–wire serial interface consisting of the bi–directional data terminal, SDA, and the serial clock input, SCL. The 2–wire serial interface and chip select inputs A0, A1, and A2 allow operation of up to eight devices in a bus topology; with A0, A1, and A2 being the physical address of the device. Complete details of the 2–Wire interface are discussed in the section entitled "2–Wire Serial Data Bus".

DS1807 BLOCK DIAGRAM Figure 1



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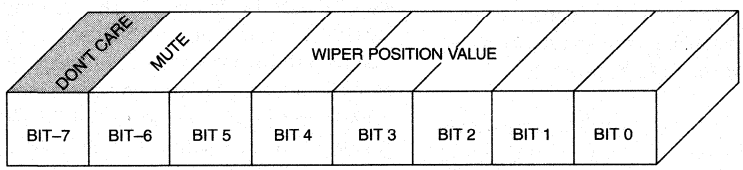
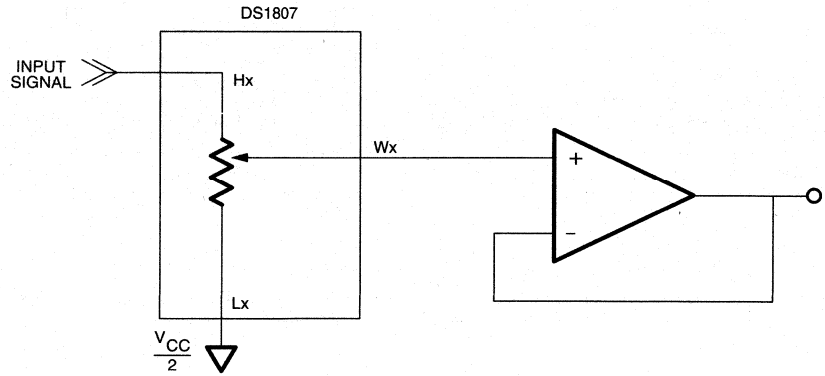
WIPER REGISTER CONFIGURATION Figure 2



DS1807 ATTENUATOR CONFIGURATION Figure 3



ZERO–CROSSING DETECTION

The DS1807 provides many features for digitally controlled audio applications. Zero–crossing detection is useful in eliminating "zipper noise" , which is commonly associated with digital potentiometers. Zipper Noise (because it sounds like a zipper) is caused by discrete wiper position changes on the resistor array. These changes cause discontinuities in the audio output signal which are manifested as audible pops heard at the output of the audio chain. If subsequent amplification follows the digital potentiometer, this audible noise can be quite disturbing. The DS1807 minimizes zipper noise by allowing wiper position changes only during zero–crossings of the input signal.

The zero–crossing detection feature can be enabled or disabled via software. The complete software command for enabling or disabling zero–crossing is discussed in the section, "2–wire serial data bus".

When enabled, the zero crossing detect feature allows *independent* wiper changes within a 50 millisecond time window when the Hx and Lx (where x = 0 or 1) terminals have equal potentials. The 50 millisecond time window begins once the DS1807 has responded with an ACKNOWLEDGE after a "write potentiometer " command. The STOP condition is discussed in the following section.

If at 50 milliseconds the DS1807 has not detected a zero–crossing (Hx – Lx = 0), the wiper position of the potentiometer(s) will change regardless of the state of the input signal.

When the zero–crossing detect feature is not activated, the DS1807 will allow movement to the new wiper position as soon as the ACKNOWLEDGE condition has been issued by the master controlling device.

The DS1807 is designed to provide the zero–crossing detection feature when initially powered. If this feature is not to be used, it must be deactivated once the device has reached a fully powered condition.

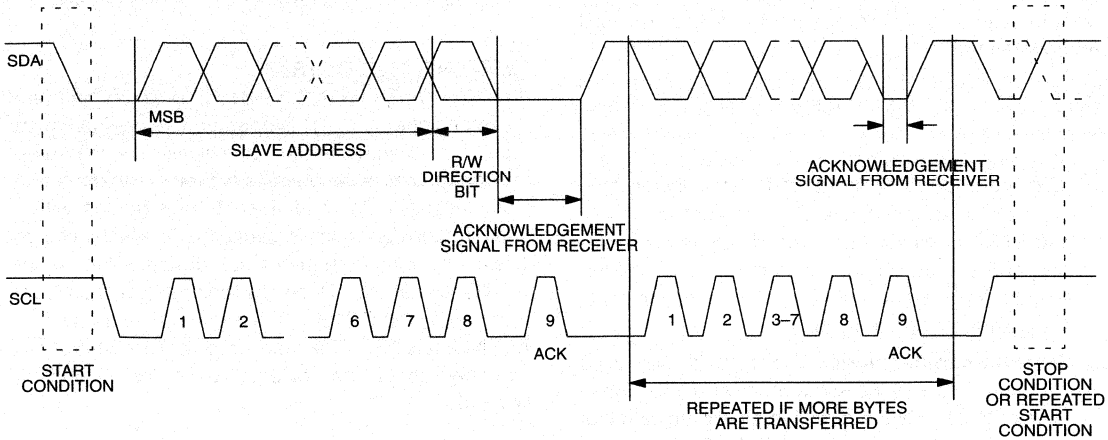
2–WIRE SERIAL DATA BUS

The DS1807 supports a bi–directional two–wire bus and data transmission protocol. A device that sends data on the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a "master". The devices that are controlled by the master are "slaves". The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS1807 operates as a slave on the two–wire bus. Connections to the bus are made via the open–drain I/O line, SDA, and the serial clock line, SCL.

The following bus protocol has been defined (See Figure 4).

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high will be interpreted as control signals.

2–WIRE DATA TRANSFER OVERVIEW Figure 4



Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW , while the clock is HIGH, defines a START condition.

Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data. Figure 4 details how data transfer is accomplished on the two–wire bus. Depending upon the state of the R/W bit, two types of data transfer are possible:

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte–wise and each receiver acknowledges with a ninth bit.

Within the bus specifications a regular mode (100 KHz clock rate) and a fast mode (400 KHz clock rate) are defined. The DS1807 works in both modes.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

1. **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the control byte (or slave address). Next follows a number of data bytes. The slave returns an acknowledge bit after each received. byte.
2. **Data transfer from a slave transmitter to a master receiver.** The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit . Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a 'not acknowledge' is returned.

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer

is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

The DS1807 may operate in the following two modes:

1. **Slave receiver mode:** Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.
2. **Slave transmitter mode:** The first byte is received and handled as in the slave receiver mode. However, in this mode the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1807 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

SLAVE ADDRESS

A control byte is the first byte received following the START condition from the master device. The control byte consists of a four bit control code. For the DS1807, this is set as 0101 binary for read/write operations. The next three bits of the control byte are the device select bits (A2, A1, and A0). They are used by the master device to select which of eight devices are to be accessed. The select bits are in effect the three least significant bits of the slave address. The last bit of the control byte (R/W) defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. Figure 5 shows the control byte structure for the DS1807.

Following the START condition, the DS1807 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving the 0101 address code and appropriate device select bits, the slave device outputs an acknowledge signal on the SDA line.

COMMAND AND PROTOCOL

The command and protocol structure of the DS1807 allows the user to read or write the potentiometer(s). The command structures for the part are presented in Figures 6 and 7. Potentiometer data values and control and command values are always transmitted most significant bit (MSB) first. During communications, the receiving unit always generates the acknowledge.

READING THE DS1807

As shown in Figure 6, the DS1807 provides one read command operation. This operation allows the user to read both potentiometers. Specifically, the R/W bit of the control byte is set equal to a 1 for a read operation. Communication to read the DS1807 begins with a START condition which is issued by the master device. The control byte from the master device will follow the START condition. Once the control byte has been received by the DS1807, the part will respond with an ACKNOWLEDGE. The read/write bit of the control byte as stated should be set equal to '1' for reading the DS1807.

When the master has received the ACKNOWLEDGE from the DS1807, the master can then begin to receive potentiometer wiper data. The value of the potentiometer–0 wiper position will be the first returned from the DS1807. Once the eight bits of the potentiometer–0 wiper position have been transmitted, the master will need to issue an ACKNOWLEDGE, unless it is the only byte to be read, in which case the master issues a NOT ACKNOWLEDGE. If desired the master may stop the communication transfer at this point by issuing the STOP condition. However, if the value of the potentiometer–1 wiper position value is needed communication transfer can continue by clocking the remaining eight bits of the potentiometer–1 value, followed by a NOT ACKNOWLEDGE. Final communication transfer is terminated by issuing the STOP command. Again the flow of the read operation is presented in Figure 6.

WRITING THE DS1807

A data flow diagram for writing the DS1807 is shown in Figure 7. The DS1807 has three commands which are used to change the position(s) of the wiper. These include write pot–0, write pot–1, and write pot–0/1. The write pot–0 command allows the user to write the value of potentiometer–0 and as an option the the value of potentiometer–1. The write–1 command allows the user to write the value of potentiometer–1 only. The last write command, write–0/1, allows the user to write both potentiometers to the same value with one command and one data value being issued.

All the write operations begin with a START condition. Following the START condition, the master device will issue the control byte. The read/write bit of the control byte will be set to '0' for writing the DS1807. Once the control byte has been issued and the master receives the acknowledgment from the DS1807, the command byte is transmitted to the DS1807. As mentioned above, there exist three write operations that can be used with the DS1807. The binary value of each write command is shown in Figure 7 and also in Table 1.

2–WIRE WRITE COMMAND WORDS Table 1

COMMAND	COMMAND VALUE
Write Potentiometer–0	101010 01
Write Potentiometer–1	101010 10
Write Both Pots	101011 11

Once the DS1807 has received the command byte, it will responds with an ACKNOWLEDGE. The master can then write the corresponding data–byte associated with the command byte. When the DS1807 has received the data byte(s), it will respond with an acknowledge. At this point the master device should respond with the STOP condition.

ZERO–CROSSING DETECTION COMMAND WORD

Zero–crossing detection was described under the operation section of this document. As stated earlier, zero–crossing detection must be deactivated or activated under software control. The command words used to activate or deactivate the zero–crossing detection feature is shown in Table 2.

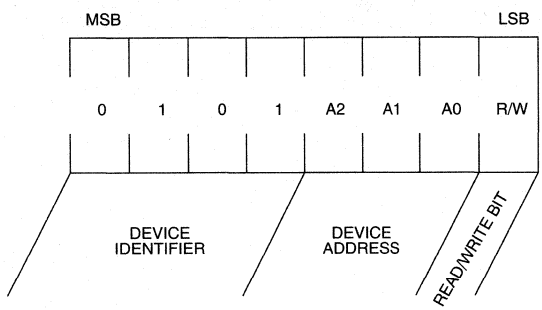
ZERO–CROSSING DETECTION COMMAND WORDS Table 2

COMMAND	COMMAND VALUE
Activate Zero–Crossing	101111 01
Deactivate Zero–Crossing	101111 10

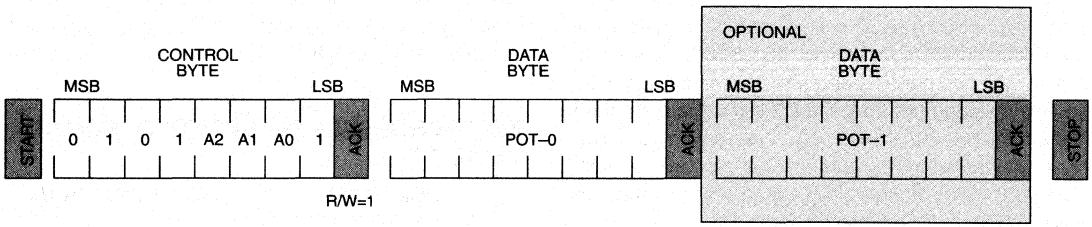
Communication to activate or deactivate zero–crossing detection begins with a START condition which is issued by the master device. The control byte from the master device will follow the START condition. Once the control byte has been received by the DS1807, the part will respond with an ACKNOWLEDGE. The read/write bit of the control byte, as stated, should be set equal to '0' for writing the DS1807.

When the master has received the ACKNOWLEDGE from the DS1807, the master can then begin to transmit the desired zero–crossing detection mode. Once the DS1807 has received the command byte, it will respond with an ACKNOWLEDGE. At this point, the master device should respond with the STOP condition.

CONTROL BYTE Figure 5

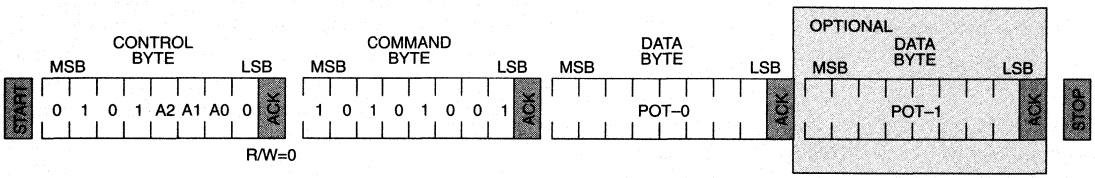


2–WIRE READ PROTOCOL Figure 6

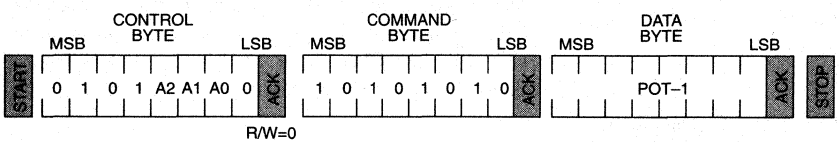


2–WIRE WRITE PROTOCOLS Figure 7

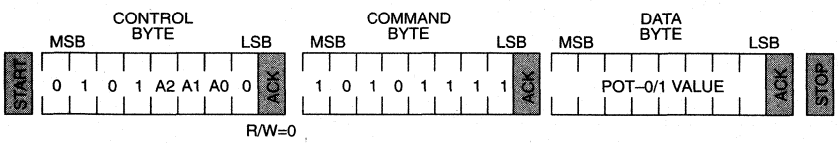
Write Pot–0



Write Pot–1



Write Pot–0/1 (same value)



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–1.0V to +7.0V
Operating Temperature	0°C to 70°C; commercial –40°C to +85°C; industrial
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(–40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	+2.7		5.5	V	1
Resistor Inputs	L,H,W	GND–0.5		V_{CC}+0.5	V	1
Ground	GND	GND		GND	V	1, 16
Analog Ground	AGND	GND –0.7		GND +0.7	V	1, 16

4

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC}=2.7V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Current Active	I_{CC}				2000	µA	3
Input Leakage	I_{LI}		–1		+1	µA	
Wiper Resistance	R_W			400	1000	Ω	
Wiper Current	I_W				1	mA	
Input Logic 1	V_{IH}		0.7V_{CC}		V_{CC}+0.5	V	1, 2
Input Logic 0	V_{IL}		GND–0.5		0.3V_{CC}	V	1, 2
Input Logic Levels A0, A1, A2		Input Logic 1 Input Logic 0	0.7V_{CC} GND–0.5		V_{CC}+0.5 0.3V_{CC}	V	13
Input Current each I/O Pin		$0.4<V_{I/O}<0.9V_{DD}$	–10		10	µA	
Standby Current 3V 5V	I_{STBY}			12 20	40	µA	4
Low Level Output Voltage	V_{OL1}	3 mA sink current	0.0		0.4	V	
	V_{OL2}	6 mA sink current	0.0		0.6	V	
I/O Capacitance	$C_{I/O}$				10	pF	
Pulse Width of Spikes which must be suppressed by the input filter	t_{SP}	Fast Mode	0		50	ns	

ANALOG RESISTOR CHARACTERISTICS

(–40°C to +85°C; V_{CC}=2.7V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Resistance		36	45	54	KΩ	
Absolute Tolerance		–1		+1	dB	10
Interchannel Matching		–0.5		+0.5	dB	15
Tap–to–Tap		–0.25		+0.25	dB	11
–3 dB Cutoff Frequency	f_{cutoff}	700			KHz	14
Temperature Coefficient			650		ppm/°C	
Total Harmonic Distortion (V_{IN}=1 V_{RMS}, 1 KHz, Tap=–6 dB)	THD		0.002		%	14
Output Noise (20 Hz to 20 KHz, Grounded Input, Tap=–6 dB)			2.2		μV_{RMS}	14
Digital Feedthrough (20 Hz to 20 KHz, Tap=–6 dB)			–90		dB	14
Interchannel Isolation (1 KHz, Tap=–6 dB)			–100		dB	14
Mute Control Active			–100		dB	

AC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC}=2.7V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
SCL Clock Frequency	f_{SCL}	0 0		400 100	KHz	* **
Bus Free Time Between STOP and START Condition	t_{BUF}	1.3 4.7			µs	* **
Hold Time (Repeated) START Condition	$t_{HD:STA}$	0.6 4.0			µs	5
Low Period of SCL Clock	t_{LOW}	1.3 4.7			µs	
High Period of SCL Clock	t_{HIGH}	0.6 4.0			µs	
Data Hold Time	$t_{HD:DAT}$	0 0		0.9	µs	6, 7
Data Set–Up Time	$t_{SU:DAT}$	100 250			ns	8
Rise Time of both SDA and SCL Signals	t_R	$20+0.1C_R$		300 1000	ns	9
Fall Time of both SDA and SCL Signals	t_F	$20+0.1C_R$		300 300	ns	9
Set–Up Time for STOP Condition	$t_{SU:STO}$	0.6 4.0			µs	
Capacitive Load for each Bus Line	C_R			400	pF	

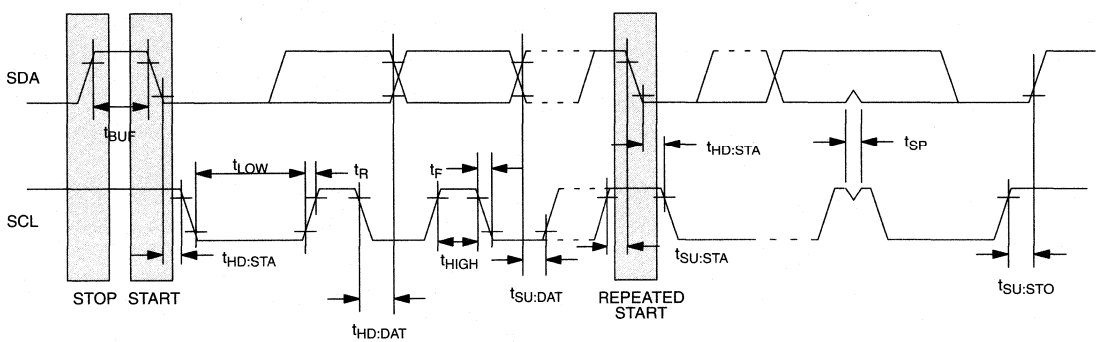
*fast mode

**standard mode

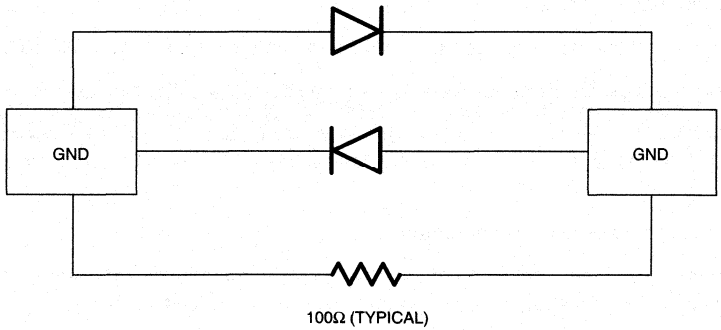
NOTES:

1. All voltages are referenced to ground.
2. I/O pins of fast mode devices must not obstruct the SDA and SCL lines if V_{DD} is switched off.
3. I_{CC} specified with zero–crossing detect active and operating device serial port in fast mode.
4. I_{STBY} specified with for V_{CC} equal 3.0V and 5.0V and SDA and SCL are driven to the appropriate logic levels. I_{STBY} is specified as the current consumption of the device when SDA and SCL are in the inactive (high) states.
5. After this period, the first clock pulse is generated.
6. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
7. The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
8. A fast mode device can be used in a standard mode system, but the requirement $t_{SU:DAT} > 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{RMAX} + t_{SU:DAT} = 1000+250=1250$ ns before the SCL line is released.
9. C_B – total capacitance of one bus line in picofarads, timing referenced to $(0.9(V_{CC})$ and $(0.1)(V_{CC}))$.
10. Absolute tolerance is used to determine measured wiper voltage versus expected wiper voltage as determined by wiper position.
11. Tap–to–Tap tolerance is used to determine the change in voltage between successive tap positions. The DS1807 is specified for a ±0.25 dB tap–to–tap tolerance.
12. Typical values are for $t_A = 25°C$ and nominal supply voltage.
13. Address Inputs, A0, A1, and A2, should be tied to either V_{CC} or GND depending on the desired address selections.
14. These parameters are characterized and not 100% tested.
15. Interchannel matching is used to determine the relative difference in dB between the same position on each potentionmeter. The DS1807 is specified for ±0.5 dB Interchannel matching.
16. See Figure 9.

TIMING DIAGRAM Figure 8



INTERNAL GROUND CONNECTIONS Figure 9



NOTE: GND and AGND must be tied to the same voltage level.

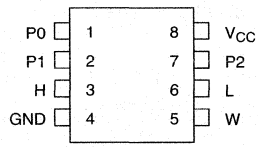
DALLAS SEMICONDUCTOR

DS1866
Log Trimmer Potentiometer

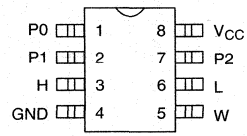
FEATURES

- Single 8-position Log Trimmer Potentiometer 5-dB/step
- Operates from 2.7V to 5.5V supplies
- Parallel interface control: P0, P1, P2
- Resistance values: 10KΩ
- 8-pin DIPs; 8-pin (150) SOICs
- Operating temperature:
  - Commercial: 0°C to +70°C
  - Industrial: –40°C to +85°C

PIN ASSIGNMENT



8-Pin DIP (300 Mil)
See Mech. Drawings Section



8-Pin SOIC (150 Mil)
See Mech. Drawings Section

PIN DESCRIPTION

H	–	High End of Resistor
L	–	Low End of Resistor
W	–	Wiper Terminal
V_{CC}	–	3V or 5V Power Supply Input
P0	–	Position Select – Bit-0
P1	–	Position Select – Bit-1
P2	–	Position Select – Bit-2
GND	–	Ground

DESCRIPTION

The DS1866 is a single volatile digital potentiometer having eight positions with a 5 dB resolution per step. The device provides an ideal method for low-cost trimming or volume control using a CPU or manual control input. The device's wiper position is set to one of eight positions by a 3-terminal parallel port. The value of the wiper position is determined by the states the P0, P1, and P2 port pins.

The DS1866 is available as a 10K potentiometer and in commercial and industrial versions. Additionally, the DS1866 will operate from 3V or 5V supplies and is ideal for portable application requirements requiring low standby current. Two packaging options are available and include the 8-pin (300 mil) DIP, 8-pin (150 mil) SOIC.

OPERATION

The DS1866 is a single volatile potentiometer. The device has a total of eight positions providing a resolution of 5 dB per step and giving a total attenuation range of 0 dB to -35 dB. These tap points are accessible to the W-terminal whose position is controlled via a 3-terminal parallel port consisting of input signals P0, P1, and P2. A block diagram of the DS1866 is shown in Figure 1.

Wiper position setting of the DS1866 is determined by the states of the P0, P1, and P2 input terminals. Table 1 below outlines position setting versus value of the parallel port inputs. A Position-0 setting places the wiper position at the L-terminal of the potentiometer and provides 35 dB of attenuation. As wiper position increase, attenuation decreases with position 7 giving 0 dB of attenuation.

On power–up, the wiper position of the DS1866 will be set to the P0, P1, and P2 values.

P0 P1 P2 (binary)	Wiper Position	Attenuation (dB)
000	0	35 dB
001	1	30 dB
010	2	25 dB
011	3	20 dB
100	4	15 dB
101	5	10 dB
110	6	5 dB
111	7	0 dB

PIN DESCRIPTIONS

V_{CC} – Power Supply Terminal. The DS1866 will support supply voltages ranging from +2.7 to +5.5 volts.

GND – Ground Terminal.

H – High-end Resistor. This is the high–end terminal of the potentiometer. It is not required that this terminal be connected to a potential greater than the L–terminal. Maximum voltage on the H-terminal can not exceed the power supply voltage, V_{CC}, or go below ground.

L – Low-end Resistor. This is the low–end terminal of the potentiometer. It is not required that this terminal be connected to a potential less than the H-terminal. Maximum voltage on the L-terminal can not exceed the power-supply voltage, V_{CC}, or go below ground.

W – Wiper of the Potentiometer. This pin is the wiper terminal of the potentiometer. Its position on the resistor array is controlled by the 3-terminal parallel port. Maximum voltage on the W-terminal can not exceed the power supply voltage, V_{CC}, or go below ground.

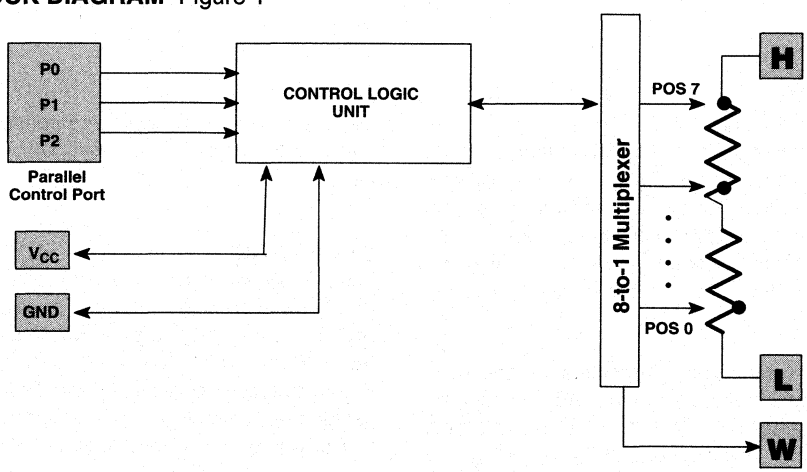
P0 – Bit-0. P0 is the bit-0 data input to the parallel port.

P1 – Bit-1. P1 is the bit-1 data input to the parallel port.

P2 – Bit-2. P2 is the bit-2 data input to the parallel port.

One Time Programmability (OTP). The DS1866 can be easily used as an OTP device. This can be accomplished by terminating the P0, P1, or P2 to desired logic levels during system manufacturing. One power up, the value of P0, P1, and P2 will then set the wiper position setting of the DS1866.

DS1866 BLOCK DIAGRAM Figure 1



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	0°C to 70°C, commercial –40°C to +85°C, industrial
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(–40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	+2.7		5.5	V	1
Input Logic 1	V_{IH}	2.0		V_{CC} +0.5	V	1, 2
Input Logic 0	V_{IL}	–0.5		+0.8 +0.6	V	1, 2
Ground	GND	GND –0.5		GND +0.5		
Resistor Inputs	L, H, W	GND –0.5		V_{CC} +0.5	V	1, 3

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC} = 2.7V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}			400	µA	4
Input Leakage	I_U	–1		+1	µA	
Wiper Resistance	R_W		400	1000	Ω	
Wiper Current	I_W			1	mA	
Standby Current 3 volts 5 volts	I_{STBY}		 10 20	 40	 µA µA	5

ANALOG RESISTOR CHARACTERISTICS

(–40°C to +85°C; V_{CC} = 2.7V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Total Resistance		8	10	12	KΩ	6
Absolute Tolerance		–1.0		1.0	dB	8
Tap-to-Tap		–1.0		1.0	dB	9
–3 dB Cutoff Frequency	f_{cutoff}		1MHz		MHz	10
Temperature Coefficient		650		ppm/°C		

CAPACITANCE

(25°C; V_{CC} = 2.7V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	11
Output Capacitance	C_{OUT}			7	pF	11

AC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC} = 2.7V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Parallel Port Transition	t_{PC}			200	ns	12

NOTES:

1. All voltages are referenced to ground.
2. For V_{CC} = 5V ± 10% maximum V_{IL} = +0.8V. For V_{CC} 3.0 ± 10% V_{IL} = +0.6V. For V_{CC}=2.7 volts V_{IH}=2.0 volts minimum.
3. Resistor input voltages cannot go below ground or exceed V_{CC} by the amounts as shown in the table.
4. Maximum current specifications are based on the change rate of the parallel port inputs P0, P1, and P2.
5. Standby current levels apply when all inputs are driven to appropriate supply levels.
6. The DS1866 is available as a 10 KΩ potentiometer.
7. The end-to-end resistance tolerance of the DS1866 can be expected to shift with temperature. However, this change will not exceed ±20% of the nominal resistor value of the part.
8. Absolute Tolerance is used to compare measured wiper voltage versus expected wiper voltage as determined by wiper position. The DS1866 is specified to provide an absolute tolerance of ±1.0 dB.
9. Tap-to-tap Tolerance is used to determine the change in voltage between successive tap positions. The DS1866 is specified to provide a tap-to-tap tolerance specification of ±1.0 dB.
10. –3 dB cutoff frequency characteristics for the DS1866 is 1 MHz.
11. Capacitance values apply at 25°C.
12. This specification refers to the time difference between parallel port input changes to stabilize and wiper transition.

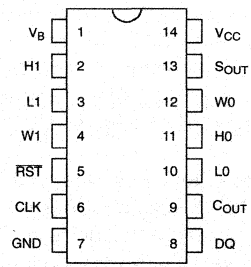
DALLAS SEMICONDUCTOR

DS1867
Dual Digital Potentiometer with EEPROM

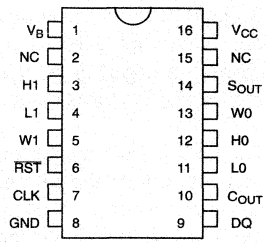
FEATURES

- Nonvolatile version of the popular DS1267
- Low power consumption, quiet, pumpless design
- Operates from single 5V or ±5V supplies
- Two digitally controlled, 256–position potentiometers
- Wiper position is maintained in the absence of power
- Serial port provides means for setting and reading both potentiometers
- Resistors can be connected in series to provide increased total resistance
- 16–pin SOIC and 20–pin TSSOP for surface mount applications
- Standard resistance values:
  - DS1867–10 ~ 10KΩ
  - DS1867–50 ~ 50KΩ
  - DS1867–100 ~ 100KΩ
- Temperature:
  - Commercial: 0°C to 70°C
  - Industrial: –40°C to +85°C

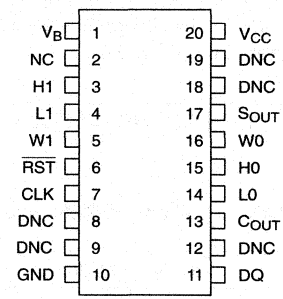
PIN ASSIGNMENT



14–PIN DIP (300 MIL)
See Mech. Drawings Section



16–PIN SOIC (300 MIL)
See Mech. Drawings Section



20–PIN TSSOP (173 MIL)
See Mech. Drawings Section

DESCRIPTION

The DS1867 is the nonvolatile version of the popular DS1267 Dual Digital Potentiometer. The DS1867 consists of two digitally controlled potentiometers having 256–position wiper settings. Wiper position is maintained in the absence of power through the use of EEPROM memory cell arrays. Communication and control of the device is accomplished over a 3–wire serial port which allows reads and writes of the wiper position. Both potentiometers can be stacked for increased total resistance with the same resolution. For multiple device–single processor environments, the DS1867 can be cascaded for control over a single 3–wire bus. The DS1867 is offered in three standard resistance values and commercial and industrial temperature versions.

PIN DESCRIPTION

L0, L1	–	Low End of Resistor
H0, H1	–	High End of Resistor
W1, W2	–	Wiper End of Resistor
V_B	–	Substrate Bias
S_{OUT}	–	Wiper for Stacked Configuration
$\overline{RST}$	–	Serial Port Reset Input
DQ	–	Serial Port Data Input
CLK	–	Serial Port Clock Input
C_{OUT}	–	Cascade Serial Port Output
V_{CC}	–	+5 Volt Supply Input
GND	–	Ground
NC	–	No Internal Connection
DNC	–	Do Not Connect

102794 1/11

OPERATION

The DS1867 contains two 256–position potentiometers whose wiper positions are set by an 8–bit value. These two 8–bit values are written to a 17–bit I/O shift register which is used to store wiper position and the stack select bit when the device is powered. An additional memory area, the shadow memory, stores the 17–bit I/O shift register during a power–down sequence which provides for wiper nonvolatility. A block diagram of the DS1867 is presented in Figure 1.

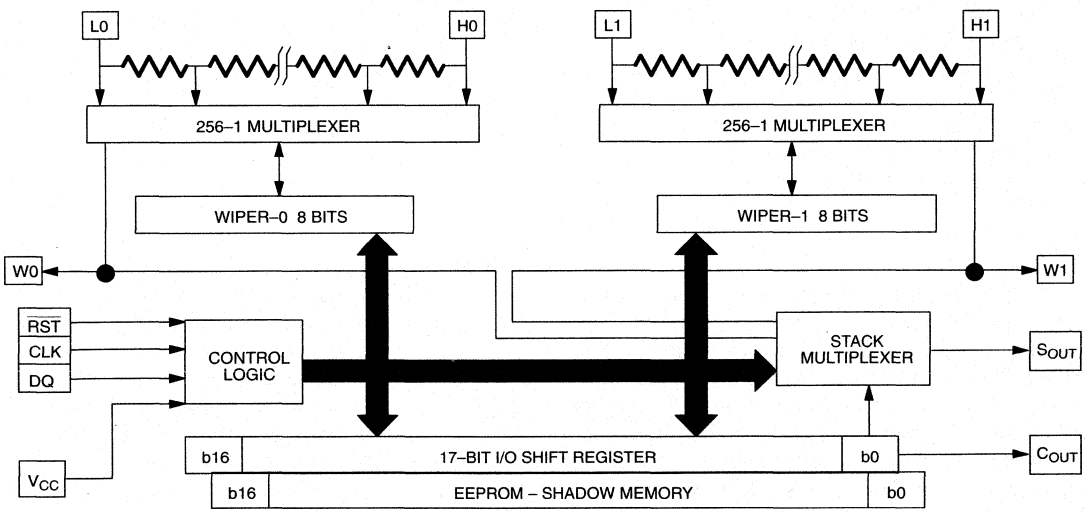
Communication and control of the DS1867 is accomplished through a 3–wire serial port interface that drives an internal control logic unit. The 3–wire serial interface consists of the three input signals: $\overline{RST}$, CLK, and DQ.

The $\overline{RST}$ control signal is used to enable 3–wire serial port operation of the device. The $\overline{RST}$ signal is an active high input and is required to begin any communication to the DS1867. The CLK signal input is used to provide timing synchronization for data input and output. The DQ signal line is used to transmit potentiometer wiper settings and the stack select bit configuration to the 17–bit I/O shift register of the DS1867.

Figure 2(a) presents the 3–wire serial port protocol. As shown, the 3–wire port is inactive when the $\overline{RST}$ signal input is low. Communication with the DS1867 requires the transition of the $\overline{RST}$ input from a low state to a high state. Once the 3–wire port has been activated, data is latched into the part on the low to high transition of the CLK signal input. Three–wire serial timing requirements are provided in the timing diagrams of Figure 2(b) and (c).

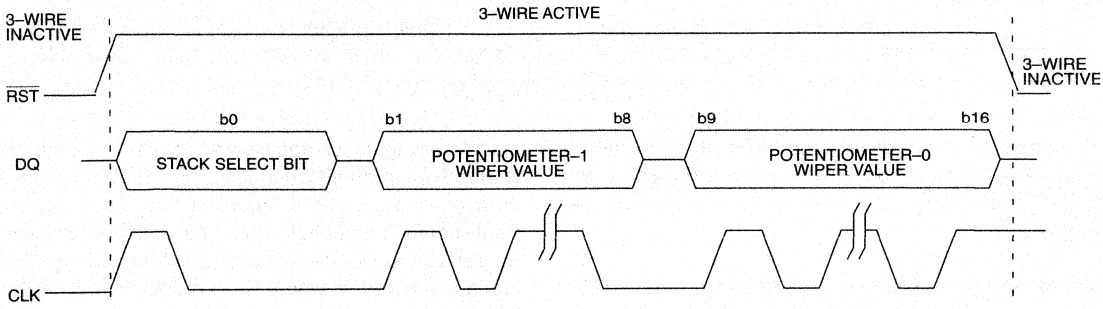
Data written to the DS1867 over the 3–wire serial interface is stored in the 17–bit I/O shift register (see Figure 3). The 17–bit I/O shift register contains both 8–bit potentiometer wiper position values and the stack select bit. The composition of the I/O shift register is presented in Figure 3. Bit 0 of the I/O shift register contains the stack select bit. This bit will be discussed in the section entitled Stacked Configuration. Bits 1 through 8 of the I/O shift register contain the potentiometer–1 wiper position value. Bit 1 will contain the MSB of the wiper setting for potentiometer–1 and bit 8 the LSB for the wiper setting. Bits 9 through 16 of the I/O shift register contain the value of the potentiometer–0 wiper position with the MSB for the wiper position occupying bit 9 and the LSB bit 16.

DS1867 BLOCK DIAGRAM Figure 1

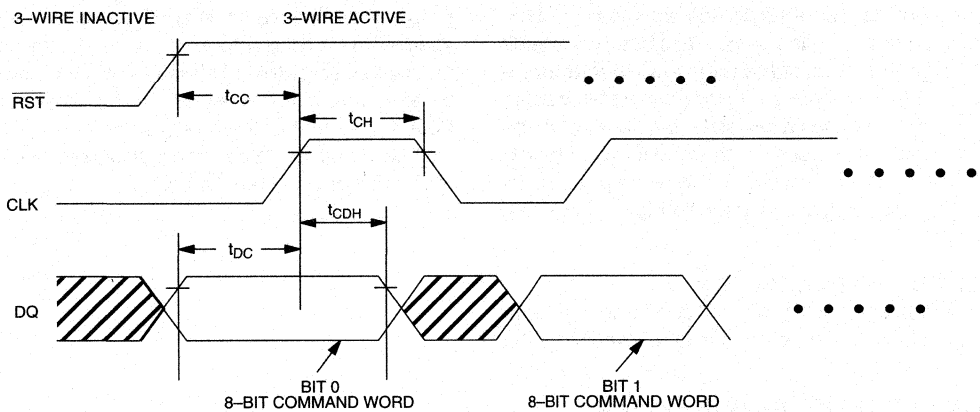


TIMING DIAGRAMS Figure 2

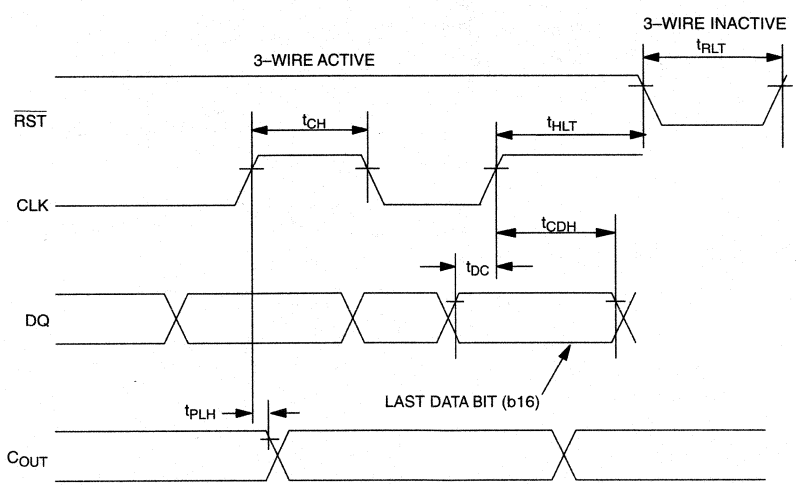
(a) 3–Wire Serial Interface General Overview



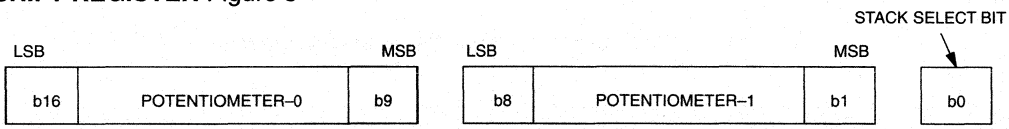
(b) Start of Communication Transaction



(c) End of Communication Transaction



I/O SHIFT REGISTER Figure 3



17–BIT I/O SHIFT REGISTER

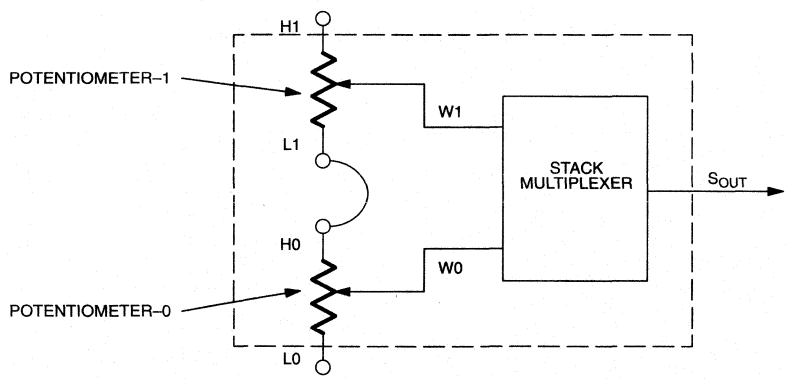
Transmission of data always begins with the stack select bit followed by the potentiometer–1 wiper position value and lastly the potentiometer–0 wiper position value (see Figure 2(a)).

When wiper position data is to be written to the DS1867, 17 bits (or some integer multiple) of data should always be transmitted. Transactions which do not send a complete 17 bits (or multiple) will leave the register incomplete and possibly an error in desired wiper position. After a communication transaction has been completed the $\overline{RST}$ signal input should be taken to a low state to prevent any inadvertent changes to the device shift register. Once $\overline{RST}$ has reached a low state, the contents of the I/O shift register are loaded into the respective multiplexers for setting wiper position. A new wiper position will only engage pending a $\overline{RST}$ transition to the low state.

STACKED CONFIGURATION

The potentiometers of the DS1867 can be connected in series as shown in Figure 4. This is referred to as the stacked configuration and allows the user to double the total end–to–end resistance of the part. The resolution of the combined potentiometers will remain the same as a single potentiometer but with a total of 512 wiper positions available. Device resolution is defined as $R_{TOT}/256$ (per potentiometer); where R_{TOT} is equal to the device resistance value. The wiper output for the combined stacked potentiometer will be taken at the Sout pin, which is the multiplexed output of the wiper of potentiometer–0 (W0) or potentiometer–1 (W1). The potentiometer wiper selected at the Sout output is governed by the setting of the stack select bit (bit–0) of the 17–bit I/O shift register. If the stack select bit has value 0, the multiplexed output , Sout, will be that of the potentiometer–0 wiper. If the stack select bit has value 1, the multiplexed output, Sout, will be that of the potentiometer–1 wiper.

STACKED CONFIGURATION Figure 4



CASCADE OPERATION

A feature of the DS1867 is the ability to control multiple devices from a single processor. Multiple DS1867s can be linked or daisy chained as shown in Figure 5. As a data bit is entered into the I/O shift register of the DS1867 it will appear at the Cout output after a maximum delay of 70 nanoseconds.

The Cout output of the DS1867 can be used to drive the DQ input of another DS1867. When connecting multiple devices, the total number of bits sent is always 17 times the number of DS1867s in the daisy chain.

An optional feedback resistor can be placed between the Cout terminal of the last device and the DQ input of the first DS1867, thus allowing the controlling processor to read, as well as, write data or circularly clock data through the daisy chain. The value of the feedback or isolation resistor should be in the range from 2K to 10K ohms.

When reading data via the Cout pin and isolation resistor, the DQ line is left floating by the reading device. When $\overline{RST}$ is driven high, bit 17 is present on the Cout pin, which is fed back to the input DQ pin through the isolation resistor. When the CLK input transitions low to high, bit 17 is loaded into the first position of the I/O shift register and bit 16 becomes present on Cout and DQ of the next device. After 17 bits (or 17 times the number of DS1867s in the daisy chain), the data has shifted completely around and back to its original position. When $\overline{RST}$ transitions to the low state to end data transfer, the value (the same as before the read occurred) is loaded into the wiper–0, wiper–1, and stack select bit I/O register.

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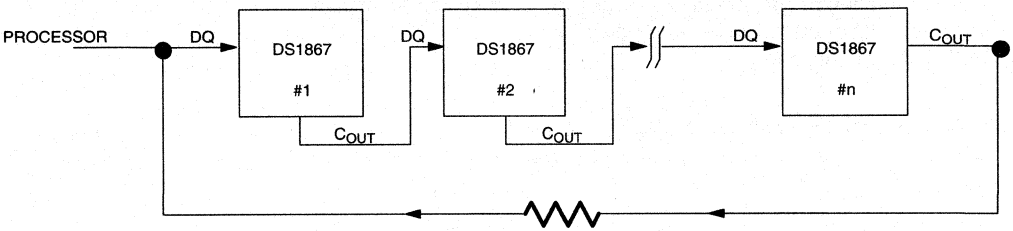
CASCADING MULTIPLE DEVICES Figure 5



OPTIONAL FEEDBACK RESISTOR
FOR READING DATA (2K TO 10K)

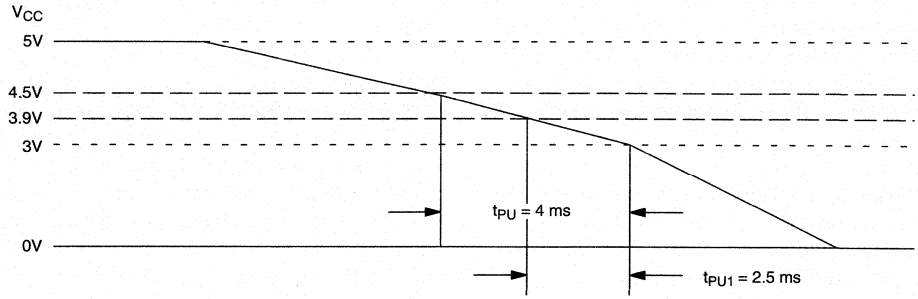
NONVOLATILE WIPER SETTINGS

The DS1867 maintains the position of the wiper in the absence of power. This feature is provided through the use of EEPROM type memory cell arrays. During normal operation, the position of the wiper is determined by the device multiplexers and stored in the shadow memory (EEPROM). The manner in which an update occurs has been optimized for reliability, durability, and performance. Additionally, the update operation is totally transparent to the user.

When power is applied to the DS1867, wiper settings will be the last recorded in the EEPROM memory cells or shadow memory before the last power–down. Changes to the EEPROM memory cells occur during a predefined power–down sequence. If the DS1867 detects a voltage transistion to 4.5 volts or less, on the power supply input, the part initiates an automatic wiper storage sequence. This storage sequence will save in EEPROM memory the contents of the I/O shift register before a total power–shutdown; provided specific power–down timing requirements are met. The minimum total power down time is specified at 4 milliseconds. Power–down timing requirements on V_{CC} are shown in Figure 6.

The EEPROM memory cells are specified to accept greater than 50,000 writes before a wear–out condition. If the EEPROM memory cells do reach a wear–out condition, the DS1867 will still function properly while power is applied. A minimum time of 4 ms between 4.5V and 3V is required to perform the proper position storage of the wiper.

POWER–DOWN EEPROM TIMING REQUIREMENTS Figure 6



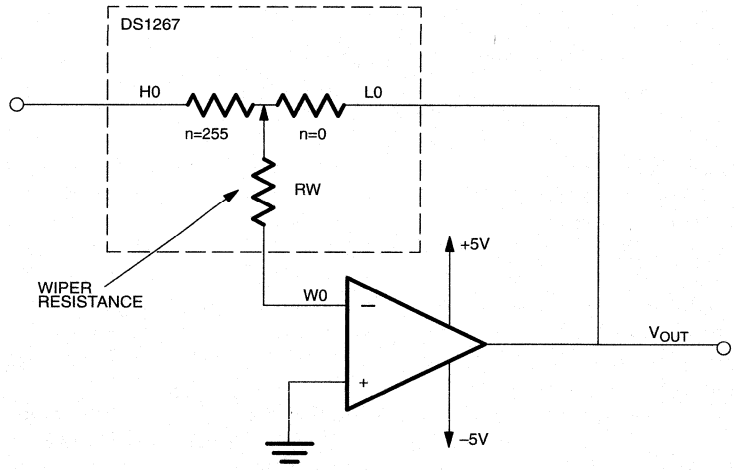
TYPICAL APPLICATION CONFIGURATIONS

Figures 7 and 8 show two typical application configurations for the DS1867. By connecting the wiper terminal of the part to a high impedance load, the effects of the wiper resistance is minimized, since the wiper resistance can vary from 400 to 1000 ohms depending on wiper voltage. Figure 7 presents the device connected in an inverting varible gain amplifier. The gain of the circuit on Figure 7 is given by the following equation:

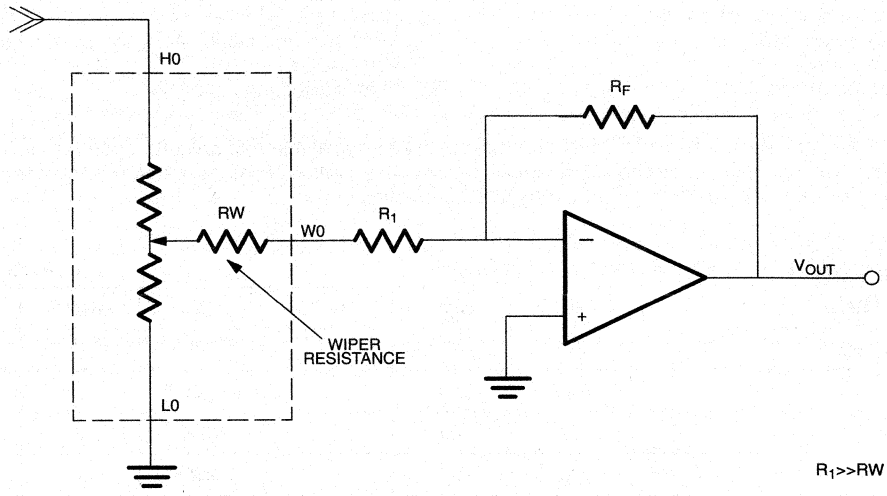
Av = –n/(255–n); where n = 0 to 255

Figure 8 shows the device operaing in a fixed gain attenuator where the potentiometer is used to attenuate an incoming signal. Note the resistance R1 is chosen to be much greater than the wiper resistance to minimize its effect on circuit gain.

INVERTING VARIABLE GAIN AMPLIFIER Figure 7



FIXED GAIN ATTENUATOR Figure 8



4

ABSOLUTE AND RELATIVE LINEARITY

Absolute linearity is defined as the difference between the actual measured output voltage and the expected output voltage. Figure 9 presents the test circuit used to measure absolute linearity. Absolute linearity is given in terms of a minimum increment or expected output when the wiper position is moved one position. In the case of the test circuit, a minimum increment (MI) would equal 10/512 volts. The equation for absolute linearity is given in equation (1).

Eq: (1) Absolute Linearity

$$AL = \{Vo(actual) - Vo(expected)\}/MI$$

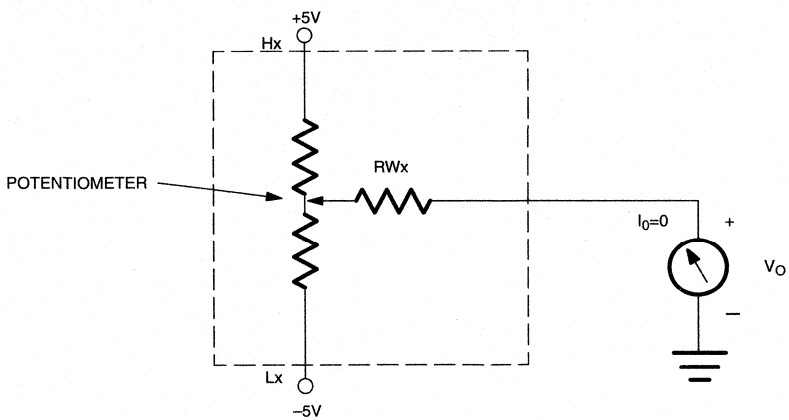
Relative Linearity is a measure of error between two adjacent wiper position points and is given in terms of MI by equation (2).

Eq: (2) Relative Linearity

$$RL = \{Vo(n+1) - Vo(n)\}/MI$$

Figure 10 is a plot of absolute linearity and relative linearity versus wiper position for the DS1867 at 25°C. The specification for absolute linearity of the DS1867 is ±0.75 MI typical. The specification for relative linearity of the DS1867 is ±0.30 MI typical.

LINEARITY MEASUREMENT CONFIGURATION Figure 9



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground (V_B=GND)	–1.0V to +5.5V
Voltage on Resistor Pins when V_B=–5.5V	–5.5V to +5.5V
Operating Temperature	0°C to 70°C commercial; –40°C to +85°C industrial
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(–40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5		5.5	V	
Input Logic 1	V_{IH}	2.0		V_{CC}+0.5	V	1
Input Logic 0	V_{IL}	–0.5		+0.8	V	1
Substrate Bias	V_B	–5.5		GND	V	
Resistor Inputs	L, H, W	V_B		V_{CC}+0.5	V	2

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}		250	900	µA	
Input Leakage	I_{LI}	–1		+1	µA	
Wiper Resistance	R_W		400	1000	Ω	
Wiper Current	I_W			1	mA	
Logic 1 Output @ 2.4 Volts	I_{OH}	–1.0			mA	8
Logic 0 Output @ 0.4 Volts	I_{OL}			4	mA	8
Standby Current	I_{STBY}		250		µA	
Power–Down Time	t_{PU} t_{PU1}	4 2.5			ms ms	9 10
Power Trip Point		3.9	4.2	4.5	V	
Recovery Time	t_{REC}	2	5	10	ms	11, 14

ANALOG RESISTOR CHARACTERISTICS

(–40°C to +85°C; V_{CC}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
End–to–End Resistor Tolerance		–20		+20	%	
Absolute Linearity			±0.75		LSB	4
Relative Linearity			±0.30		LSB	5
–3 dB Cutoff Frequency	f_{CUTOFF}				Hz	7
Noise Figure			120		dB/(Hz)1/2	
Temperature Coefficient			+800		ppm/°C	

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	3
Output Capacitance	C_{OUT}			7	pF	3

4

AC ELECTRICAL CHARACTERISTICS

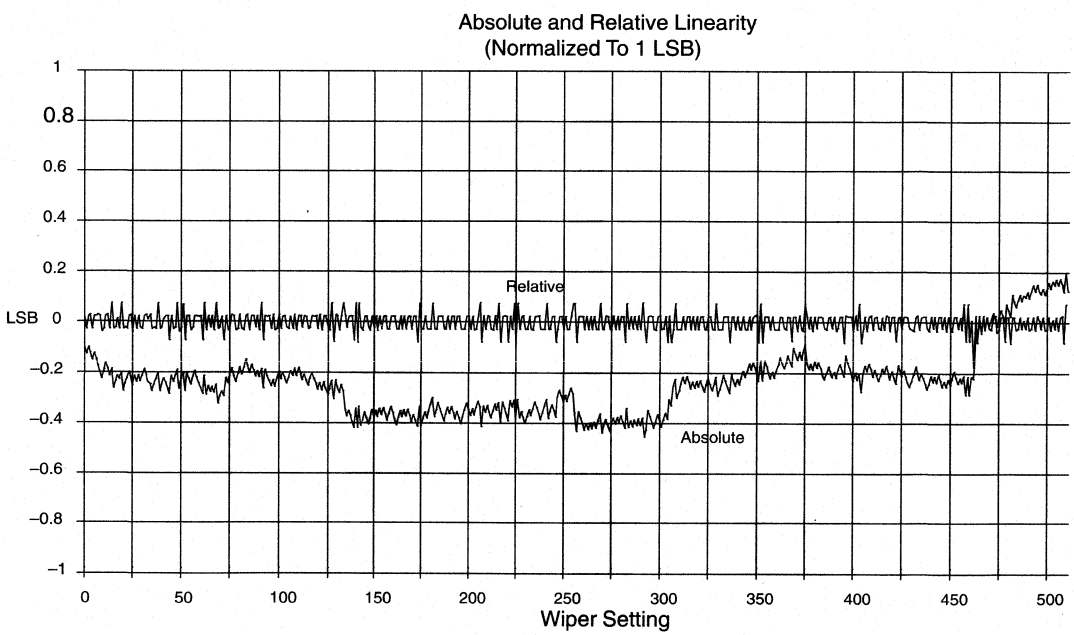
(–40°C to +85°C; V_{CC}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CLK Frequency	f_{CLK}	DC		10	MHz	15
Width of CLK Pulse	t_{CH}	50			ns	15
Data Setup Time	t_{DC}	30			ns	15
Data Hold Time	t_{CDH}	10			ns	15
Propagation Delay Time Low to High Level Clock to Output	t_{PLH}			70	ns	13, 15
Propagation Delay Time High to Low Level Clock to Output	t_{PHL}			70	ns	13, 15
$\overline{RST}$ High to Clock Input High	t_{CC}	50			ns	15
$\overline{RST}$ Low from Clock Input High	t_{HLT}	50			ns	15
CLK Rise Time	t_{CR}			50	ns	15
$\overline{RST}$ Inactive Time	t_{RLT}	200			ns	15

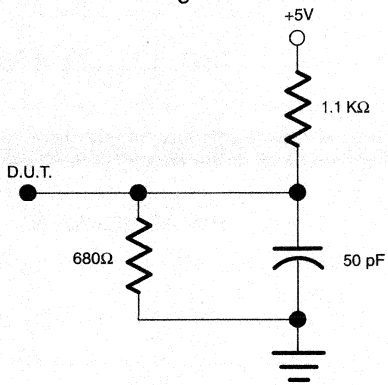
NOTES:

1. All voltages are referenced to ground.
2. Resistor inputs cannot exceed the substrate bias voltage, V_B, in the negative direction.
3. Capacitance values apply at 25°C.
4. Absolute linearity is used to determine wiper voltage versus expected voltage as determined by wiper position.
5. Relative linearity is used to determine the change in voltage between successive tap positions.
6. Typical values are for t_A=25°C and nominal supply voltage.
7. –3 dB cuttof frequency characteristics for the DS1867 depend on potentiometer total resistance: DS1867–010; 1 MHz, DS1867–050; 200 KHz, DS1867–100; 100 KHz.
8. C_{OUT} is active regardless of the state of $\overline{RST}$.
9. Power–down time is specified at a minimum of 4 ms. It is the time required for the DS1867 to guarantee wiper position storage as V_{CC} moves from 4.5V to 3.0V.
10. This is the time from power trip point min (3.9V) to 3.0V to guarantee wiper storage.
11. t_{REC} is the time required before the DS1867 stored wiper position becomes valid on power–up.
12. Power trip points reference required voltage necessary for DS1867 to restore the stored wiper position setting.
13. See Figure 11.
14. During power up the wiper position will be set at 80H.
15. See Figure 2.

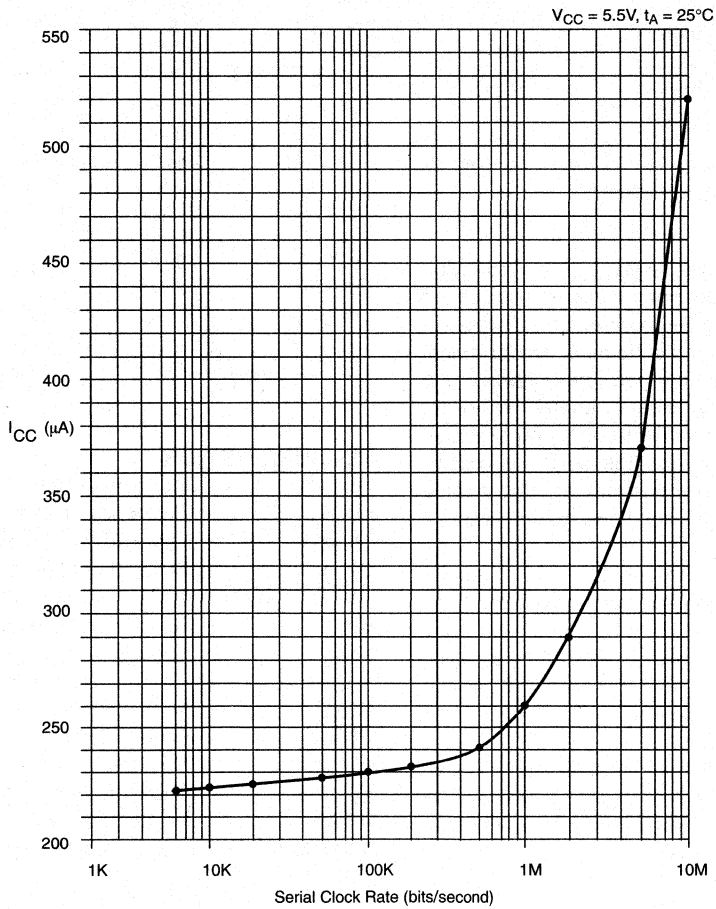
ABSOLUTE AND RELATIVE LINEARITY Figure 10



DIGITAL OUTPUT LOAD SCHEMATIC Figure 11



TYPICAL SUPPLY CURRENT VS. SERIAL CLOCK RATE Figure 12



PRELIMINARY

DALLAS SEMICONDUCTOR

DS1868
Dual Digital Potentiometer Chip

FEATURES

- Ultra–low power consumption, quiet, pumpless design
- Two digitally controlled, 256–position potentiometers
- Serial port provides means for setting and reading both potentiometers
- Resistors can be connected in series to provide increased total resistance
- 20–pin TSSOP package
- Resistive elements are temperature compensated to ±0.3 LSB relative linearity
- Standard resistance values:
  - DS1868–10 ~ 10KΩ
  - DS1868–50 ~ 50KΩ
  - DS1868–100 ~ 100KΩ
- +5V or ±3V operation
- Temperature range of 0°C to 70°C

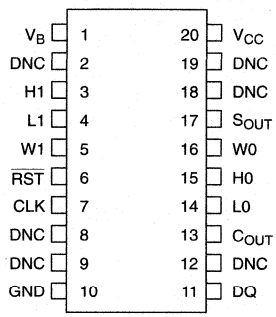
DESCRIPTION

The DS1868 consist of two digitally controlled solid–state potentiometers. Each potentiometer is composed of 256 resistive sections. Between each resistive section and both ends of the potentiometer are tap points which are accessible to the wiper. The position of the wiper on the resistive array is set by an 8–bit value that controls which tap point is connected to the wiper output. Communication and control of the device is accomplished via a 3–wire serial port interface. This interface allows the device wiper position to be read or written.

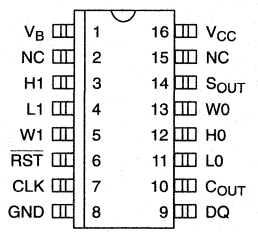
Both potentiometers can be connected in series (or stacked) for an increased total resistance with the same resolution. For multiple device–single processor environments, the DS1868 can be cascaded or daisy chained. This feature provides for control of multiple devices over a single 3–wire bus.

The DS1868 is offered in two standard resistance values which include 10K, 50K, and 100K ohm versions. The part is available in 16–pin SOIC (300 mil), 14–pin DIP, and 20–pin TSSOP packages.

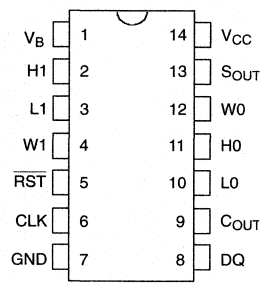
PIN ASSIGNMENT



20–Pin TSSOP (173 MIL)



DS1868S 16–Pin SOIC (300 MIL)
See Mech. Drawings Section



14–Pin DIP (300 MIL)
See Mech. Drawings Section

PIN DESCRIPTION

L0, L1	–	Low End of Resistor
H0, H1	–	High End of Resistor
W0, W1	–	Wiper Terminal of Resistor
S_{OUT}	–	Stacked Configuration Output
$\overline{RST}$	–	Serial Port Reset Input
DQ	–	Serial Port Data Input
CLK	–	Serial Port Clock Input
C_{OUT}	–	Cascade Port Output
V_{CC}	–	+5 Volt Supply
GND	–	Ground Connections
NC	–	No Internal Connection
V_B	–	Substrate Bias Voltage
DNC	–	Do Not Connect

*All GND pins must be connected to ground.

OPERATION

The DS1868 contains two 256–position potentiometers whose wiper positions are set by an 8–bit value. These two 8–bit values are written to a 17–bit I/O shift register which is used to store the two wiper positions and the stack select bit when the device is powered. A block diagram of the DS1868 is presented in Figure 1.

Communication and control of the DS1868 is accomplished through a 3–wire serial port interface that drives an internal control logic unit. The 3–wire serial interface consists of the three input signals: $\overline{RST}$, CLK, and DQ.

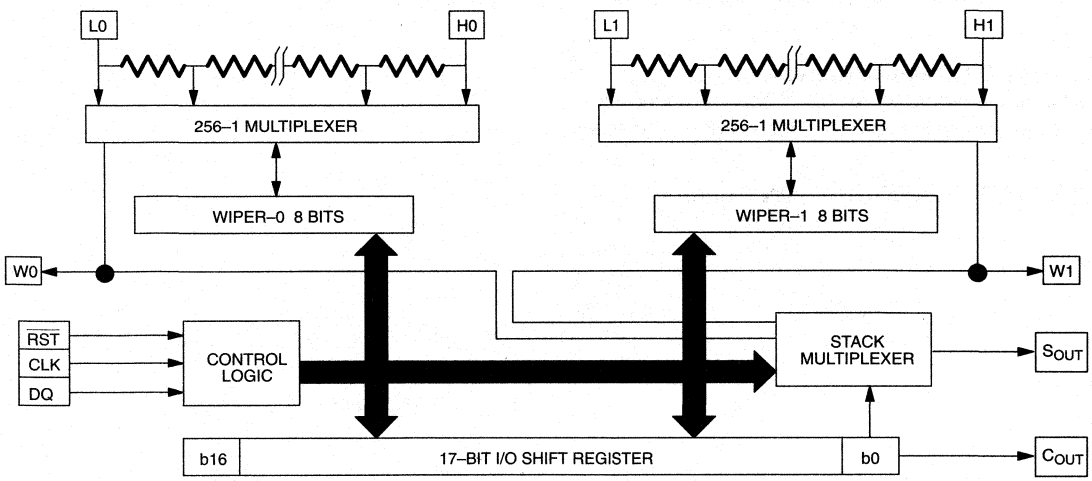
The $\overline{RST}$ control signal is used to enable the 3–wire serial port operation of the device. The $\overline{RST}$ signal is an active high input and is required to begin any communication to the DS1868. The CLK signal input is used to provide timing synchronization for data input and output. The DQ signal line is used to transmit potentiometer wiper settings and the stack select bit configuration to the 17–bit I/O shift register of the DS1868.

Figure 9(a) presents the 3–wire serial port protocol. As shown, the 3–wire port is inactive when the $\overline{RST}$ signal input is low. Communication with the DS1868 requires the transistion of the $\overline{RST}$ input from a low state to a high state. Once the 3–wire port has been activated, data is entered into the part on the low to high transistion of the CLK signal inputs. Three–wire serial timing requirements are provided in the timing diagrams of Figure 9(b),(c).

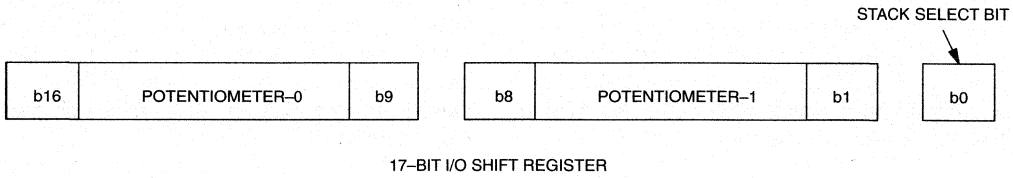
Data written to the DS1868 over the 3–wire serial interface is stored in the 17–bit I/O shift register (see Figure 2). The 17–bit I/O shift register contains both 8–bit potentiometer wiper position values and the stack select bit. The composition of the I/O shift register is presented in Figure 2. Bit 0 of the I/O shift register contains the stack select bit. This bit will be discussed in the section entitled Stacked Configuration. Bits 1 through 8 of the I/O shift register contain the potentiometer–1 wiper position value. Bit 1 will contain the MSB of the wiper setting for potentiometer–1 and bit 8 the LSB for the wiper setting. Bits 9 through 16 of the I/O shift register contain the value of the potentiometer–0 wiper position with the MSB for the wiper position occupying bit 9 and the LSB bit 16.

4

DS1868 BLOCK DIAGRAM Figure 1



I/O SHIFT REGISTER Figure 2



17–BIT I/O SHIFT REGISTER

Transmission of data always begins with the stack select bit followed by the potentiometer–1 wiper position value and lastly the potentiometer–0 wiper position value.

When wiper position data is to be written to the DS1868, 17 bits (or some integer multiple) of data should always be transmitted. Transactions which do not send a complete 17–bits (or multiple) will leave the register incomplete and possibly an error in the desired wiper positions.

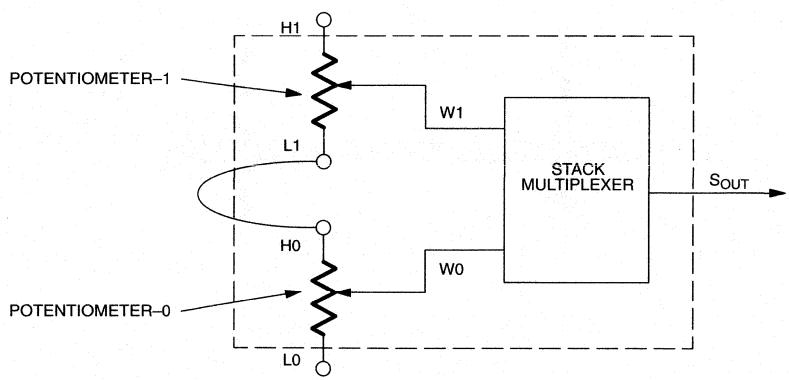
After a communication transaction has been completed the $\overline{RST}$ signal input should be taken to a low state to prevent any inadvertent changes to the device shift register. Once $\overline{RST}$ has reached a low state, the contents of the I/O shift register are loaded into the respective multiplexers for setting wiper position. A new wiper position will only engage after a $\overline{RST}$ transition to the inactive state. On device power–up, wiper position will be random.

STACKED CONFIGURATION

The potentiometers of the DS1868 can be connected in series as shown in Figure 3. This is referred to as the stacked configuration and allows the user to double the total end–to–end resistance of the part. The resolution of the combined potentiometers will remain the same as a single potentiometer but with a total of 512 wiper positions available. Device resolution is defined as $R_{TOT}/256$ (per potentiometer); where R_{TOT} equals the total potentiometer resistance.

The wiper output for the combined stacked potentiometer will be taken at the S_{OUT} pin, which is the multiplexed output of the wiper of potentiometer–0 (W0) or potentiometer–1 (W1). The potentiometer wiper selected at the S_{OUT} output is governed by the setting of the stack select bit (bit 0) of the 17–bit I/O shift register. If the stack select bit has value 0, the multiplexed output, S_{OUT}, will be that of the potentiometer–0 wiper. If the stack select bit has value 1, the multiplexed output, S_{OUT}, will be that of the potentiometer–1 wiper.

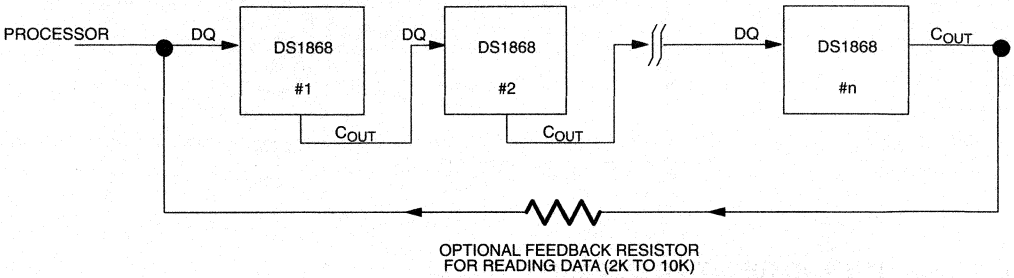
STACKED CONFIGURATION Figure 3



CASCADE OPERATION

A feature of the DS1868 is the ability to control multiple devices from a single processor. Multiple DS1868s can be linked or daisy chained as shown in Figure 4. As a data bit is entered into the I/O shift register of the DS1868 a bit will appear at the C_{OUT} output after a minimum delay of 50 nanoseconds. The stack select bit of the DS1868 will always be the first out the part at the beginning of a transaction. Additionally the C_{OUT} pin is always active regardless of the state of $\overline{RST}$. This allows one to read the I/O shift register without changing its value.

CASCADING MULTIPLE DEVICES Figure 4



The C_{OUT} output of the DS1868 can be used to drive the DQ input of another DS1868. When connecting multiple devices, the total number of bits transmitted is always 17 times the number of DS1868s in the daisy chain.

An optional feedback resistor can be placed between the C_{OUT} terminal of the last device and the first DS1868 DQ input thus allowing the controlling processor to read, as well as, write data, or circularly clock data through the daisy chain. The value of the feedback or isolation resistor should be in the range from 2K to 10K ohms.

When reading data via the C_{OUT} pin and isolation resistor, the DQ line is left floating by the reading device. When $\overline{RST}$ is driven high, bit 17 is present on the C_{OUT} pin, which is fed back to the input DQ pin through the isolation resistor. When the CLK input transitions low to high, bit 17 is loaded into the first position of the I/O shift register and bit 16 becomes present on C_{OUT} and DQ of the next device. After 17 bits (or 17 times the number of DS1868s in the daisy chain), the data has shifted completely around and back to its original position. When $\overline{RST}$ transitions to the low state to end data transfer, the value (the same as before the read occurred) is loaded into the wiper–0, wiper–1, and stack select bit I/O register.

ABSOLUTE AND RELATIVE LINEARITY

Absolute linearity is defined as the difference between the actual measured output voltage and the expected output voltage. Figure 5 presents the test circuit used to measure absolute linearity. Absolute linearity is given in terms of a minimum increment or expected output when the wiper is moved one position. In the case of the test circuit, a minimum increment (MI) or one LSB would equal 10/512 volts. The equation for absolute linearity is given as follows:

(1) ABSOLUTE LINEARITY

$$AL=\{V_O(actual) - V_O(expected)\}/MI$$

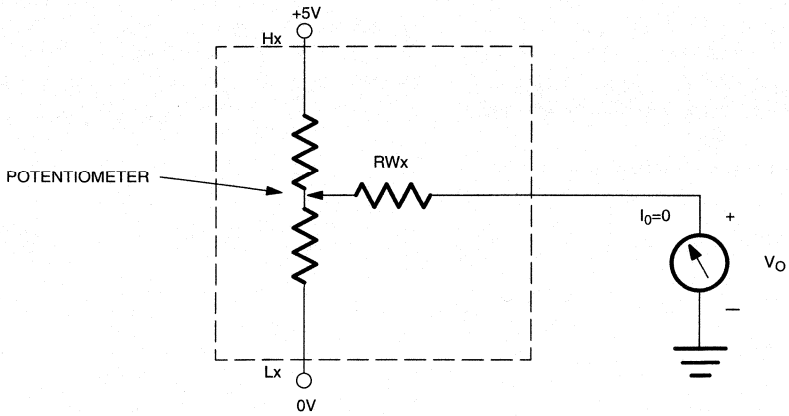
Relative Linearity is a measure of error between two adjacent wiper position points and is given in terms of MI by equation (2).

(2) RELATIVE LINEARITY

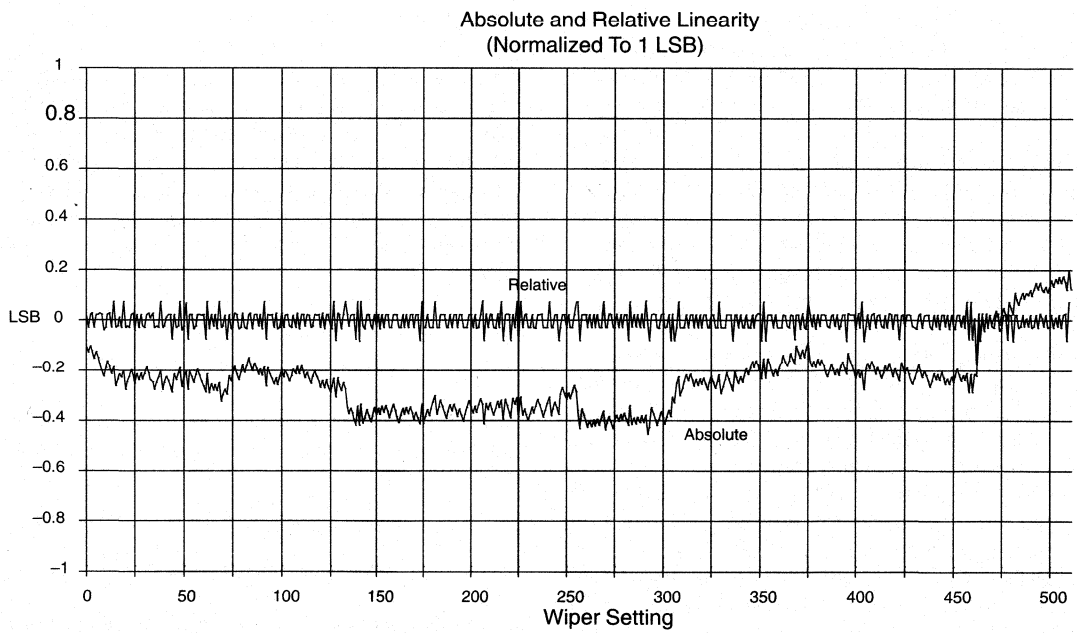
$$RL=\{V_O(n+1) - V_O(n)\}/MI$$

Figure 6 is a plot of absolute linearity and relative linearity versus wiper position for the DS1868 at 25°C. The specification for absolute linearity of the DS1868 is ±0.75 MI typical. The specification for relative linearity of the DS1868 is ±0.3 MI typical.

LINEARITY MEASUREMENT CONFIGURATION Figure 5



DS1868 ABSOLUTE AND RELATIVE LINEARITY Figure 6



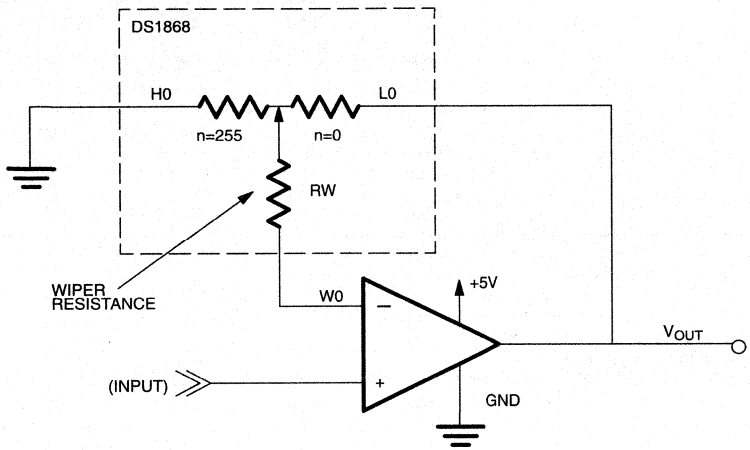
TYPICAL APPLICATION CONFIGURATIONS

Figures 7 and 8 show two typical application configurations for the DS1868. By connecting the wiper terminal of the part to a high impedance load, the effects of the wiper resistance is minimized, since the wiper resistance can vary from 400 to 1000 ohms depending on wiper voltage. Figure 7 presents the device connected in a varible gain amplifier. The gain of the circuit on Figure 7 is given by the following equation:

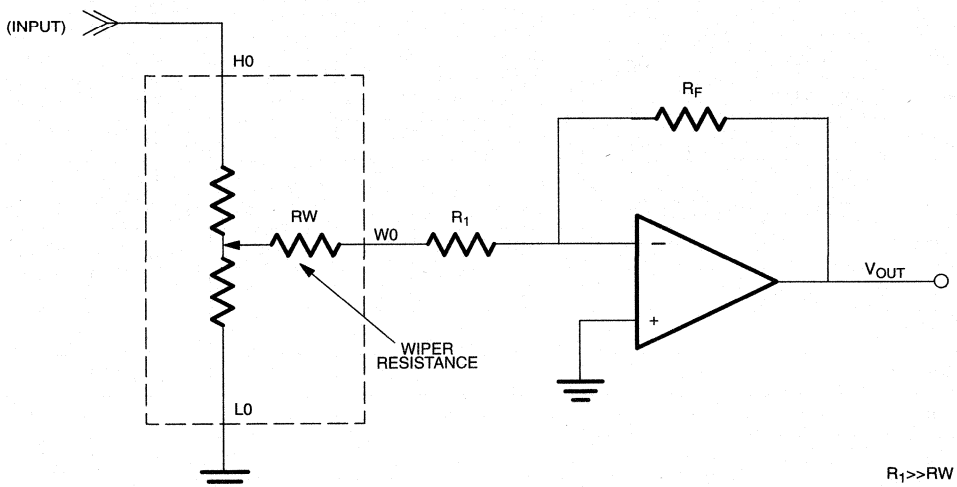
$$A_V = \frac{+256}{N+1} \quad \text{where } N = 0 \text{ to } 255$$

Figure 8 shows the device operating in a fixed gain attenuator where the potentiometer is used to attenuate an incoming signal. Note the resistance R1 is chosen to be much greater than the wiper resistance to minimize its effect on circuit gain.

VARIABLE GAIN AMPLIFIER Figure 7



FIXED GAIN ATTENUATOR Figure 8



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground (V_B=GND)	–1.0V to +7.0V
Voltage on Any Pin when V_B=–3.3V	–3.3V to +4.7V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C; V_{CC}=5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5 2.7		5.5 3.3	V	1 15
Input Logic 1	V_{IH}	2.0		V_{CC}+0.5	V	1, 2
Input Logic 0	V_{IL}	–0.5		+0.8	V	1, 2
Ground	GND	GND		GND	V	1
Resistor Inputs	L, H, W	V_B–0.5		V_{CC}+0.5	V	2, 15
Substrate Bias	V_B	–3.3		GND	V	1, 15

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}			400	µA	12
Input Leakage	I_{LI}	–1		+1	µA	
Wiper Resistance	R_W		400	1000	Ω	
Wiper Current	I_W			1	mA	
Logic 1 Output @ 2.4 Volts	I_{OH}	–1			mA	8, 9
Logic 0 Output @ 0.4 Volts	I_{OL}			4	mA	8, 9
Standby Current	I_{STBY}			1	µA	14

ANALOG RESISTOR CHARACTERISTICS

(0°C to 70°C; V_{CC}=5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
End–to–End Resistor Tolerance		–20		+20	%	
Absolute Linearity			±0.75		LSB	4
Relative Linearity			±0.3		LSB	5
–3 dB Cutoff Frequency	F_{CUTOFF}				Hz	7
Noise Figure						11
Temperature Coefficient			±800		ppm/C	

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	3, 6
Output Capacitance	C_{OUT}			7	pF	3, 6

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CLK Frequency	f_{CLK}	DC		10	MHz	10
Width of CLK Pulse	t_{CH}	50			ns	10
Data Setup Time	t_{DC}	30			ns	10
Data Hold Time	t_{CDH}	10			ns	10
Propagation Delay Time Low to High Level Clock to Output	t_{PLH}			50	ns	10, 13
Propagation Delay Time High to Low Level	t_{PLH}			50	ns	10, 13
$\overline{RST}$ High to Clock Input High	t_{CC}	50			ns	10
$\overline{RST}$ Low from Clock Input High	t_{HLT}	50			ns	10
$\overline{RST}$ Inactive	t_{RLT}	125			ns	10
Clock Low to Data Valid on a Read	t_{CDD}			30	ns	10
CLK Rise Time, CLK Fall Time	t_{CR}			50	ns	10

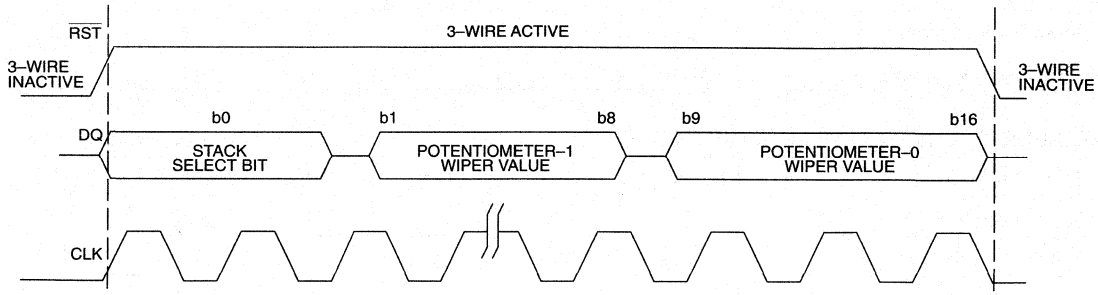
4

NOTES:

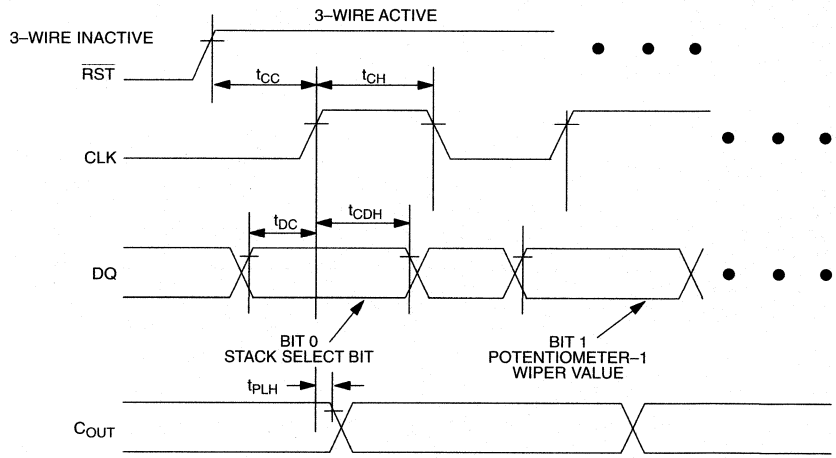
1. All voltages are referenced to ground.
2. Resistor inputs cannot exceed V_B – 0.5V in the negative direction.
3. Capacitance values apply at 25°C.
4. Absolute linearity is used to determine wiper voltage versus expected voltage as determined by wiper position. Device test limits ±1.6 LSB.
5. Relative linearity is used to determined the change in voltage between successive tap positions. Device test limits ±0.5 LSB.
6. Typical values are for t_A = 25°C and nominal supply voltage.
7. –3 dB cutoff frequency characteristics for the DS1868 depend on potentiometer total resistance: DS1868–010; 1 MHz, DS1868–050; 200 KHz; and DS1868–100; 80 KHz.
8. Cout is active regardless of the state of $\overline{RST}$.
9. V_{REF}= 1.5 volts .
10. See Figure 9(a), (b), and (c).
11. Noise < –120 dB/$\sqrt{Hz}$. Reference 1 volt (thermal).
12. Supply current is dependent on clock rate (see Figure 11).
13. See Figure 10.
14. Maximum standby current at 50°C is specified at 50 µA.
15. When biasing the substrate minimum V_B = –3.0V ± 10% and maximum V_{CC} = 3.0V ± 10%.

TIMING DIAGRAMS Figure 9

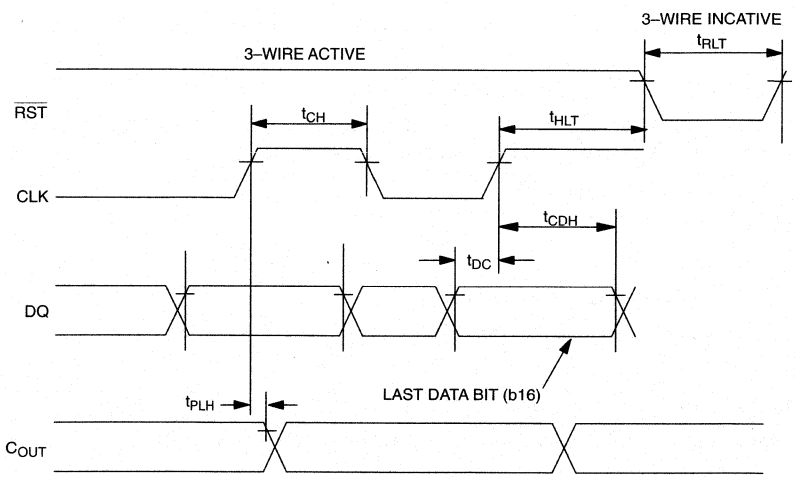
(a) 3–Wire Serial Interface General Overview



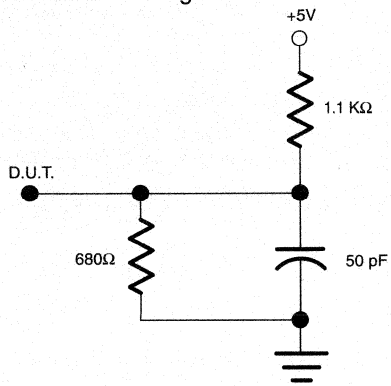
(b) Start of Communication Transaction



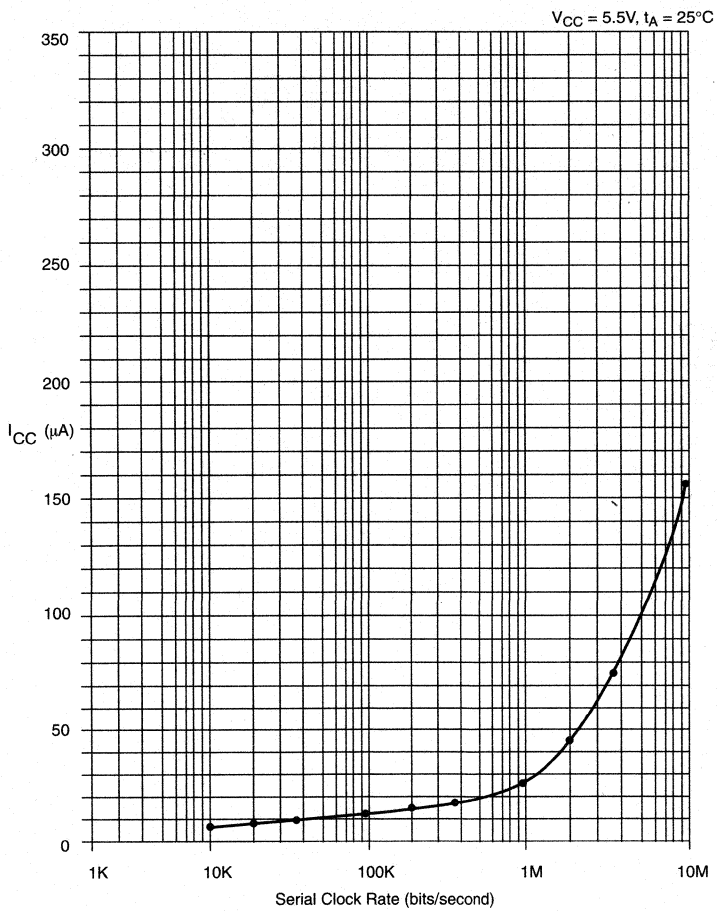
(c) End of Communication Transaction



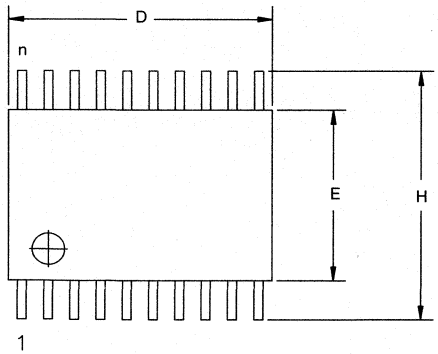
DIGITAL OUTPUT LOAD SCHEMATIC Figure 10

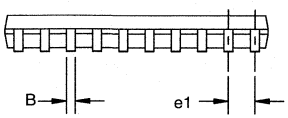


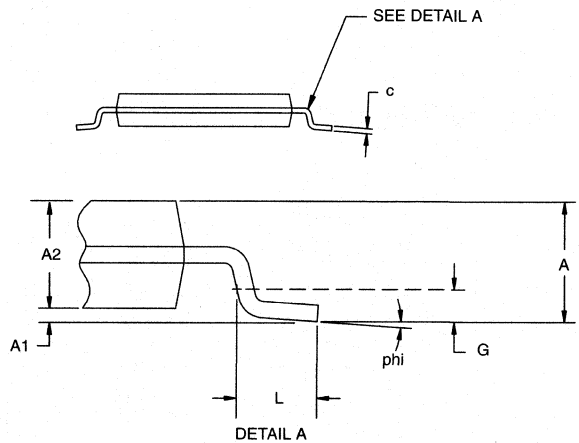
TYPICAL SUPPLY CURRENT VS. SERIAL CLOCK RATE Figure 11



DS1868 20-PIN TSSOP







DIM	MIN	MAX
A MM	–	1.10
A1 MM	0.05	–
A2 MM	0.75	1.05
C MM	0.09	0.18
L MM	0.50	0.70
e1 MM	0.65 BSC	
B MM	0.18	0.30
D MM	6.40	6.90
E MM	4.40 NOM	
G MM	0.25 REF	
H MM	6.25	6.55
phi	0°	8°

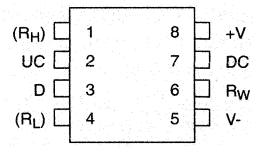
DALLAS SEMICONDUCTOR

DS1869
3V Dallastat™ Electronic Digital Rheostat

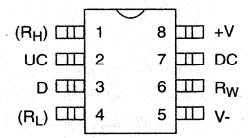
FEATURES

- Replaces mechanical variable resistors
- Operates from 3V or 5V supplies
- Electronic interface provided for digital as well as manual control
- Wiper position is maintained in the absence of power
- Low cost alternative to mechanical controls
- Applications include volume, tone, contrast, brightness, and dimmer control
- 8–pin SOIC and 8–pin DIP packages for DS1869
- Standard resistance values for Dallastat
  - DS1869–10 ~ 10KΩ
  - DS1869–50 ~ 50KΩ
  - DS1869–100 ~ 100KΩ
- Operating Temperature Range
  - Commercial: 20°C to 70°C
- 3V to 8V differential supplies operational range

PIN ASSIGNMENT



8-Pin DIP (300 Mil)
See Mech. Drawings Section



8-Pin SOIC (208 Mil)
See Mech. Drawings Section

PIN DESCRIPTION

R_H	-	Resistor High End (Option)
R_W	-	Resistor Wiper
R_L	-	Resistor Low End
-V, +V	-	Voltage Inputs
UC	-	Up Contact Input
D	-	Digital Input
DC	-	Down Contact Input

DESCRIPTION

The DS1869 Dallastat is a digital rheostat or potentiometer. This device provides 64 possible uniform tap points over the resistive range and is available in standard versions of 10K, 50K, and 100K ohms. The Dallastats can be controlled by either a mechanical–type contact closure input or a digital source input such as a CPU, and the DS1869 operates from 3V or 5V supplies. Wiper position is maintained in the absence of power which is accomplished through the use of a EEPROM memory cell array. The EEPROM cell array is specified to accept greater than 50,000 writes.

The DS1869 is offered in two standard IC packages which include an 8–pin 300 mil DIP and an 8–pin 200 mil SOIC. The DS1869 can be configured to operate using a single pushbutton, dual pushbutton or digital source input. This is illustrated in Figure 1. The DS1869 pinouts allow access to both ends of the potentiometer RL, RH, and the wiper, RW. Control inputs include the digital source input, D, the up contact input, UC, and the down contact input, DC. Other pins include the positive,+V, and negative, –V , supply inputs. The DS1869 is available in commercial temperature versions.

OPERATION

The DS1869 can be configured to operate from a single contact closure, dual contact closure inputs or driven using a digital source input. Figures 1 and 2 illustrate both configurations, respectively. Contact closure is defined as the transition from a high level to a low level on the up contact (UC), down contact (DC), or digital source (D) inputs. These inputs are inactive when in the high state.

The DS1869 interprets input pulse widths as the means of controlling wiper movement. A single pulse input over the UC, DC, or D input terminals will cause the wiper position to move 1/64th of the total resistance. A transition from a high to low on these inputs is considered the beginning of pulse activity or contact closure. A single pulse is defined as being greater than 1 ms but lasting no longer than 1 second. This is shown is Figures 3, 4, and 5 (a).

Repetitive pulsed inputs can be used to step through each resistive position of the device in a relatively fast manner (see Figure 5b). The requirement for repetitive pulsed inputs is that pulses must be separated by a minimum time of 1 ms. If not, the DS1869 will interpret repetitive pulses as a single pulse.

Pulse inputs lasting longer 1 second will cause the wiper to move one position every 100 ms following the initial 1 second hold time. The total time to transcend the entire potentiometer using a continuous input pulse is given by the formula below:

$$\approx 1 \text{ second} + 63 \times 100 \text{ ms} = 7.3 \text{ (seconds)}$$

Single contact closure operation allows the user to control wiper movement in either direction from a single push–button input. Figure 1 presents a typical single push–button configuration. The UC input is used to increment and decrement wiper position for single push–button mode of operation. The DC input provides no functionality in this mode but must be connected to the positive supply voltage (V_{CC}). The digital source input (D) can be allowed to float.

On device power–up, the configuration shown in Figure 1 must exist in order to enter the single contact closure mode of operation; especially and specifically, the (DC) input's connection to the positive supply voltage (V_{CC}) .

The direction of wiper movement, in single push–button operation, is determined by prior activity; with the direction of wiper movement being opposite to that of the previous activity.

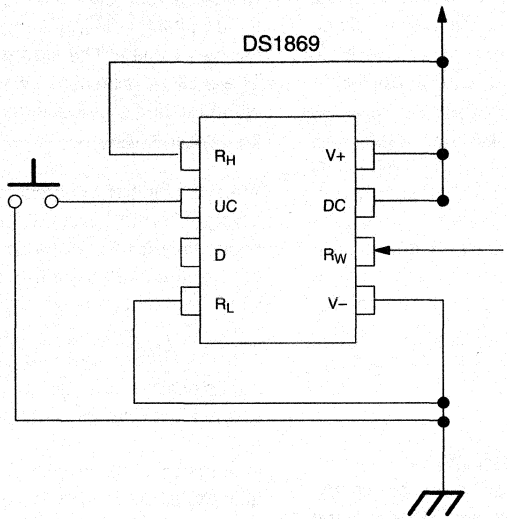
Changing the direction of wiper movement in single push–button mode is accomplish by a period of inactivity on the UC input of a (minimum) 1 second or greater. Also, in single push–button mode, as the wiper reaches the end of the potentiometer range its direction of movement reverses. This will occur, regardless, if the input is a continuous pulse, a sequence of repetitive pulses or a single pulse.

Dual push–button mode of operation is accomplished when the DC input is floated on power–up. If interfacing contact closure control inputs to digital logic, the DC input must be interfaced to an open drain drive which is high impedance during power–up. This will prevent the device from entering a single push–button mode of operation.

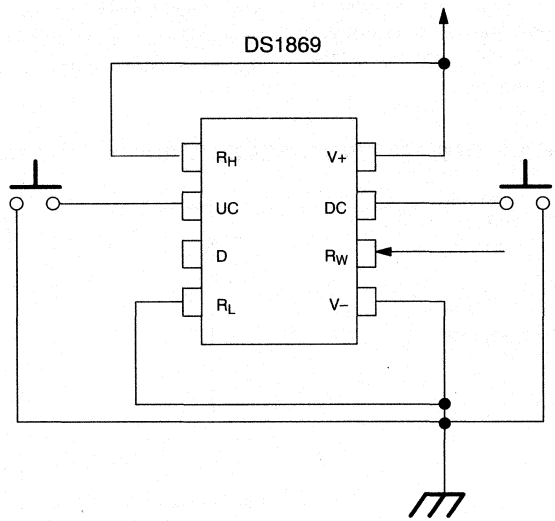
In dual push–button mode, each direction is controlled by the up contact (UC) and down contact (DC) inputs, respectively. No wait states are required to change wiper direction in dual push–button mode. In dual push–button mode, as the wiper position reaches the end of the potentiometer, the direction of wiper movement will not change. Wiper position will remain at the potentiometers' end until an opposite direction input is given.

All contact closure control inputs, UC, DC, and D are internally pulled–up by a 100K ohm resistance. The UC and DC inputs are internally debounced and require no external components for input signal conditioning.

DS1869 SINGLE PUSHBUTTON CONFIGURATION (TYPICAL EXAMPLE) Figure 1



DS1869 DUAL PUSHBUTTON CONFIGURATION (TYPICAL EXAMPLE) Figure 2



The DS1869 is provided with two supply inputs –V and +V. The maximum voltage difference between the two supply inputs is + 8.0 volts while the minimum voltage difference is 2.7 volts. All input levels are referenced to the negative supply input, –V. The voltage applied to any Dallastat terminal must not exceed the negative supply voltage (–V) by –0.5 or the positive supply voltage (+V) by + 0.5 volts. The minimum logic high level must be +2.4 volts with reference to the –V supply voltage input for +V=5V. A logic low level with reference to the –V supply voltage has a maximum value of +0.8 volts. Dallastats exhibit a typical wiper resistance of 400 ohms with a maximum wiper resistance of 1000 ohms. The maximum wiper current allowed through the Dallastat is specified at 1 milliamps (see DC Electrical Characteristics).

NONVOLATILE WIPER SETTINGS

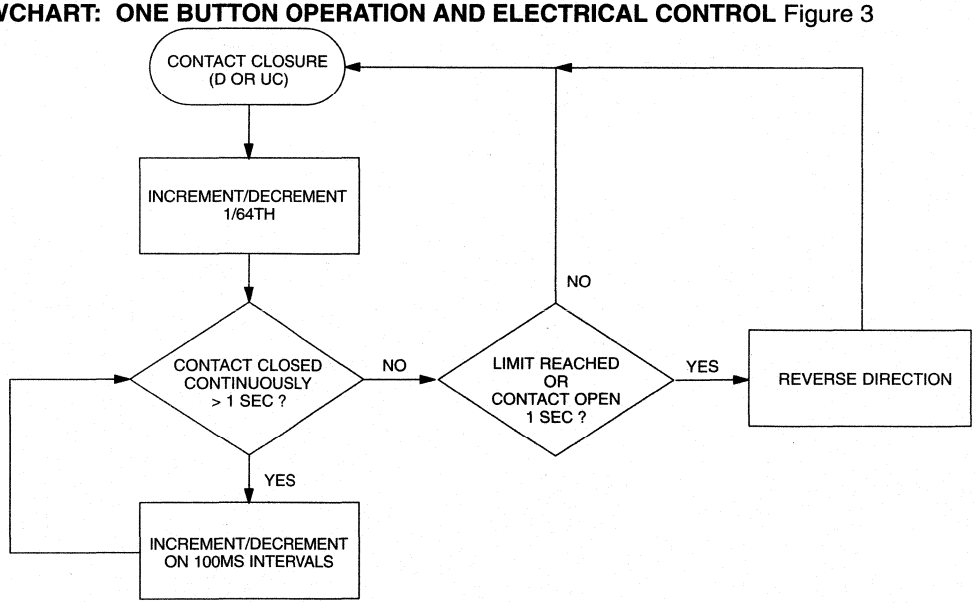
Dallastats maintain the position of the wiper in the absence of power. This feature is provided through the use of EEPROM type memory cell arrays. During normal operation the position of the wiper is determined by the input multiplexer. Periodically, the multiplexer will update the EEPROM memory cells. The manner in which an update occurs has been optimized for reliability, durability, and performance. Additionally, the update operation is totally transparent to the user.

When power is applied to the Dallastat, the wiper setting will be the last recorded in the EEPROM memory cells. If the Dallastat setting is changed after power is applied, the new value will be stored after a delay of 2 seconds. The initial storage of a new value after power–up occurs when the first change is made, regardless of when this change is made.

After the initial change on power–up, subsequent changes in the Dallastat EEPROM memory cells will occur only if the wiper position of the part is moved greater than 12.5% of the total resistance range. Any wiper movement after initial power–up which is less than 12.5% will not be recorded in the EEPROM memory cells. Since the Dallastat contains a 64–to–1 multiplexer, a change of greater than 12.5% corresponds to a change of the fourth LSB.

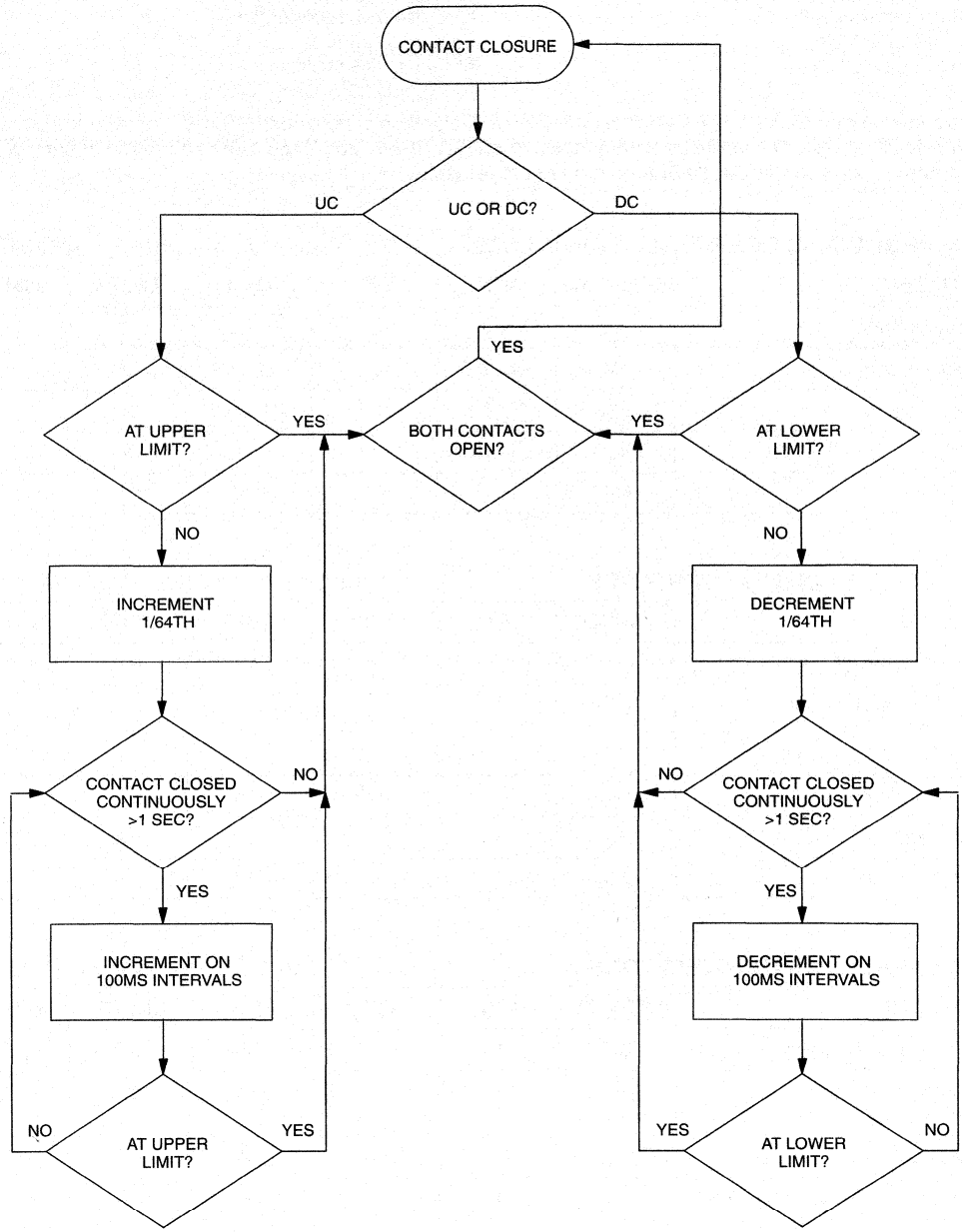
Changes or storage to the EEPROM memory cells must allow for a 2 second delay to guarantee that updates will occur. The EEPROM memory cells are specified to accept greater that 50,000 writes before a wear–out condition. If the EEPROM memory cells do reach a wear–out condition, the Dallastat will still function properly while power is applied. However, on power–up the device's wiper position will be that of the position last recorded before memory cell wear out.

FLOWCHART: ONE BUTTON OPERATION AND ELECTRICAL CONTROL Figure 3



CONTACT OPEN AND CONTACT CLOSURE TIMING IS 1 second ± 15%

FLOWCHART: TWO BUTTON OPERATION Figure 4



CONTACT OPEN AND CONTACT CLOSURE TIMING IS 1 second ± 15%

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to -V	-V –0.5V + 8.0V
Operating Temperature	-20°C to 70°C commercial
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
+ Supply Voltage	+V	-V + 2.7		-V + 8.0	V	
- Supply Voltage	-V	+V - 8.0		+V - 2.7	V	
Rheostat Inputs	R_H,R_W,R_L	-V - 0.5		+V + 0.5	V	
Logic Input 1	V_{IH}	+2.4			V	1, 2, 10
Logic Input 0	V_{IL}			+0.8	V	1, 2, 10

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; -V to +V = 2.7V to 8.0V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
+, - Supply Current	I_{CC1}		1	2	mA	3
Supply Current, Idle State At 3.3V At 8.0V	I_{CC2}			 2 10	µA	9
Wiper Resistance	R_W		400	1000	Ω	
Wiper Current	I_W			1	mA	5
Rheostat Current	I_H, I_L			1	mA	5

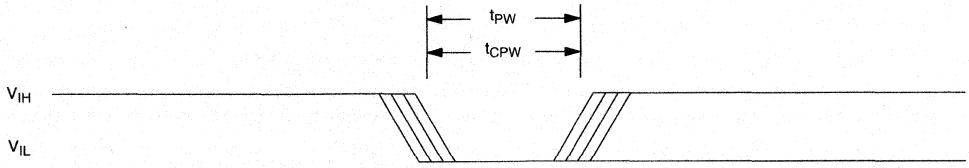
AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; -V to+V = 2.7V to 8.0V)

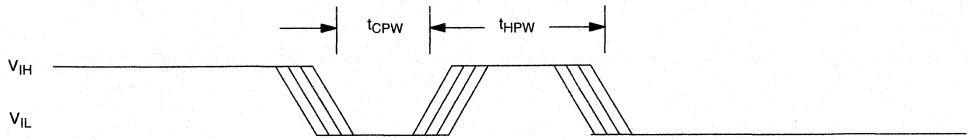
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width (D–input)	t_{PW}	1		DC	µs	1, 7, 8
Contact Pulse Width (UC, DC inputs)	t_{CPW}	1		DC	ms	1, 7, 8
Capacitance	C_{IN}		5	10	pF	6
Repetitive Input Pulse High Time	t_{HPW}	1		DC	ms	1, 7, 8
Continuous Input Pulse	t_{CCP}	1		DC	s	1, 7, 8

TIMING DIAGRAMS Figure 5

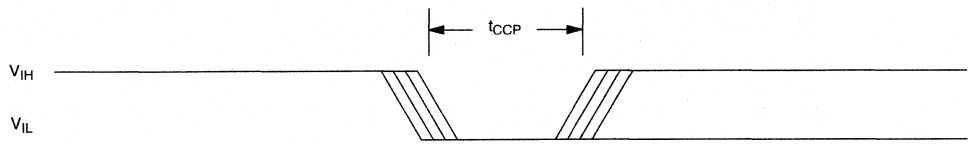
(A) SINGLE PULSE INPUTS



(B) REPETITIVE PULSE INPUTS



(C) CONTINUOUS PULSE INPUTS



NOTES:

1. All inputs; UC, DC, and D are internally pulled up with a resistance of 100KΩ.
2. Input logic levels are referenced to -V.
3. I_{CC} is the internal current that flows between -V and +V.
4. Input leakage applies to contact inputs UC and DC and digital input (D).
5. Wiper current and rheostat currents are the maximum current which can flow in the resistive elements.
6. Capacitance values apply at 25°C.
7. Input pulse width is the minimum time required for an input to cause an increment or decrement. If the UC, DC or D input is held active for longer than 1 second, subsequent increments or decrements will occur on 100 ms intervals until the inputs UC, DC, and/or D is released to V_{IH}.
8. Repetitive pulsed inputs on UC, DC, or D will be recognized as long as the pulse repetition occurs within 1 second of each other. Pulses occurring faster than 1 ms apart may not be recognized as individual inputs but can be interpreted a constant input. Tolerances for pulse timing ±15% on minimum inputs.
9. Idle state supply current is measured with no pushbutton pressed and with the wiper R_W tied to a CMOS load.
10. For +V referenced to –V=5V.

LINE INTERFACE

5

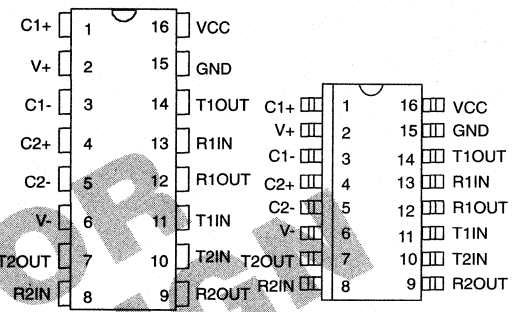
DALLAS SEMICONDUCTOR

DS1228
+5V Powered Dual RS-232 Transmitter/Receiver

FEATURES

- Operates from a single 5V power supply
- Two drivers and two receivers
- Meets all EIA RS-232-C specifications
- On-board voltage doubler
- On-board voltage inverter
- ± 30V input levels
- ± 9V output levels with + 5V supply
- Low-power CMOS
- Pin-compatible with the MAX 232
- Optional 16-pin SOIC surface mount package

PIN ASSIGNMENT



16-Pin DIP (300 MIL) See Mech. Drawings Section

16-Pin SOIC (300 MIL) See Mech. Drawings Section

PIN DESCRIPTION

C1+, C1	–	Capacitor 1 Connections
C2+, C2	–	Capacitor 2 Connections
V+, V-	–	± 10 Volts
T1IN, T2IN	–	Transmitter In
T1OUT, T2OUT	–	Transmitter Out
R1IN, R2IN	–	Receiver In
R1OUT, R2OUT	–	Receiver Out
V_{CC}	–	+5 Volts
GND	–	Ground

DESCRIPTION

The DS1228 is a dual RS-232-C Receiver/Transmitter that meets all EIA specifications while operating from a single, +5 volt supply. The DS1228 has two internal charge pumps. One of the charge pumps is used to generate +10 volts. The other is used to generate -10 volts. The DS1228 also contains four level translators. Two of the level translators are RS-232 transmitters which convert TTL/CMOS inputs into ±9V RS-232 outputs. The other two level translators are capable of operating with up to ±30V inputs. The DS1228 is suitable for all RS-232 communications and is particularly valuable where higher voltage power supplies for RS-232 drivers are not available. The power supply section of the DS1228 supplies ±10 volts from the V_{CC} input.

See the DS1229 data sheet for electrical specifications and operation.

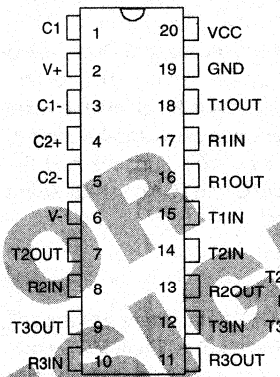
DALLAS SEMICONDUCTOR

DS1229
+5V Powered Triple RS-232 Transmitter/Receiver

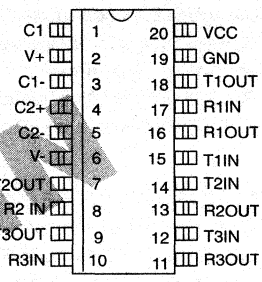
FEATURES

- Operates from a single 5V power supply
- Three drivers and three receivers
- Meets all EIA RS–232–C specifications
- Onboard voltage doubler
- Onboard voltage inverter
- ±30V input levels
- ±9V output levels with ±5V supply
- Low-power CMOS
- Optional 20-Pin SOIC surface mount package

PIN ASSIGNMENT



20-Pin DIP (300 MIL)
See Mech. Drawings Section



20-Pin SOIC (300 MIL)
See Mech. Drawings Section

PIN DESCRIPTION

C1+, C1-	Capacitor 1 Connections
C2+, C2-	Capacitor 2 Connections
V+, V-	±10 Volts
T1IN, T2IN, T3IN	Transmitter In
T1OUT, T2OUT, T3OUT	Transmitter Out
R1IN, R2IN, R3IN	Receiver In
R1OUT, R2OUT, R3OUT	Receiver Out
V_{CC}	+5 Volts
GND	Ground

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DESCRIPTION

The DS1229 is a triple RS–232–C receiver/transmitter that meets all EIA specifications while operating from a single +5V supply. The DS1229 has two internal charge pumps which are used to generate ±10V. The DS1229 also contains six level translators, three of which are RS–232 transmitters that convert TTL/CMOS inputs into +9V RS-232 outputs. The other three level translators are RS–232 receivers that convert RS–232 inputs to 5V TTL/CMOS outputs. These receivers are capable of operating with up to ±30V inputs. The DS1229 is suitable for all RS–232–C communications and is particularly valuable where higher voltage power supplies for RS–232 drivers are not available. The power supply section of the DS1229 supplies ±10V from the V_{CC} input.

OPERATION

The DS1229 consists of three major sections: a triple transmitter, a triple receiver and a dual charge pump which generates ±10V from the 5V supply.

CHARGE PUMP SECTION

The dual charge pumps within the DS1229 are used to generate the voltages necessary for level conversion from TTL/CMOS to RS-232. One charge pump uses external capacitor C1 to double the V_{CC} input to +10V. The second charge pump uses external capacitor C2 to invert the +10V to -10V. Capacitors C3 and C4 are used to filter the +10V and -10V power supply. The recommended size of capacitors C1-C4 is 22 µF but the value is not critical. Increasing the value of C3 and C4 will lower the 16 KHz ripple on the +10V supplies and the RS-232 outputs. The value of C1 and C4 can be lowered to 1 µF where size is critical.

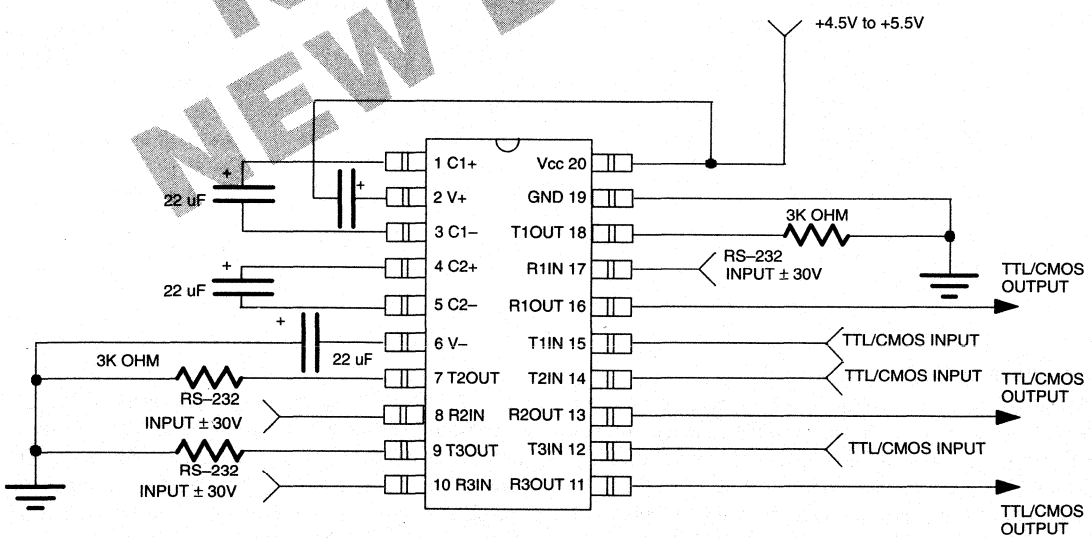
TRANSMITTER SECTION

The three transmitters are CMOS inverters powered by the internal +10V supply. The input is TTL/CMOS-compatible. Each input has an internal 750K pull-up resistor so that unused transmitter inputs can be left unconnected. Unused transmitter inputs will force the outputs low. The open circuit output voltage swing is from +10V to -10V. Worst-case conditions for RS-232-C of ±5V driving a 3K load are met at maximum allowable ambient temperature and a V_{CC} level of 5.0V. Typical voltage swings of ±9V occur with outputs of 5K and V_{CC} equal to 5V. The slew rate at the output is limited to less than 30V/us and the power-down output impedance will be a minimum of 300 ohms with ±2V applied to the outputs and V_{CC} at zero volts. The outputs are also short-circuit-protected and can be short-circuited to ground indefinitely.

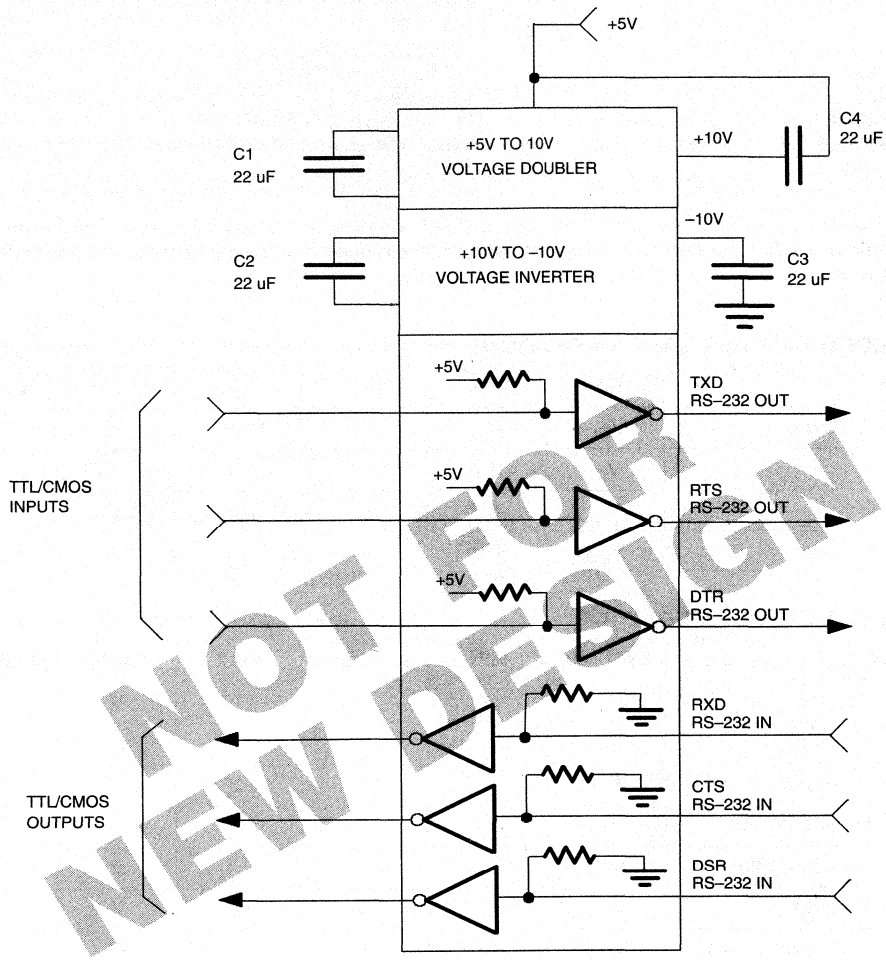
RECEIVER SECTION

The three receivers conform fully to the RS-232-C specifications. The input impedance is between 3K ohms and 7K ohms and can withstand up to ±30V with or without V_{CC} applied. The input switching thresholds are within the ±3V limit of RS-232-C specification with a V_{IL} of 0.7V and a V_{IH} of 2.4V. The receivers have 0.5 volts of hysteresis to improve noise rejection. The TTL/CMOS compatible output of the receiver will be low whenever the RS-232 input is greater than 2.4 volts. The receiver output will be high when the input is floating or driven between +0.8V and -30 V.

DS1229 RS-232 TRANSMITTER/RECEIVER Figure 1



TYPICAL APPLICATIONS Figure 2



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ABSOLUTE MAXIMUM RATINGS*

V_{CC}	7.0V
V+	+12 volts
V-	-12 volts
Transmitter Inputs	-0.3V to (V_{CC} +0.3V)
Receiver Inputs	±30 volts
Transmitter Outputs	(V+ + 0.3V) to (V - -0.3V)
Receiver Outputs	-0.3V to (V_{CC} + 0.3V)
Storage Temperature	–55°C to +125°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.2		V_{CC} +0.3	V	1
Logic 0 Input	V_{IL}	-0.3		+0.8	V	1
RS-232 Input Voltage	V_{RS}	-30		+30	V	1,2,11

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RS-232 Output Voltage	V_{ORS}	±4	±9	±10	V	3,12
Power Supply Current	I_{DD}		5	10	mA	4
Transmitter Pull-up Current	I_{TP}		5	200	µA	5
RS-232 Input Threshold Low	V_{TL}	0.7	1.2		V	6
RS-232 Input Threshold High	V_{TH}		1.7	2.4	V	6
RS-232 Input Hysteresis	V_{HY}	0.2	0.5	1.0	V	
Receiver Output Current @ 2.4V	I_{OH}	-1.0			mA	
Receiver Output Current @ 0.4V	I_{OL}			3.2	mA	
Output Resistance	R_{OUT}	300			ohms	7
RS-232 Output Current @ 0.4 V	I_{SC}			±25	mA	
Propagation Delay	t_{PD}		3		µs	8
Transmitter Output Instantaneous Slew Rate	t_{SR}			30	V/µs	9
Transmitter Output Transition Slew Rate	t_{TSR}		3		V/µs	10

NOTES:

1. All voltages are referenced to ground.
2. Applies to Receiver Inputs only.
3. T1, T2, and T3 loaded with 3K ohms to ground.
4. All outputs are unloaded.
5. T1, T2, and T3 Inputs = 0 volts.
6. V_{CC} = +5 volts.
7. V_{OUT} = ±2 volts.
8. RS-232 to TTL or TTL to RS-232.
9. C_L = 10 pF, R_L = 3K, t_A = 0°C. This parameter is sample tested only.
10. R_L = 3K, C_L = 2500 pF measured from +3 volts to -3 volts or -3 volts to +3 volts.
11. This parameter is sample tested only.
12. Negative output level of -5V is increased to -4.0 for the DS1229 only. Positive output level remains at +5V. Use of a +10%, -5% power supply will restore the negative level to -5V.

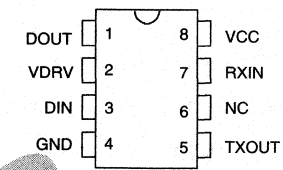
DALLAS SEMICONDUCTOR

DS1275
Line-Powered RS-232 Transceiver Chip

FEATURES

- Low-power serial transmitter/receiver for battery-backed systems
- Transmitter steals power from receive signal line to save power
- Ultra-low static current, even when connected to RS-232-C port
- Variable transmitter level from +5 to +12 volts
- Compatible with RS-232-C signals
- Available in 8-pin, 150-mil wide SOIC package (DS1275S)
- Low-power CMOS

PIN ASSIGNMENT



DS1275 8-Pin DIP (300 Mil.)
See Mech. Drawings Section

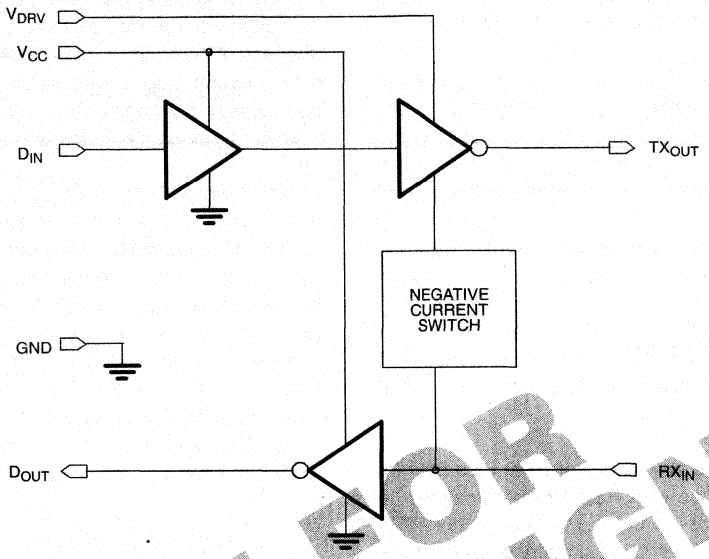
PIN DESCRIPTION

D_{OUT}	–	Digital data out
V_{DRV}	–	Transmit driver +V
D_{IN}	–	Digital data in
GND	–	System ground (0V)
TX_{OUT}	–	Transmit RS-232 out
NC	–	No connection
RX_{IN}	–	Receive RS-232 in
V_{CC}	–	System logic supply (+5V)

DESCRIPTION

The DS1275 Line-Powered RS-232 Transceiver Chip is a CMOS device that provides a low-cost, very low-power interface to RS-232 serial ports. The receiver input translates RS-232 signal levels to common CMOS/TTL levels. The transmitter employs a unique circuit which steals current from the receive RS-232 signal when that signal is in a negative state (marking). Since most serial communication ports remain in a negative state statically, using the receive signal for negative power greatly reduces the DS1275's static power consumption. This feature is especially important for battery-powered systems such as laptop computers, remote sensors, and portable medical instruments. During an actual communication session, the DS1275's transmitter will use system power (5-12 volts) for positive transitions while still employing the receive signal for negative transitions.

DS1275 BLOCK DIAGRAM Figure 1



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OPERATION

Designed for the unique requirements of battery-backed systems, the DS1275 provides a low-power half-duplex interface to an RS-232 serial port. Typically, a designer must use an RS-232 device which uses system power during both negative and positive transitions of the transmit signal to the RS-232 port. If the connector to the RS-232 port is left connected for an appreciable time after the communication session has ended, power will statically flow into that port, draining the battery capacity. The DS1275 eliminates this static current drain by stealing current from the receive line (RX_{IN}) of the RS-232 port when that line is at a negative level (marking). Since most asynchronous communication over an RS-232 connection typically remains in a marking state when data is not being sent, the DS1275 will not consume system power in this condition. System power would only be used when positive-going transitions are needed on the transmit RS-232 output (TX_{OUT}) when data is sent. However, since synchronous communication sessions typically exhibit a very low duty-cycle, overall system power consumption remains low.

RECEIVER SECTION

The RX_{IN} pin is the receive input for an RS-232 signal whose levels can range from ±3 to ±15 volts. A negative data signal is called a mark while a positive data signal is called a space. These signals are inverted and then level-shifted to normal +5 volt CMOS/TTL logic levels. The logic output associated with RX_{IN} is D_{OUT} which swings from $+V_{CC}$ to ground. Therefore, a mark on RX_{IN} produces a logic 1 at D_{OUT}; a space produces a logic 0.

The input threshold of RX_{IN} is typically around 1.8 volts with 500 millivolts of hysteresis to improve noise rejection. Therefore, an input positive-going signal must exceed 1.8 volts to cause D_{OUT} to switch states. A negative-going signal must now be lower than 1.3 volts (typically) to cause D_{OUT} to switch again. An open on RX_{IN} is interpreted as a mark, producing a logic 1 at D_{OUT}.

TRANSMITTER SECTION

D_{IN} is the CMOS/TTL-compatible input for digital data from the user system. A logic 1 at D_{IN} produces a mark (negative data signal) at TX_{OUT} while a logic 0 produces a space (positive data signal). As mentioned earlier, the transmitter section employs a unique driver design that uses the RX_{IN} line for swinging to negative levels. The RX_{IN} line must be in a marking or idle state to take advantage of this design; if RX_{IN} is in a spacing state, TX_{OUT} will only swing to ground. When TX_{OUT} needs to transition to a positive level, it uses the V_{DRV} power pin for this level. V_{DRV} can be a voltage supply between 5 to

12 volts, and in many situations it can be tied directly to the +5 volt V_{CC} supply. *It is important to note that V_{DRV} must be greater than or equal to V_{CC} at all times.*

The voltage range on V_{DRV} permits the use of a 9-volt battery in order to provide a higher voltage level when TX_{OUT} is in a space state. When V_{CC} is shut off to the DS1275 and V_{DRV} is still powered (as might happen in a battery-backed condition) , only a small leakage current (about 50-100 nA) will be drawn. If TX_{OUT} is loaded during such a condition, V_{DRV} will draw current only if RX_{IN} is not in a negative state. During normal operation (V_{CC}=5 volts), V_{DRV} will draw less than 2 uA when TX_{OUT} is marking. Of course, when TX_{OUT} is spacing, V_{DRV} will draw substantially more current – about 3 mA depending upon its voltage and the impedance that TX_{OUT} sees.

The TX_{OUT} output is slew-rate limited to less than 30 volts/us in accordance with RS-232 specifications. In the event TX_{OUT} should be inadvertently shorted to ground, internal current-limiting circuitry prevents damage, even if continuously shorted.

RS-232 COMPATIBILITY

The intent of the DS1275 is not so much to meet all the requirements of the RS-232 specification as to offer a low-power solution that will work with most RS-232 ports with a connector length of less than 10 feet. As a prime example, the DS1275 will not meet the RS-232 requirement that the signal levels be at least ±5 volts minimum when terminated by a 3K ohm load and V_{DRV}= +5 volts. Typically a voltage of 4 volts will be present at TX_{OUT} when spacing. However, since most RS-232 receivers will correctly interpret any voltage over 2 volts as a space, there will be no problem transmitting data.

APPLICATIONS INFORMATION

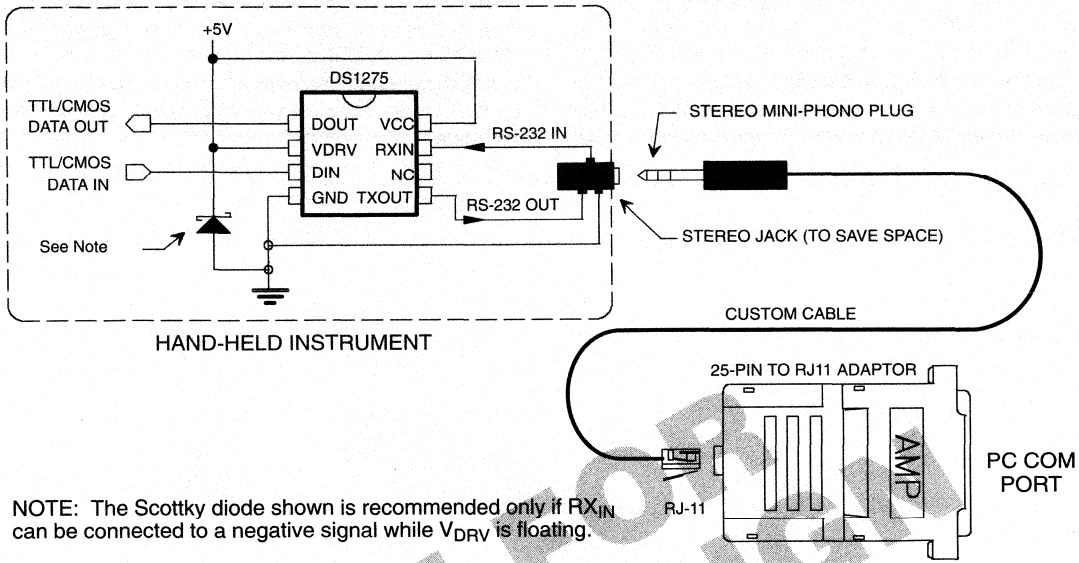
The DS1275 is designed as a low-cost, RS-232-C interface expressly tailored for the unique requirements of battery-operated handheld products. As shown in the electrical specifications, the DS1275 draws exceptionally low operating and static current. During normal operation when data from the handheld system is sent from the TX_{OUT} output, the DS1275 only draws significant V_{DRV} current when TX_{OUT} transitions positively (spacing). This current flows primarily into the RS-232 receiver's 3-7K ohm load at the other end of the attaching cable. When TX_{OUT} is marking (a negative data signal), the V_{DRV} current falls dramatically since the negative voltage is provided by the transmit signal from the other end of the cable. This represents a large reduction in overall operating current, since typical RS-232 interface chips use charge-pump circuits to establish both positive and negative levels at the transmit driver output.

To obtain the lowest power consumption from the DS1275, observe the following guidelines. First, to minimize V_{DRV} current when connected to an RS-232 port, always maintain D_{IN} at a logic 1 when data is not being transmitted (idle state). This will force TX_{OUT} into the marking state, minimizing V_{DRV} current. Second, V_{DRV} current will drop to less than 100 nA when V_{CC} is grounded. Therefore, if V_{DRV} is tied directly to the system battery, the logic +5 volts can be turned off to achieve the lowest possible power state.

FULL-DUPLEX OPERATION

The DS1275 is intended primarily for half-duplex operation; that is, RX_{IN} should remain idle in the marking state when transmitting data out TX_{OUT} and visa versa. However, the part can be operated full-duplex with most RS-232-C serial ports since signals swinging between 0 and +5V will usually be correctly interpreted by an RS-232-C receiver device. The 5-volt swing occurs when TX_{OUT} attempts to swing negative while RX_{IN} is at a positive voltage, which turns on an internal weak pull-down to ground for the TX_{OUT} driver's negative reference. So, transmit mark signals at TX_{OUT} may have voltage jumps from some negative value (corresponding to RX_{IN} marking) to approximately ground. One possible problem that may occur in this case is if the receiver at the other end requires a negative voltage for recognizing a mark. In this situation, the full- duplex circuit shown in Figure 3 can be used as an alternative. The 22 µF capacitor forms a negative-charge reservoir; consequently, when the TXD line is spacing (positive), TX_{OUT} still has a negative source available for a time period determined by the capacitor and the load resistance at the other end (3-7K ohms). This circuit was tested from 150-19,200 bps with error-free operation using a SN75154 Quad Line Receiver as the receiver for the TX_{OUT} signal. Note that the SN75154 can have a marking input threshold below ground; hence there is the need for TX_{OUT} to swing both positive and negative in full-duplex operation with this device.

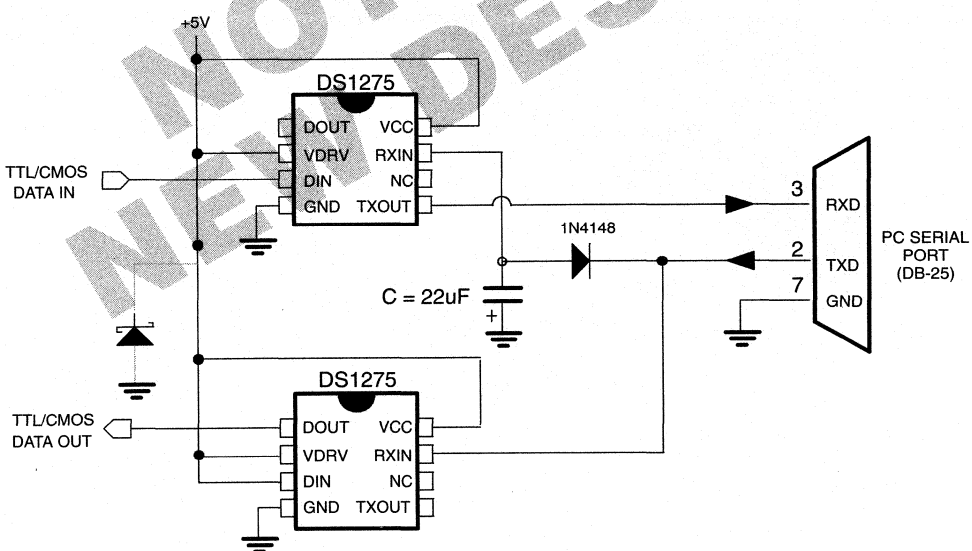
HANDHELD RS-232-C APPLICATION USING A STEREO MINI-JACK Figure 2



NOTE: The Scottky diode shown is recommended only if RX_{IN} can be connected to a negative signal while V_{DRV} is floating.

5

FULL-DUPLEX CIRCUIT USING NEGATIVE-CHARGE STORAGE Figure 3



NOTE:

The capacitor stores negative charge whenever the TXD signal from the PC serial port is in a marking data state (a negative voltage that is typically -10 volts). The top DS1275's TX_{OUT} uses this negative charge reservoir when it is in a marking state. The capacitor will discharge to 0 volts when the TXD line is spacing (and TX_{OUT} is still marking) at a time constant determined by its value and the value of the load resistance reflected back to TX_{OUT}. However, when TXD is marking, the capacitor will quickly charge back to -10 volts. Note that TXD remains in a marking state when idle, which improves the performance of this circuit.

LATCHUP PROTECTION

In most cases the DS1275 offers a high level of ESD and latchup protection. However, latchup can occur if V_{DRV} is left floating (high impedance) while a negative signal is attached to RX_{IN}. One possible scenario for this is as follows: if the handheld device is powered off with a FET switch, floating V_{DRV}, and at the same time the user still has the the RS-232-C port connected. In order to eliminate this latchup potential, a Schottky diode from V_{DRV} to ground is recommended as shown in Figure 2. The lower clamp voltage of the Schottky (300 mV) is required to prevent an internal silicon diode on the DS1275 from turning on, which precipitates the latchup condition.

ABSOLUTE MAXIMUM RATINGS*

V_{CC}	-0.3 to +7 volts
V_{DRV}	-0.3 to +13 volts
RX_{IN}	±15 volts
D_{IN}	-0.3 to V_{CC} + 0.3 volts
TX_{OUT}	±15 volts
D_{OUT}	-0.3 to V_{CC} + 0.3 volts
Storage Temperature	-55°C to +125°C
Operating Temperature	0°C to 70°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic Supply	V_{CC}	4.5	5.0	5.5	V	1
Transmit Driver Supply	V_{DRV}	4.5	5-12	13.0	V	1
Logic 1 Input	V_{IH}	2.0		V_{CC}+0.3	V	2
Logic 0 Input	V_{IL}	-0.3		+ 0.8	V	
RS-232 Input Range (RX_{IN})	V_{RS}	-15		+15	V	
Dynamic Supply Current D_{IN} = V_{CC} D_{IN} = GND	 I_{DRV1} I_{CC1} I_{DRV1} I_{CC1}		 0.1 0.5 3.8 0.5	 5.0 5.0 5.0 5.0	 mA mA mA mA	3
Static Supply Current D_{IN} = V_{CC} D_{IN} = GND	 I_{DRV2} I_{CC2} I_{DRV2} I_{CC2}		 1.5 10.0 3.8 10.0	 15.0 15.0 5.0 30.0	 µA µA mA µA	4
Driver Leakage Current (V_{CC}= 0V)	I_{DRV3}		0.05	1.0	µA	5

DC ELECTRICAL CHARACTERISTICS

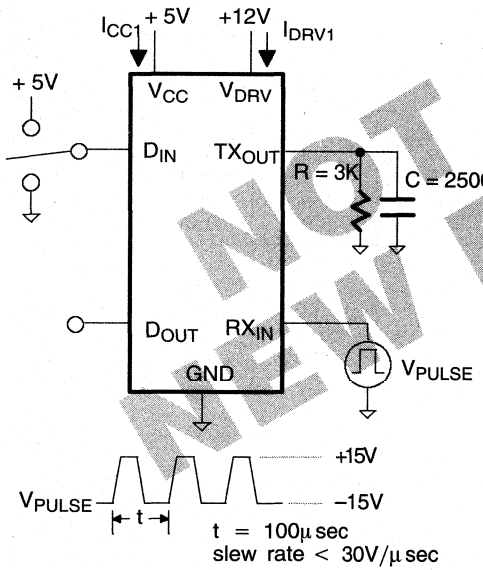
(0°C to 70°C; V_{CC} = V_{DRV} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TX_{OUT} Level High	V_{OTXH}	3.5	4.0	4.5	V	6
TX_{OUT} Level Low	V_{OTXL}	-8.5	-9.0		V	7
TX_{OUT} Short Circuit Current	I_{SC}		+60	+85	mA	
TX_{OUT} Output Slew Rate	t_{SR}			30	V/µs	
Propagation Delay	t_{PD}		5		µs	8
RX_{IN} Input Threshold Low	V_{TL}	0.8	1.2	1.6	V	
RX_{IN} Input Threshold High	V_{TH}	1.6	2.0	2.4	V	
RX_{IN} Threshold Hysteresis	V_{HYS}	0.5	0.8		V	9
D_{OUT} Output Current @ 2.4 V	I_{OH}	-1.0			mA	
D_{OUT} Output Current @ 0.4 V	I_{OL}			3.2	mA	

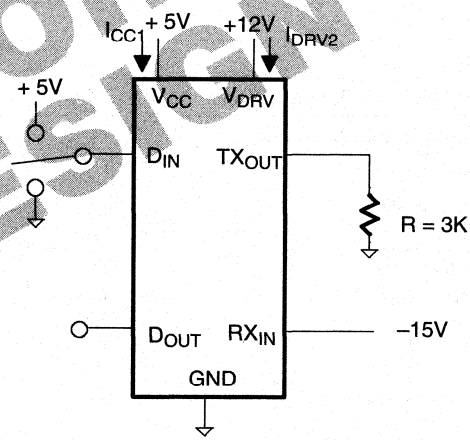
NOTES:

1. V_{DRV} must be greater than or equal to V_{CC}.
2. $V_{CC} = V_{DRV} = 5V \pm 10\%$.
3. See test circuit in Figure 4.
4. See test circuit in Figure 5.
5. See test circuit in Figure 6.
6. $D_{IN} = V_{IL}$ and TX_{OUT} loaded by 3K ohms to ground.
7. $D_{IN} = V_{IH}$, RX_{IN} = -10 volts and TX_{OUT} loaded by 3K ohms to ground.
8. D_{IN} to TX_{OUT} - see Figure 7.
9. $V_{HYS} = V_{TH} - V_{TL}$.

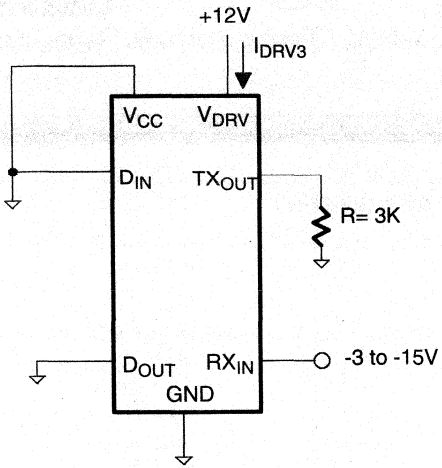
DYNAMIC OPERATING CURRENT TEST CIRCUIT Figure 4



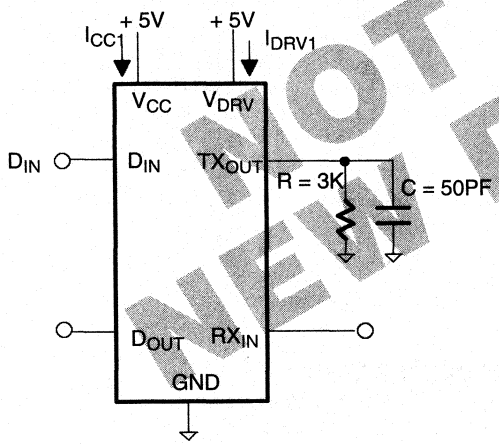
STATIC OPERATING CURRENT TEST CIRCUIT Figure 5

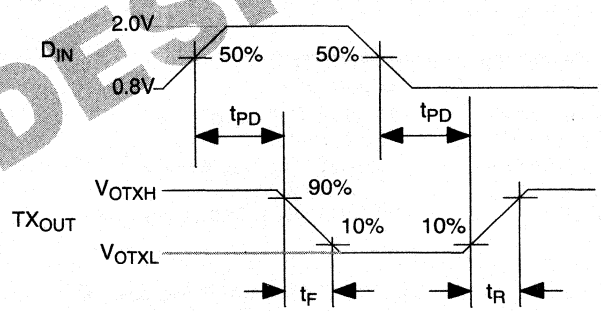


DRIVER LEAKAGE TEST CIRCUIT Figure 6



PROPAGATION DELAY TEST CIRCUIT Figure 7





$$t_{SR} = \frac{0.8(V_{OTXH} - V_{OTXL})}{t_F \text{ or } t_R}$$

5

DALLAS SEMICONDUCTOR

DS232A
Dual RS–232 Transmitter/Receiver

FEATURES

- Compatible with LT1181A and MAX232A
- High data rate – 250 kbits/sec under load
- 16–pin DIP or SOIC package
- 20–pin TSSOP package for height restricted applications
- Operate from single +5V power
- Meets all EIA–232E and V.28 specifications
- Uses small capacitors: 0.1 µF
- Optional industrial temperature range available (–40°C to +85°C)

ORDERING INFORMATION

DS232A	16–pin DIP
DS232A–N	16–pin DIP (Industrial)
DS232AS	16–pin SOIC
DS232AS–N	16–pin SOIC (Industrial)
DS232AE	20–pin TSSOP
DS232AE–N	20–pin TSSOP (Industrial)

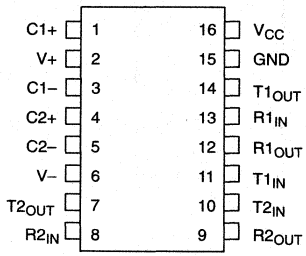
DESCRIPTION

The DS232A is a dual RS–232 driver/receiver pair that generates RS–232 voltage levels from a single +5 volt power supply. Additional ±12 volt supplies are not needed since the DS232A uses on–board charge pumps to convert the +5 volt supply to ±10 volts. The DS232A is fully compliant with EIA RS–232E and V.28/V.24 standards. The DS232A contains two drivers and two receivers. Driver slew rates and data rates are guaranteed up to 250 kbits/sec. The DS232A operates with only 0.1 µF charge pump capacitors.

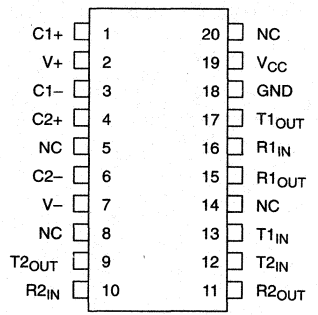
OPERATION

The diagram in Figure 1 shows the main elements of the DS232A. The following paragraphs describe the function of each pin.

PIN ASSIGNMENT



16–PIN DIP AND SOIC

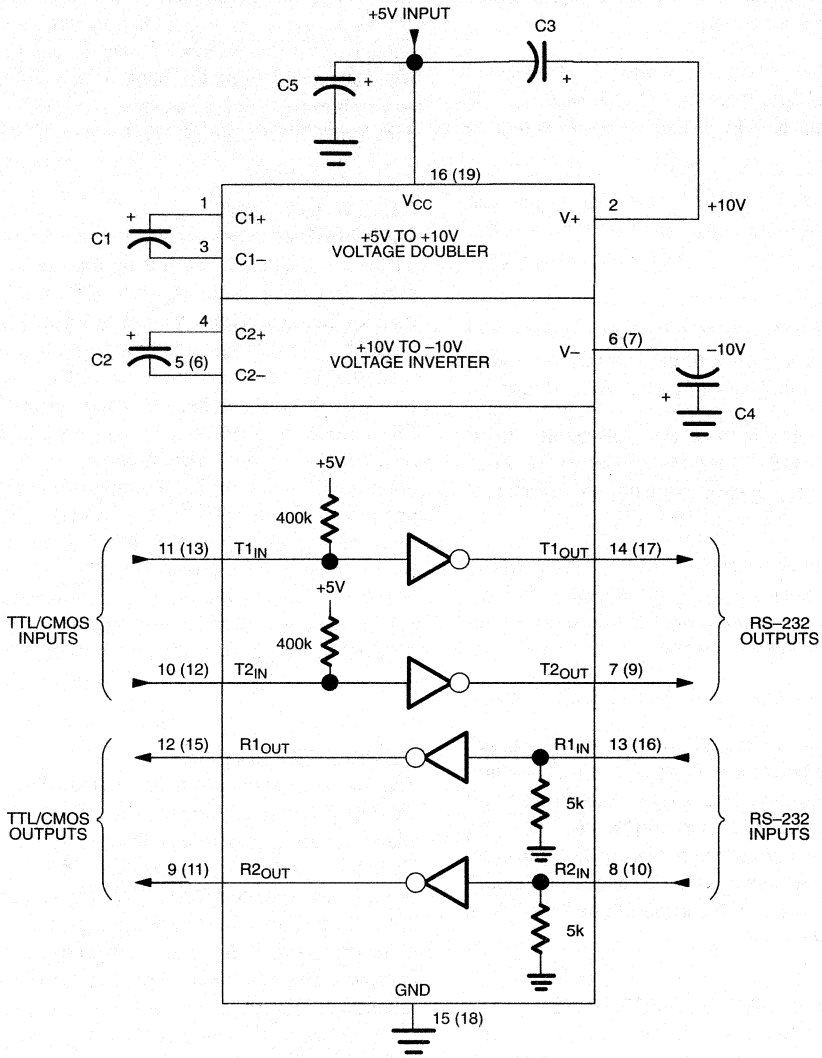


20–PIN TSSOP

PIN DESCRIPTION

V_{CC}	–	+5 Volt Supply
GND	–	Ground
V+	–	Positive Supply Output
V–	–	Negative Supply Output
$T1_{IN}$, $T2_{IN}$	–	RS–232 Driver Inputs
$T1_{OUT}$, $T2_{OUT}$	–	RS–232 Driver Outputs
$R1_{IN}$, $R2_{IN}$	–	Receiver Inputs
$R1_{OUT}$, $R2_{OUT}$	–	Receiver Outputs
C1+, C1–	–	Capacitor 1 Connections
C2+, C2–	–	Capacitor 2 Connections

FUNCTIONAL DIAGRAM OF DS232A Figure 1



NOTE: C5 is a recommended decoupling capacitor which is the same value as C1, C2, C3, and C4.

( ) Are for TSSOP package only.

PIN DESCRIPTIONS

V_{CC}, GND: DC power is provided to the device on these pins. V_{CC} is the +5 volt input.

V+: Positive supply output (RS–232). V+ requires an external storage charge capacitor of at least 0.1 µF. A larger capacitor (up to 10 µF) can be used to reduce supply ripple.

V–: Negative supply output (RS–232). V– requires an external storage capacitor of at least 0.1 µF. A larger capacitor (up to 10 µF) can be used to reduce supply ripple.

$T1_{IN}$, $T2_{IN}$: Standard TTL/CMOS inputs for the RS–232 drivers. The inputs of unused drivers can be left unconnected since each input has a 400 kΩ pull–up resistor.

$T1_{OUT}$, $T2_{OUT}$: Driver outputs at RS–232 levels. Driver output swing meets RS–232 levels for loads up to 3 kΩ. These driver outputs provide current necessary to meet RS–232 levels for loads up to 2500 pF.

$R1_{IN}$, $R2_{IN}$: Receiver inputs. These inputs accept RS–232 level signals (±25 volts) into a protected 5 kΩ terminating resistor. Each receiver provides 0.5V hysteresis (typical) for noise immunity.

$R1_{OUT}$, $R2_{OUT}$: Receiver outputs at TTL/CMOS levels.

C1+, C1–, C2+, C2–: Charge pump capacitor inputs. These pins require two external capacitors (0.1 µF minimum, 10 µF maximum and should be the same size as C3 and C4). Capacitor 1 is connected between C1+ and C1–. Capacitor 2 is connected between C2+ and C2–. Capacitor C1 can be omitted if +12 volts is connected directly to V+. Likewise, C2 can be omitted if –12V is connected directly to V–.

DUAL CHARGE PUMP CONVERTERS

The DS232A has a two stage on–board charge pump circuit that is used to generate ±10 volts from a single +5 volt supply. In the first stage, capacitor C1 doubles the +5V supply to +10 volts which is then stored on capacitor C3. The second stage uses capacitor C2 to invert the +10V potential to –10V. This charge is then stored on capacitor C4. The ±10 volt supplies allow the DS232A to provide the necessary output levels for RS–232 communication. The DS232A will operate with charge pump capacitors as low as 0.1 µF. Larger capacitors (up to 10 µF) can be used to reduce supply ripple.

RS–232 DRIVERS

The two RS–232 drivers are powered by the internal ±10 volt supplies generated by the on–board charge pump. The driver inputs are both TTL and CMOS compatible. Each input has an internal 400 kΩ pull–up resistor so that unused transmitter inputs can be left unconnected. The open circuit output voltage swing is from (V+ – 0.6) to V– volts. Worst case conditions for EIA–232E/V.28 of ±5 volt driving a 3 kΩ load and 2500 pF are met at maximum operating temperature and V_{CC} equal to 4.5 volts. Typical voltage swings of ±8 volts occur when loaded with a nominal 5 kΩ RS–232 receiver. As required by EIA–232E and V.28 specifications, the slew rate at the output is limited to less than 30 volts/µs. Typical slew rates are 20 volts/µs unloaded and 12 volts/µs with 3 kΩ and 2500 pF load. These slew rates allow for bit rates of over 250 kbits/s. Driver outputs maintain high impedance when power is off.

RS–232 RECEIVERS

The two receivers conform fully to the RS–232E specifications. The input impedance is typically 5 kΩ and can withstand up to ±25 volts with or without V_{CC} applied. The input switching thresholds are within the ±3 volt limit of RS–232E specification with an input threshold low of 0.8 volts and an input threshold high of 2.4 volts. The receivers have 0.5 volts of hysteresis (typical) to improve noise rejection. The TTL/CMOS compatible outputs of the receivers will be low whenever the RS–232 input is greater than 2.4 volts. The receiver output will be high when the input is floating or driven between +0.8 volts and –25 volts.

ABSOLUTE MAXIMUM RATINGS*

Absolute Maximum Ratings

V_{CC}	−0.3V to +7.0V
V+	(V_{CC}−0.3V) to +14V
V−	+0.3V to −14V

Input Voltages

T_{IN}	−0.3V to (V_{CC}+0.3V)
R_{IN}	±30V

Output Voltages

T_{OUT}	(V+ + 0.3V) to (V− − 0.3V)
R_{OUT}	−0.3V to (V_{CC} + 0.3V)
Short Circuit Duration, T_{OUT}	Continuous

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Votlage	V_{CC}	4.5		5.5	V	1

5

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Current (No Load)	I_{CC1}		4	10	mA	
Power Supply Current (3 kΩ Load Both Outputs)	I_{CC2}		15		mA	
RS–232 Transmitters						
Output Voltage Swing	V_{ORS}	±5	±8		V	2
Input Logic Threshold Low	V_{TTL}	0.8	1.4		V	
Input Logic Threshold High	V_{TTH}		1.4	2.0	V	
Maximum Data Rate	f_D	250	350		kbits/s	
Logic Pull–up/Input Current	I_{PU}		5	40	µA	
Transmitter Output Resistance	R_{OUT}	300	10M		Ω	3
Output Short–Circuit Current	I_{TSC}	±15	±30	±100	mA	4

DC ELECTRICAL CHARACTERISTICS (cont'd)

(0°C to 70°C)

RS–232 Receivers						
RS–232 Input Voltage Operating Range	V_{IR}	±25	±30		V	
RS–232 Input Threshold Low	V_{RTL}	0.8	1.3		V	
RS–232 Input Threshold High	V_{RTH}		1.8	2.4	V	
RS–232 Input Hysteresis	V_{HY}	0.2	0.5	1	V	
RS–232 Input Resistance	R_{IN}	3	5	7	kΩ	
TTL/CMOS Output Voltage Low	V_{ROL}		0.2	0.4	V	5
TTL/CMOS Output Voltage High	V_{ROH}	3.5	V_{CC}–0.2		V	6
TTL/CMOS Output Short Circuit Current (V_{OUT}=GND)	I_{RSC}	–2	–10		mA	
TTL/CMOS Output Short Circuit Current (V_{OUT}=V_{CC})	I_{RSC}	10	30		mA	

AC ELECTRICAL CHARACTERISTICS

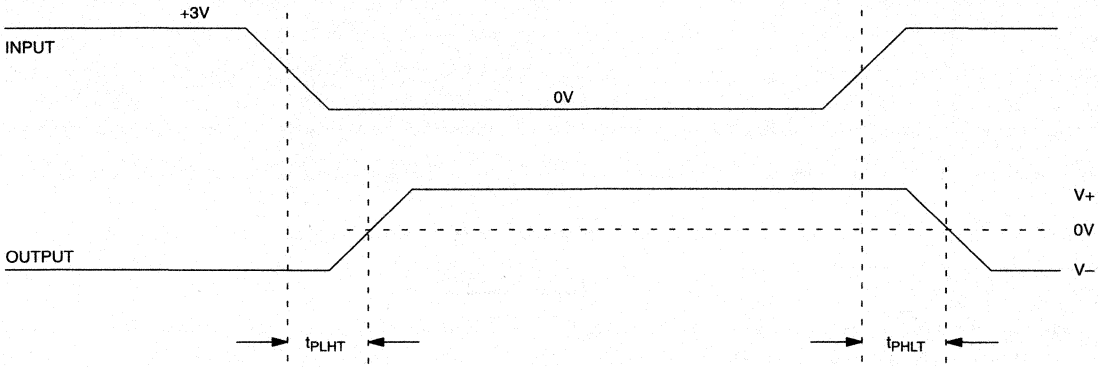
(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Transition Slew Rate	t_{SR}	6	12	30	V/µs	7
Transmitter Propagation Delay TTL to RS–232	t_{PHLT} t_{PLHT}		1.3 1.5	3.5 3.5	µs µs	
Receiver Propagation Delay RS–232 to TTL	t_{PHLR} t_{PLHR}		0.5 0.6	1 1	µs µs	
Transmitter + to – Propagation Delay Difference	t_{PHLT} $-t_{PLHT}$		300		ns	
Receiver + to – Propagation Delay Difference	t_{PHLR} $-t_{PLHR}$		100		ns	

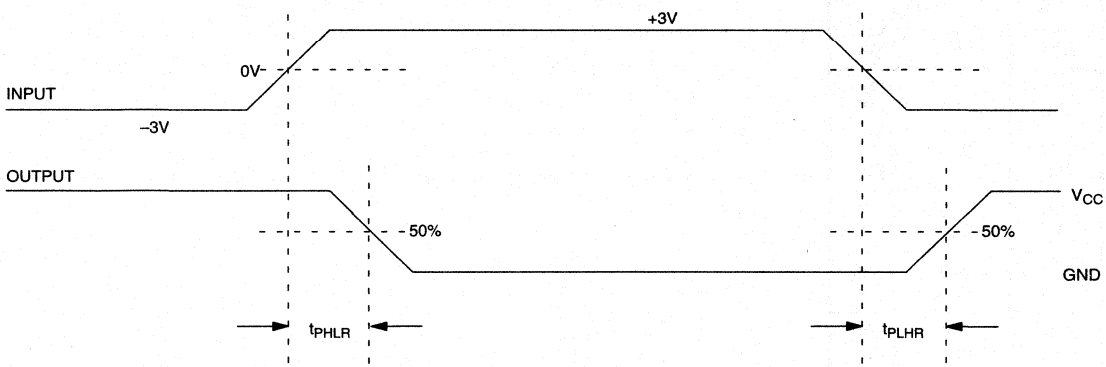
NOTES:

1. All voltages are referenced to ground.
2. All transmitter outputs loaded with 3 kΩ to ground.
3. V_{CC} = V+ = V– = 0V; V_{OUT} = ±2V .
4. V_{OUT} = 0V.
5. I_{OUT} = 3.2 mA.
6. I_{OUT} = –1.0 mA.
7. C_L = 50 pF – 2500 pF; RL = 3 kΩ – 7 kΩ; V_{CC} = 5V; TA = 25°C.

TRANSMITTER PROPAGATION DELAY TIMING Figure 2



RECEIVER PROPAGATION DELAY TIMING Figure 3



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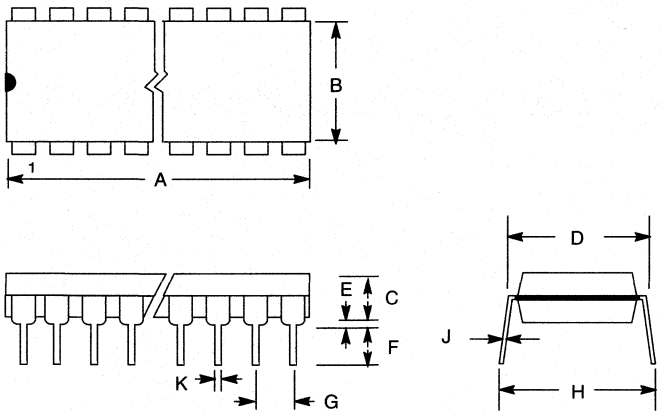
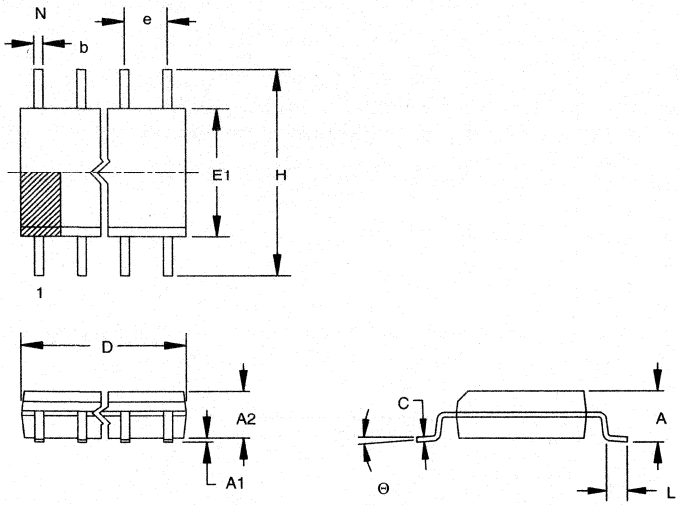
16–PIN DIP (300 MIL)



PKG	16-PIN	
DIM	MIN	MAX
A IN. MM	0.740 18.80	0.780 19.81
B IN. MM	0.240 6.10	0.260 6.60
C IN. MM	0.120 3.05	0.140 3.56
D IN. MM	0.300 7.62	0.325 8.26
E IN. MM	0.015 0.38	0.040 1.02
F IN. MM	0.120 3.04	0.140 3.56
G IN. MM	0.090 2.29	0.110 2.79
H IN MM	0.320 8.13	0.370 9.40
J IN MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53

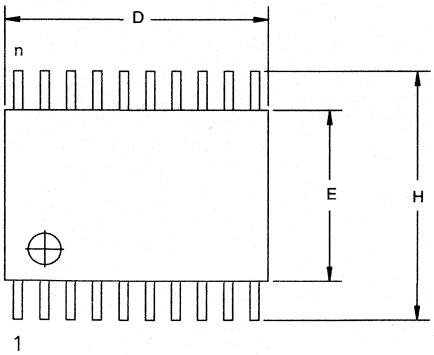
16–PIN SOIC (300 MIL)

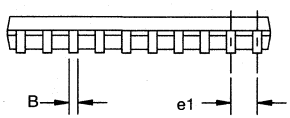


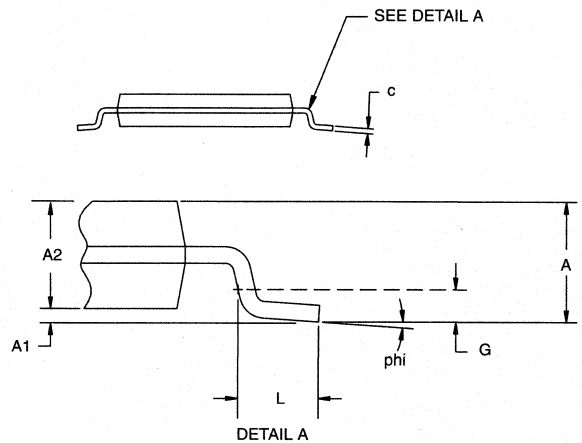
PKG	16-PIN	
DIM	MIN	MAX
A IN. MM	0.094 2.39	0.105 2.67
A1 IN. MM	0.004 0.102	0.012 0.30
A2 IN. MM	0.089 2.26	0.095 2.41
b IN. MM	0.013 0.33	0.020 0.51
C IN. MM	0.009 0.229	0.013 0.33
D IN. MM	0.398 10.11	0.412 10.46
e IN. MM	0.050 BSC 1.27 BSC	
E1 IN MM	0.290 7.37	0.300 7.62
H IN MM	0.398 10.11	0.416 10.57
L IN. MM	0.016 0.40	0.040 1.02
Θ	0°	8°

5

20-PIN TSSOP







DIM	MIN	MAX
A MM	–	1.10
A1 MM	0.05	–
A2 MM	0.75	1.05
C MM	0.09	0.18
L MM	0.50	0.70
e1 MM	0.65 BSC	
B MM	0.18	0.30
D MM	6.40	6.90
E MM	4.40 NOM	
G MM	0.25 REF	
H MM	6.25	6.55
phi	0°	8°

DALLAS SEMICONDUCTOR

DS233A
Dual RS–232 Transmitter/Receiver

FEATURES

- Compatible with MAX233A
- High data rate – 250 kbits/sec under load
- No need for external capacitors
  - Charge pump capacitors built in
- 20–pin DIP and SOIC package
- Operate from single +5V power
- Driver outputs maintain high impedance with power off
- Meets all EIA–232E and V.28 specifications
- Optional industrial temperature range available (–40°C to +85°C)

ORDERING INFORMATION

DS233A	20–pin DIP
DS233A–N	20–pin DIP (Industrial)
DS233AS	20–pin SOIC
DS233AS–N	20–pin SOIC (Industrial)

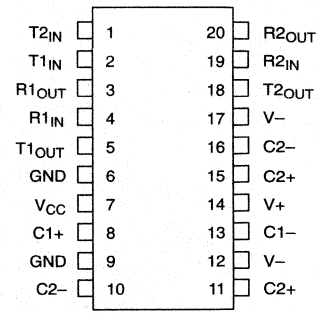
DESCRIPTION

The DS233A is a dual RS–232 driver/receiver pair that generates RS–232 voltage levels from a single +5 volt power supply. Additional ±12 volt supplies are not needed since the DS233A uses onboard charge pumps to convert the +5 volt supply to ±10 volts. The DS233A is fully compliant with EIA RS–232E and V.28/V.24 standards. The DS233A contains two drivers and two receivers. Driver slew rates and data rates are guaranteed up to 250 kbits/sec. The DS233A requires no external capacitors for the charge pump, because they are built–in to the device.

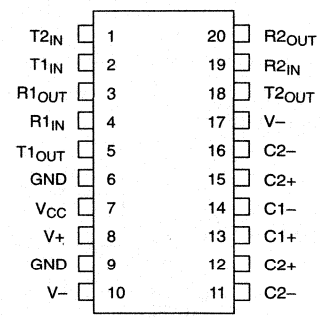
OPERATION

The diagram in Figure 1 shows the main elements of the DS233A. The following paragraphs describe the function of each pin.

PIN ASSIGNMENT



20–PIN DIP



20–PIN SOIC

PIN DESCRIPTION

V_{CC}	–	+5 Volt Supply
GND	–	Ground
V+	–	Positive Supply Output
V–	–	Negative Supply Output
$T1_{IN}$, $T2_{IN}$	–	RS–232 Driver Inputs
$T1_{OUT}$, $T2_{OUT}$	–	RS–232 Driver Outputs
$R1_{IN}$, $R2_{IN}$	–	Receiver Inputs
$R1_{OUT}$, $R2_{OUT}$	–	Receiver Outputs
C1+, C1–, C2+, C2–	–	Internal Capacitor Connections

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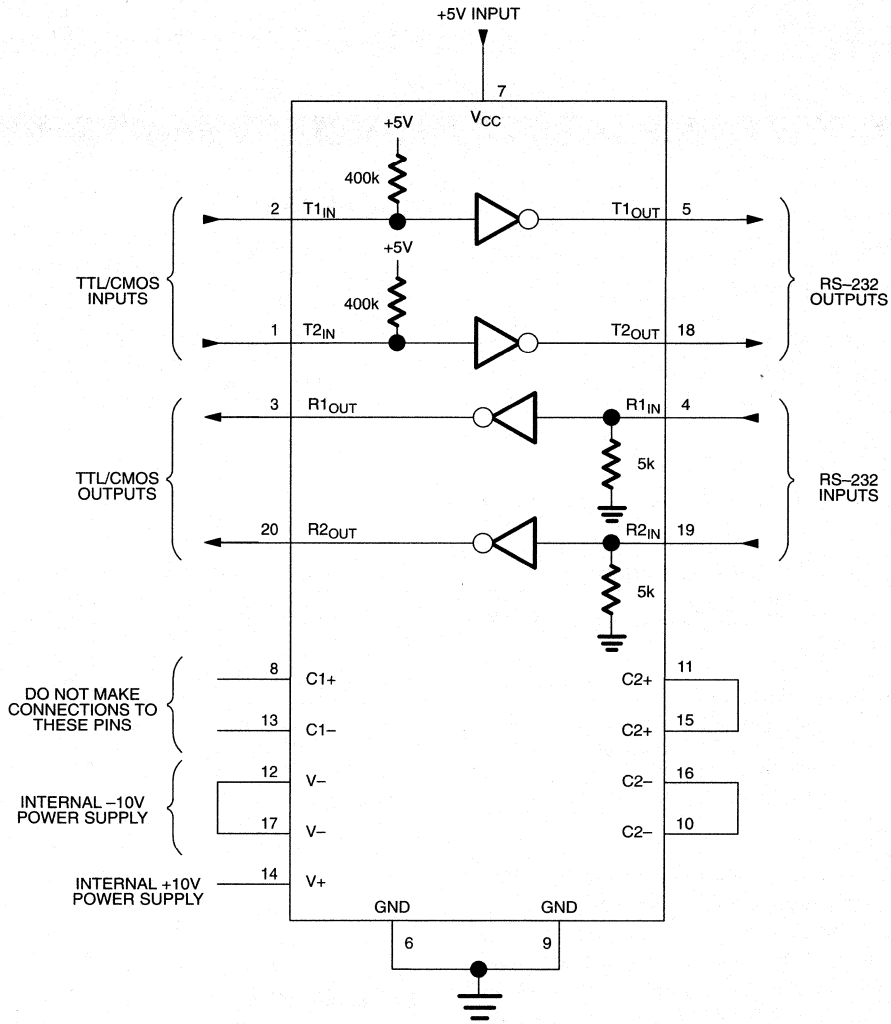
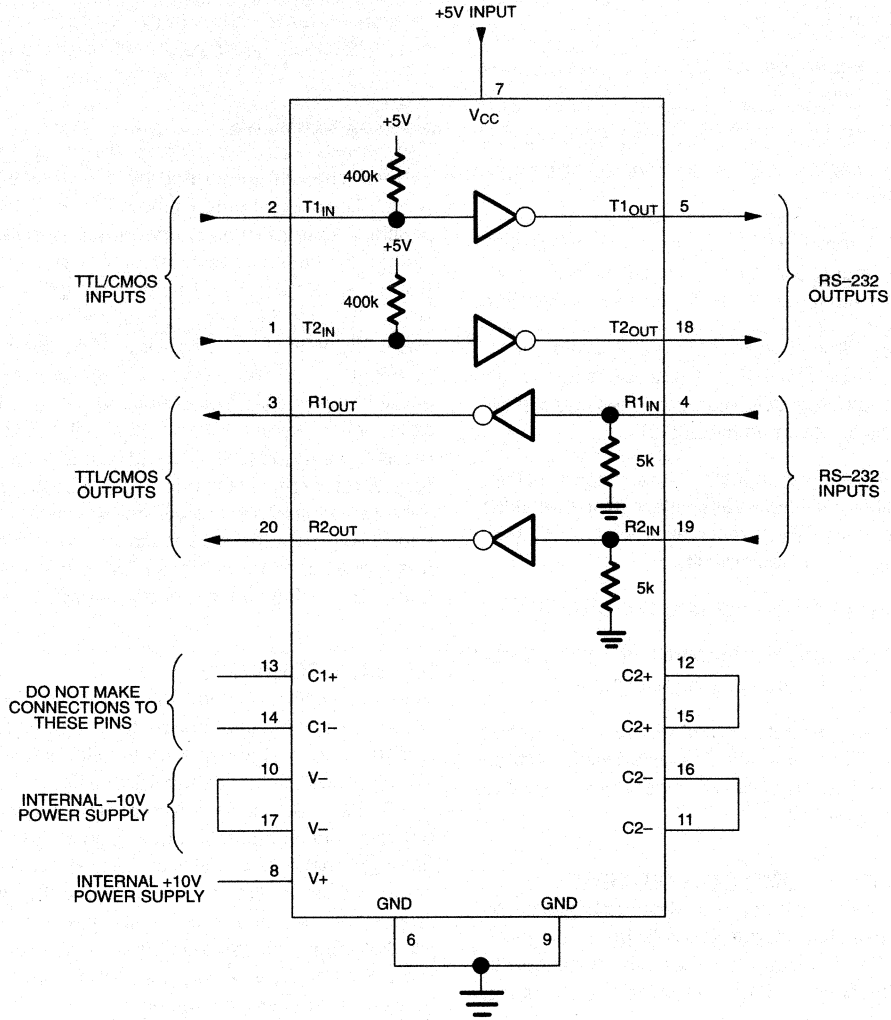
FUNCTIONAL DIAGRAM OF DS233A (20–PIN DIP) Figure 1



FUNCTIONAL DIAGRAM OF DS233A (20–PIN SOIC) Figure 2



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PIN DESCRIPTIONS

V_{CC}, GND: DC power is provided to the device on these pins. V_{CC} is the +5 volt input.

V+: Positive supply output (RS–232) generated by charge pump circuit.

V–: Negative supply output (RS–232) generated by charge pump circuit. The two V– pins must be connected together.

$T1_{IN}$, $T2_{IN}$: Standard TTL/CMOS inputs for the RS–232 drivers. The inputs of unused drivers can be left unconnected since each input has a 400 kΩ pull–up resistor.

$T1_{OUT}$, $T2_{OUT}$: Driver outputs at RS–232 levels. Driver output swing meets RS–232 levels for loads up to 3 kΩ. These driver outputs provide current necessary to meet RS–232 levels for loads up to 2500 pF.

$R1_{IN}$, $R2_{IN}$: Receiver inputs. These inputs accept RS–232 level signals (±25 volts) into a protected 5 kΩ terminating resistor. Each receiver provides 0.5V hysteresis (typical) for noise immunity.

$R1_{OUT}$, $R2_{OUT}$: Receiver outputs at TTL/CMOS levels.

C1+, C1–: These two pins are connected to the internal C1 capacitor. These pins must be left floating.

C2+, C2–: These two pins are connected to the internal C2 capacitor. There are two C2+ pins which must be connected together and two C2– pins which must also be connected together.

DUAL CHARGE PUMP CONVERTERS

The DS233A has a two stage on–board charge pump circuit that is used to generate ±10 volts from a single +5 volt supply. The first stage doubles the +5V supply to +10 volts.. The second stage inverts the +10V potential to –10V. The ±10 volt supplies allow the DS233A to provide the necessary output levels for RS–232 communication. External charge pump capacitors are not necessary because the DS233A has internal capacitors.

RS–232 DRIVERS

The two RS–232 drivers are powered by the internal ±10 volt supplies generated by the on–board charge pump. The driver inputs are both TTL and CMOS compatible. Each input has an internal 400 kΩ pull–up resistor so that unused transmitter inputs can be left unconnected. The open circuit output voltage swing is from (V+ – 0.6) to V– volts. Worst case conditions for EIA–232E/V.28 of ±5 volt driving a 3 kΩ load and 2500 pF are met at maximum operating temperature and V_{CC} equal to 4.5 volts. Typical voltage swings of ±8 volts occur when loaded with a nominal 5 kΩ RS–232 receiver. As required by EIA–232E and V.28 specifications, the slew rate at the output is limited to less than 30 volts/µs. Typical slew rates are 20 volts/µs unloaded and 12 volts/µs with 3 kΩ and 2500 pF load. These slew rates allow for bit rates of over 250 kbits/s. Driver outputs maintain high impedance when power is off.

RS–232 RECEIVERS

The two receivers conform fully to the RS–232E specifications. The input impedance is typically 5 kΩ and can withstand up to ±25 volts with or without V_{CC} applied. The input switching thresholds are within the ±3 volt limit of RS–232E specification with an input threshold low of 0.8 volts and an input threshold high of 2.4 volts. The receivers have 0.5 volts of hysteresis (typical) to improve noise rejection. The TTL/CMOS compatible outputs of the receivers will be low whenever the RS–232 input is greater than 2.4 volts. The receiver output will be high when the input is floating or driven between +0.8 volts and –25 volts.

ABSOLUTE MAXIMUM RATINGS*

Absolute Maximum Ratings

V_{CC}	–0.3V to +7.0V
V+	(V_{CC}–0.3V) to +14V
V–	+0.3V to –14V

Input Voltages

T_{IN}	–0.3V to (V_{CC}+0.3V)
R_{IN}	±30V

Output Voltages

T_{OUT}	(V+ + 0.3V) to (V– – 0.3V)
R_{OUT}	–0.3V to (V_{CC} + 0.3V)
Short Circuit Duration, T_{OUT}	Continuous

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

The Dallas Semiconductor DS233A is built to the highest quality standards and manufactured for long term reliability. All Dallas Semiconductor devices are made using the same quality materials and manufacturing methods. Ho wever, the DS233A is not exposed to environmental stresses, such as burn–in. For specific reliability information on this product, please contact the factory in Dallas at (214) 450–0448.

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RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Votlage	V_{CC}	4.5		5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Current (No Load)	I_{CC1}		4	10	mA	
Power Supply Current (3 kΩ Load Both Outputs)	I_{CC2}		15		mA	
RS–232 Transmitters						
Output Voltage Swing	V_{ORS}	±5	±8		V	2
Input Logic Threshold Low	V_{TTL}	0.8	1.4		V	
Input Logic Threshold High	V_{TTH}		1.4	2.0	V	
Maximum Data Rate	f_D	250	350		kbits/s	

DC ELECTRICAL CHARACTERISTICS (continued)

(0°C to 70°C)

Logic Pull–up/Input Current	I_{PU}		5	40	µA	
Transmitter Output Resistance	R_{OUT}	300	10M		Ω	3
Output Short–Circuit Current	I_{TSC}	±15	±30	±100	mA	4
RS–232 Receivers						
RS–232 Input Voltage Operating Range	V_{IR}	±25	±30		V	
RS–232 Input Threshold Low	V_{RTL}	0.8	1.3		V	
RS–232 Input Threshold High	V_{RTH}		1.8	2.4	V	
RS–232 Input Hysteresis	V_{HY}	0.2	0.5	1	V	
RS–232 Input Resistance	R_{IN}	3	5	7	kΩ	
TTL/CMOS Output Voltage Low	V_{ROL}		0.2	0.4	V	5
TTL/CMOS Output Voltage High	V_{ROH}	3.5	V_{CC}–0.2		V	6
TTL/CMOS Output Short Circuit Current (V_{OUT}=GND)	I_{RSC}	–2	–10		mA	
TTL/CMOS Output Short Circuit Current (V_{OUT}=V_{CC})	I_{RSC}	10	30		mA	

AC ELECTRICAL CHARACTERISTICS

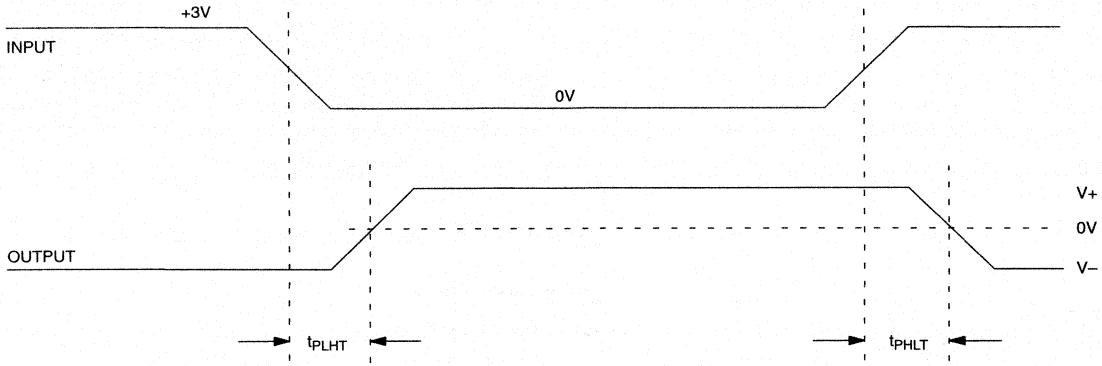
(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Transition Slew Rate	t_{SR}	6	12	30	V/µs	7
Transmitter Propagation Delay TTL to RS–232	t_{PHLT} t_{PLHT}		1.3 1.5	3.5 3.5	µs µs	
Receiver Propagation Delay RS–232 to TTL	t_{PHLR} t_{PLHR}		0.5 0.6	1 1	µs µs	
Transmitter + to – Propagation Delay Difference	t_{PHLT} $-t_{PLHT}$		300		ns	
Receiver + to – Propagation Delay Difference	t_{PHLR} $-t_{PLHR}$		100		ns	

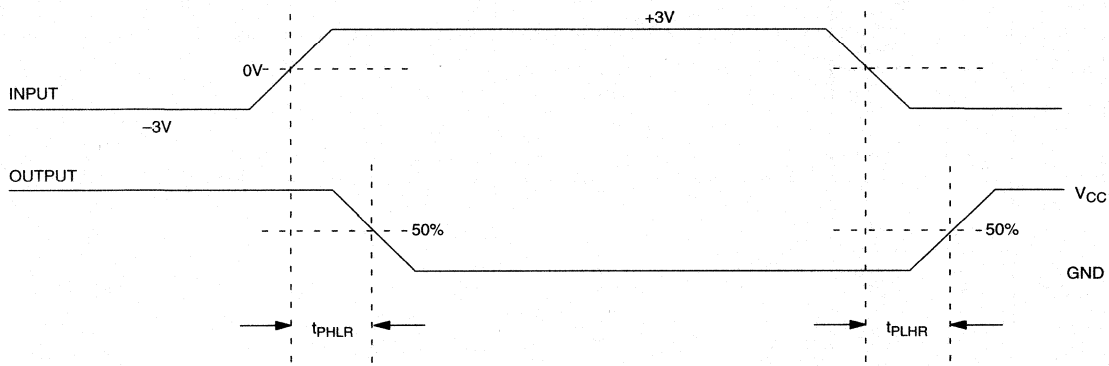
NOTES:

1. All voltages are referenced to ground.
2. All transmitter outputs loaded with 3 kΩ to ground.
3. V_{CC} = V+ = V– = 0V; V_{OUT} = ±2V .
4. V_{OUT} = 0V.
5. I_{OUT} = 3.2 mA.
6. I_{OUT} = –1.0 mA.
7. C_L = 50 pF – 2500 pF; RL = 3 kΩ – 7 kΩ; V_{CC} = 5V; TA = 25°C.

TRANSMITTER PROPAGATION DELAY TIMING Figure 3



RECEIVER PROPAGATION DELAY TIMING Figure 4



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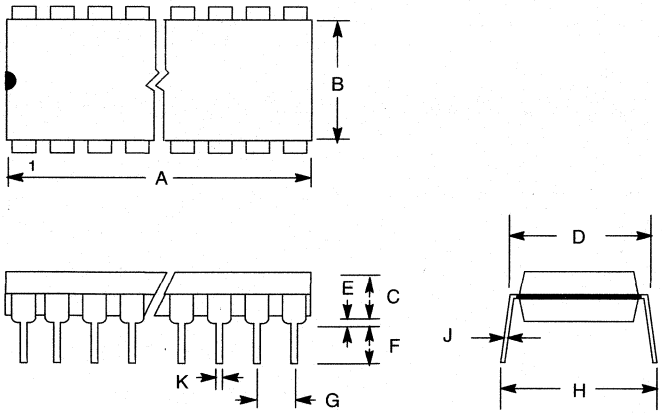
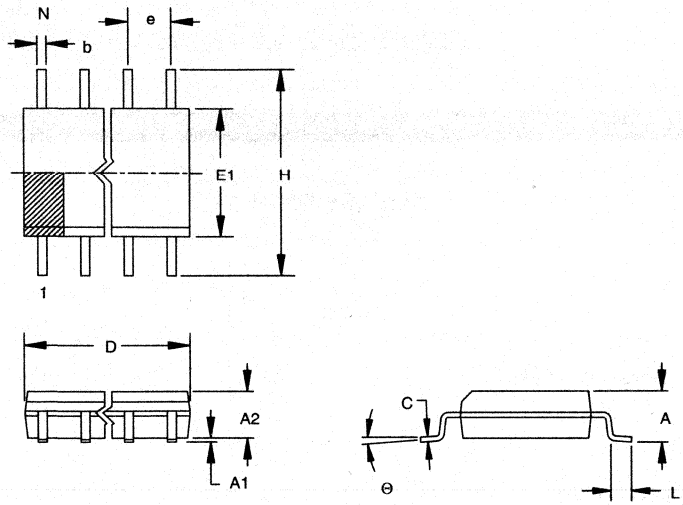
20–PIN DIP (300 MIL)



PKG	20-PIN	
DIM	MIN	MAX
A IN. MM	0.970 24.63	1.040 26.42
B IN. MM	0.240 6.09	0.270 6.86
C IN. MM	0.120 3.05	0.140 3.56
D IN. MM	0.295 7.49	0.325 8.26
E IN. MM	0.015 0.38	0.040 1.02
F IN. MM	0.120 3.04	0.140 3.56
G IN. MM	0.090 2.23	0.110 2.79
H IN MM	0.310 7.87	0.390 9.91
J IN MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53

20–PIN SOIC (300 MIL)



PKG	20-PIN	
DIM	MIN	MAX
A IN. MM	0.094 2.39	0.105 2.67
A1 IN. MM	0.004 0.102	0.012 0.30
A2 IN. MM	0.089 2.26	0.095 2.41
b IN. MM	0.013 0.33	0.020 0.51
C IN. MM	0.009 0.229	0.013 0.33
D IN. MM	0.498 12.65	0.511 12.99
e IN. MM	0.050 BSC 1.27 BSC	
E1 IN MM	0.290 7.37	0.300 7.62
H IN MM	0.398 10.11	0.416 10.57
L IN. MM	0.016 0.40	0.040 1.02
Θ	0°	8°

5

PRELIMINARY

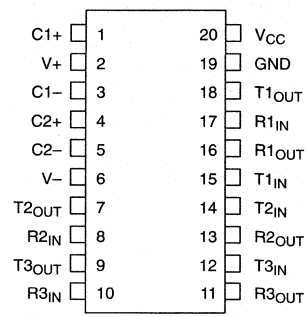
DALLAS SEMICONDUCTOR

DS229
Triple RS–232 Transmitter/Receiver

FEATURES

- Compatible with DS1229
- 5V operation
- 20–pin DIP or SOIC package
- 20–pin TSSOP package for height restricted applications
- Operate from single +5V power
- Meets all EIA–232E and V.28 specifications
- Uses small capacitors: 0.1 µF
- Optional industrial temperature range available (–40°C to +85°C)

PIN ASSIGNMENT



20–PIN DIP, SOIC AND TSSOP

PIN DESCRIPTION

V_{CC}	– +5 Volt Supply
GND	– Ground
V+	– Positive Supply Output
V–	– Negative Supply Output
$T1_{IN}$, $T2_{IN}$, $T3_{IN}$	– RS–232 Driver Inputs
$T1_{OUT}$, $T2_{OUT}$, $T3_{OUT}$	– RS–232 Driver Outputs
$R1_{IN}$, $R2_{IN}$, $R3_{IN}$	– Receiver Inputs
$R1_{OUT}$, $R2_{OUT}$, $R3_{OUT}$	– Receiver Outputs
C1+, C1–	– Capacitor 1 Connections
C2+, C2–	– Capacitor 2 Connections

ORDERING INFORMATION

DS229	20–pin DIP
DS229N	20–pin DIP (Industrial)
DS229S	20–pin SOIC
DS229SN	20–pin SOIC (Industrial)
DS229E	20–pin TSSOP
DS229EN	20–pin TSSOP (Industrial)

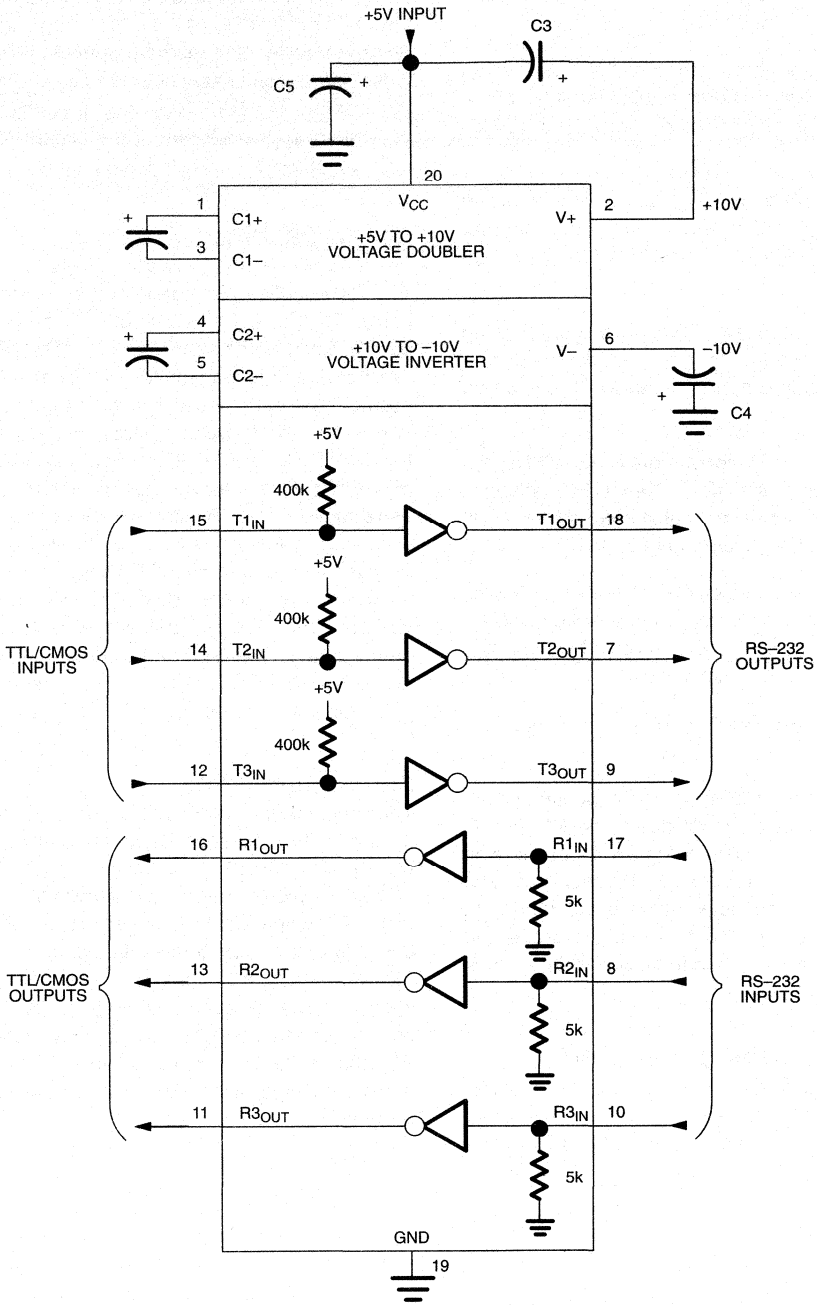
DESCRIPTION

The DS229 is a triple RS–232 driver/receiver pair that generates RS–232 voltage levels from a single +5 volt power supply. Additional ±12 volt supplies are not needed since the DS229 uses on–board charge pumps to convert the +5 volt supply to ±10 volts. The DS229 is fully compliant with EIA RS–232E and V.28/V.24 standards. The DS229 contains three drivers and three receivers. Driver slew rates and data rates are guaranteed up to 116 kbits/sec. The DS229 operates with only 0.1 µF charge pump capacitors.

OPERATION

The diagram in Figure 1 shows the main elements of the DS229. The following paragraphs describe the function of each pin.

FUNCTIONAL DIAGRAM OF DS229 Figure 1



NOTE: C5 is a recommended decoupling capacitor which is the same value as C1, C2, C3, and C4.

PIN DESCRIPTIONS

V_{CC}, GND: DC power is provided to the device on these pins. V_{CC} is the +5 volt input.

V+: Positive supply output (RS–232). V+ requires an external storage charge capacitor of at least 0.1 µF. A larger capacitor (up to 10 µF) can be used to reduce supply ripple.

V–: Negative supply output (RS–232). V– requires an external storage capacitor of at least 0.1 µF. A larger capacitor (up to 10 µF) can be used to reduce supply ripple.

$T1_{IN}$, $T2_{IN}$, $T3_{IN}$: Standard TTL/CMOS inputs for the RS–232 drivers. The inputs of unused drivers can be left unconnected since each input has a 400 kΩ pull–up resistor.

$T1_{OUT}$, $T2_{OUT}$, $T3_{OUT}$: Driver outputs at RS–232 levels. Driver output swing meets RS–232 levels for loads up to 3 kΩ. These driver outputs provide current necessary to meet RS–232 levels for loads up to 2500 pF.

$R1_{IN}$, $R2_{IN}$, $R3_{IN}$: Receiver inputs. These inputs accept RS–232 level signals (±25 volts) into a protected 5 kΩ terminating resistor. Each receiver provides 0.5V hysteresis (typical) for noise immunity.

$R1_{OUT}$, $R2_{OUT}$, $R3_{OUT}$: Receiver outputs at TTL/CMOS levels.

C1+, C1–, C2+, C2–: Charge pump capacitor inputs. These pins require two external capacitors (0.1 µF minimum, 10 µF maximum and should be the same size as C3 and C4). Capacitor 1 is connected between C1+ and C1–. Capacitor 2 is connected between C2+ and C2–. Capacitor C1 can be omitted if +12 volts is connected directly to V+. Likewise, C2 can be omitted if –12V is connected directly to V–.

DUAL CHARGE PUMP CONVERTERS

The DS229 has a two stage on–board charge pump circuit that is used to generate ±10 volts from a single +5 volt supply. In the first stage, capacitor C1 doubles the +5V supply to +10 volts which is then stored on capacitor C3. The second stage uses capacitor C2 to invert the +10V potential to –10V. This charge is then stored on capacitor C4. The ±10 volt supplies allow the DS229 to provide the necessary output levels for RS–232 communication. The DS229 will operate with charge pump capacitors as low as 0.1 µF. Larger capacitors (up to 10 µF) can be used to reduce supply ripple.

RS–232 DRIVERS

The three RS–232 drivers are powered by the internal ±10 volt supplies generated by the on–board charge pump. The driver inputs are both TTL and CMOS compatible. Each input has an internal 400 kΩ pull–up resistor so that unused transmitter inputs can be left unconnected. The open circuit output voltage swing is from (V+ – 0.6) to V– volts. Worst case conditions for EIA–232E/V.28 of ±5 volt driving a 3 kΩ load and 2500 pF are met at maximum operating temperature and V_{CC} equal to 4.5 volts. Typical voltage swings of ±8 volts occur when loaded with a nominal 5 kΩ RS–232 receiver. As required by EIA–232E and V.28 specifications, the slew rate at the output is limited to less than 30 volts/µs. Typical slew rates are 20 volts/µs unloaded and 12 volts/µs with 3 kΩ and 2500 pF load. These slew rates allow for bit rates of over 116 kbits/s. Driver outputs maintain high impedance when power is off.

RS–232 RECEIVERS

The three receivers conform fully to the RS–232E specifications. The input impedance is typically 5 kΩ and can withstand up to ±30 volts with or without V_{CC} applied. The input switching thresholds are within the ±3 volt limit of RS–232E specification with an input threshold low of 0.8 volts and an input threshold high of 2.4 volts. The receivers have 0.5 volts of hysteresis (typical) to improve noise rejection. The TTL/CMOS compatible outputs of the receivers will be low whenever the RS–232 input is greater than 2.4 volts. The receiver output will be high when the input is floating or driven between +0.8 volts and –25 volts.

ABSOLUTE MAXIMUM RATINGS*

Absolute Maximum Ratings

V_{CC}	–0.3V to +7.0V
V+	(V_{CC}–0.3V) to +14V
V–	+0.3V to –14V
Input Voltages	
T_{IN}	–0.3V to (V_{CC}+0.3V)
R_{IN}	±30V
Output Voltages	
T_{OUT}	(V+ + 0.3V) to (V– – 0.3V)
R_{OUT}	–0.3V to (V_{CC} + 0.3V)
Short Circuit Duration, T_{OUT}	Continuous

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Votlage	V_{CC}	4.5		5.5	V	1

5

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Current (No Load)	I_{CC1}		6	15	mA	
Power Supply Current (3 kΩ Load Both Outputs)	I_{CC2}		22.5		mA	
RS–232 Transmitters						
Output Voltage Swing	V_{ORS}	±5	±8		V	2
Input Logic Threshold Low	V_{TTL}	0.8	1.4		V	
Input Logic Threshold High	V_{TTH}		1.4	2.0	V	
Data Rate	f_D		200	116	kbits/s	
Logic Pull–up/Input Current	I_{PU}		5	40	µA	
Transmitter Output Resistance	R_{OUT}	300	10M		Ω	3
Output Short–Circuit Current	I_{TSC}	±15	±30	±100	mA	4

DC ELECTRICAL CHARACTERISTICS (continued) (0°C to 70°C)

RS–232 Receivers						
RS–232 Input Voltage Operating Range	V_{IR}	±25	±30		V	
RS–232 Input Threshold Low	V_{RTL}	0.8	1.3		V	
RS–232 Input Threshold High	V_{RTH}		1.8	2.4	V	
RS–232 Input Hysteresis	V_{HY}	0.2	0.5	1	V	
RS–232 Input Resistance	R_{IN}	3	5	7	kΩ	
TTL/CMOS Output Voltage Low	V_{ROL}		0.2	0.4	V	5
TTL/CMOS Output Voltage High	V_{ROH}	3.5	V_{CC}–0.2		V	6
TTL/CMOS Output Short Circuit Current (V_{OUT}=GND)	I_{RSC}	–2	–10		mA	
TTL/CMOS Output Short Circuit Current (V_{OUT}=V_{CC})	I_{RSC}	10	30		mA	

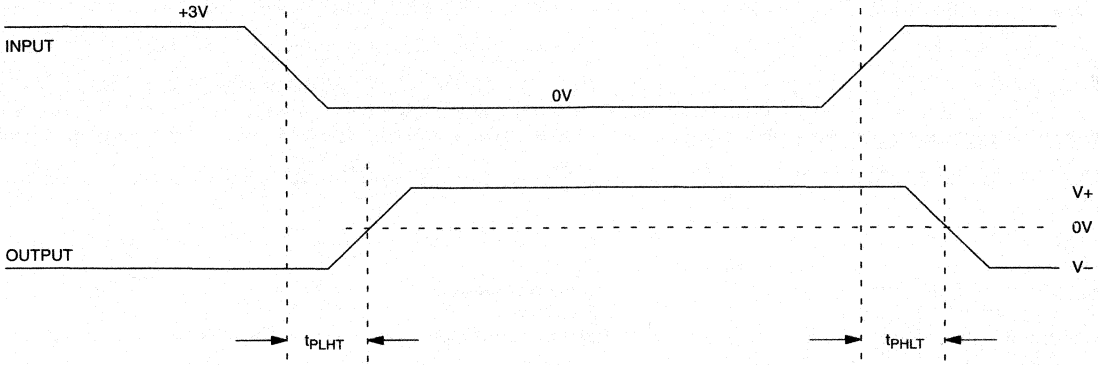
AC ELECTRICAL CHARACTERISTICS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Transition Slew Rate	t_{SR}	6	12	30	V/µs	7
Transmitter Propagation Delay TTL to RS–232	t_{PHLT} t_{PLHT}		1.3 1.5	3.5 3.5	µs µs	
Receiver Propagation Delay RS–232 to TTL	t_{PHLR} t_{PLHR}		0.5 0.6	1 1	µs µs	
Transmitter + to – Propagation Delay Difference	t_{PHLT} $-t_{PLHT}$		300		ns	
Receiver + to – Propagation Delay Difference	t_{PHLR} $-t_{PLHR}$		100		ns	

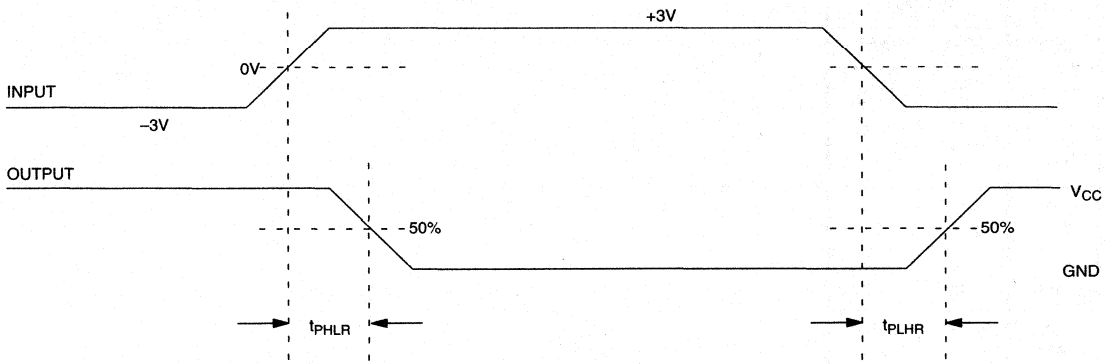
NOTES:

1. All voltages are referenced to ground.
2. All transmitter outputs loaded with 3 kΩ to ground.
3. V_{CC} = V+ = V– = 0V; V_{OUT} = ±2V .
4. V_{OUT} = 0V.
5. I_{OUT} = 3.2 mA.
6. I_{OUT} = –1.0 mA.
7. C_L = 50 pF – 2500 pF; RL = 3 kΩ – 7 kΩ; V_{CC} = 5V; TA = 25°C.

TRANSMITTER PROPAGATION DELAY TIMING Figure 2

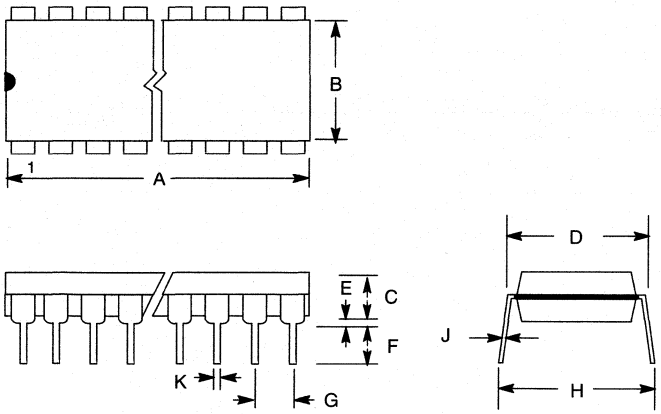


RECEIVER PROPAGATION DELAY TIMING Figure 3



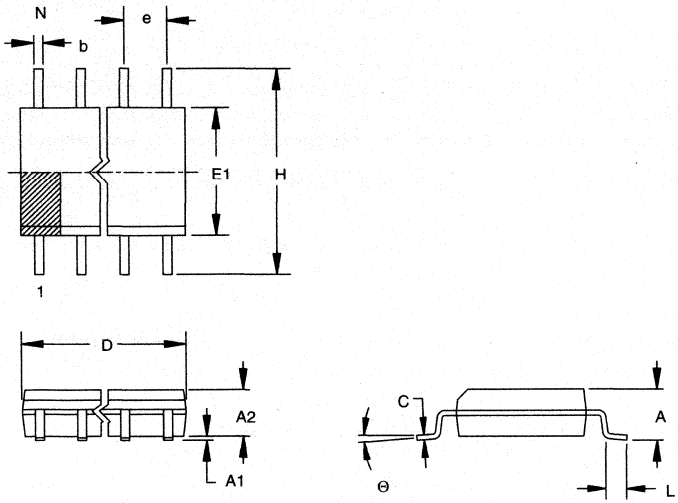
5

20–PIN DIP (300 MIL)



PKG	20-PIN	
DIM	MIN	MAX
A IN. MM	0.970 24.63	1.040 26.42
B IN. MM	0.240 6.09	0.270 6.86
C IN. MM	0.120 3.05	0.140 3.56
D IN. MM	0.295 7.49	0.325 8.26
E IN. MM	0.015 0.38	0.040 1.02
F IN. MM	0.120 3.04	0.140 3.56
G IN. MM	0.090 2.23	0.110 2.79
H IN MM	0.310 7.87	0.390 9.91
J IN MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53

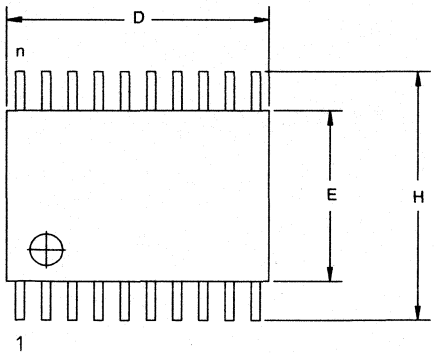
20–PIN SOIC (300 MIL)

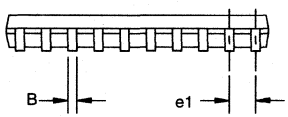


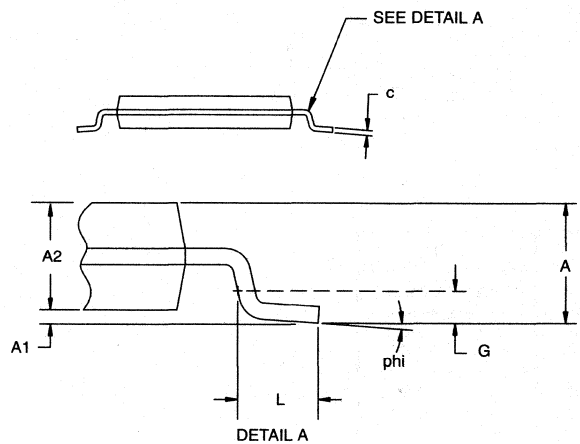
PKG	20-PIN	
DIM	MIN	MAX
A IN. MM	0.094 2.39	0.105 2.67
A1 IN. MM	0.004 0.102	0.012 0.30
A2 IN. MM	0.089 2.26	0.095 2.41
b IN. MM	0.013 0.33	0.020 0.51
C IN. MM	0.009 0.229	0.013 0.33
D IN. MM	0.498 12.65	0.511 12.99
e IN. MM	0.050 BSC 1.27 BSC	
E1 IN MM	0.290 7.37	0.300 7.62
H IN MM	0.398 10.11	0.416 10.57
L IN. MM	0.016 0.40	0.040 1.02
Θ	0°	8°

5

20-PIN TSSOP







DIM	MIN	MAX
A MM	–	1.10
A1 MM	0.05	–
A2 MM	0.75	1.05
C MM	0.09	0.18
L MM	0.50	0.70
e1 MM	0.65 BSC	
B MM	0.18	0.30
D MM	6.40	6.90
E MM	4.40 NOM	
G MM	0.25 REF	
H MM	6.25	6.55
phi	0°	8°

NONVOLATILE CONTROLLERS

6

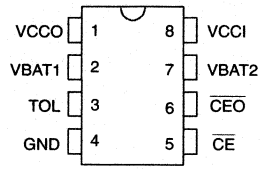
DALLAS SEMICONDUCTOR

DS1210
Nonvolatile Controller Chip

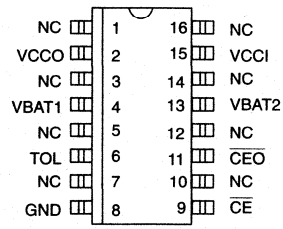
FEATURES

- Converts CMOS RAMs into nonvolatile memories
- Unconditionally write protects when V_{CC} is out of tolerance
- Automatically switches to battery when power fail occurs
- Space saving 8-pin DIP
- Consumes less than 100 nA of battery current
- Tests battery condition on power up
- Provides for redundant batteries
- Optional 5% or 10% power fail detection
- Low forward voltage drop on the V_{CC} switch
- Optional 16-pin SOIC surface mount package
- Optional industrial temperature range of -40°C to +85°C.

PIN ASSIGNMENT



DS1210 8-Pin DIP (300 MIL)
See Mech. Drawings Section



DS1210S 16-Pin SOIC (300 MIL)
See Mech. Drawings Section

PIN DESCRIPTION

V_{CCO}	–	RAM Supply
V_{BAT1}	–	+ Battery 1
TOL	–	Power Supply Tolerance
GND	–	Ground
$\overline{CE}$	–	Chip Enable Input
$\overline{CEO}$	–	Chip Enable Output
V_{BAT2}	–	+ Battery 2
V_{CCI}	–	+ Supply
NC	–	No Connect

DESCRIPTION

The DS1210 Nonvolatile Controller Chip is a CMOS circuit which solves the application problem of converting CMOS RAM into nonvolatile memory. Incoming power is monitored for an out-of-tolerance condition. When such a condition is detected, chip enable is inhibited to accomplish write protection and the battery is switched on to supply the RAM with uninterrupted power. Special circuitry uses a low-leakage CMOS process which affords precise voltage detection at extremely low battery consumption. The 8-pin DIP package keeps PC board real estate requirements to a minimum. By combining the DS1210 Nonvolatile Controller Chip with a CMOS memory and batteries, nonvolatile RAM operation can be achieved.

OPERATION

The DS1210 nonvolatile controller performs five circuit functions required to battery back up a RAM. First, a switch is provided to direct power from the battery or the incoming supply (V_{CCI}) depending on which is greater. This switch has a voltage drop of less than 0.3V. The second function which the nonvolatile controller provides is power fail detection. The DS1210 constantly monitors the incoming supply. When the supply goes out of tolerance a precision comparator detects power fail and inhibits chip enable ($\overline{CEO}$). The third function of write protection is accomplished by holding the $\overline{CEO}$ output signal to within 0.2 volts of the V_{CCI} or battery supply. If $\overline{CE}$ input is low at the time power fail detection occurs, the $\overline{CEO}$ output is kept in its present state until $\overline{CE}$ is returned high. The delay of write protection until the current memory cycle is completed prevents the corruption of data. Power fail detection occurs in the range of 4.75 volts to 4.5 volts with the tolerance Pin 3 grounded. If Pin 3 in connected to V_{CCO}, then power fail detection occurs in the range of 4.5 volts to 4.25 volts. During nominal supply conditions $\overline{CEO}$ will follow $\overline{CE}$ with a maximum propagation delay of 20ns. The fourth function the DS1210 performs is a battery status warning so that potential data loss is avoided. Each time that the circuit is powered up the battery voltage is checked with a precision comparator. If the battery voltage is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in memory, verifying that memory location content. A subsequent write cycle can then be executed to the same memory location altering the data. If the next read cycle fails to verify the written data, then the batteries are less than 2.0V and data is in danger of being corrupted. The fifth function of the nonvolatile controller provides for battery redundancy. In many applications, data integrity is paramount. In these applications it is often desirable to use two batteries to ensure reliability. The DS1210 controller provides an internal isolation switch which allows the connection of two batteries. During battery backup operation the battery with the highest voltage is selected for use. If one battery should fail, the other will take over the load. The switch to a redundant battery is transparent to circuit operation and to the user. A battery status warning will occur when the battery in use falls below 2.0 volts. A grounded V_{BAT2} pin will not activate a battery fail warning. In applications where battery redundancy is not required, a single battery should be connected to the BAT1 pin. The BAT2 battery pin must be grounded. The nonvolatile controller contains circuitry to turn off the battery back-up. This is to maintain the battery(s) at its highest capacity until the equipment is powered up and valid data is written to the SRAM. While in the freshness seal mode the $\overline{CEO}$ and V_{CCO} will be forced to V_{OL}. When the batteries are first attached to one or both of the V_{BAT} pins, V_{CCO} will not provide battery back-up until V_{CCI} exceeds V_{CCTP}, as set by the T_{OL} pin, and then falls below V_{BAT}.

Figure 1 shows a typical application incorporating the DS1210 in a microprocessor-based system. Section A shows the connections necessary to write protect the RAM when V_{CC} is less than 4.75 volts and to back up the supply with batteries. Section B shows the use of the DS1210 to halt the processor when V_{CC} is less than 4.75 volts and to delay its restart on power- up to prevent spurious writes.

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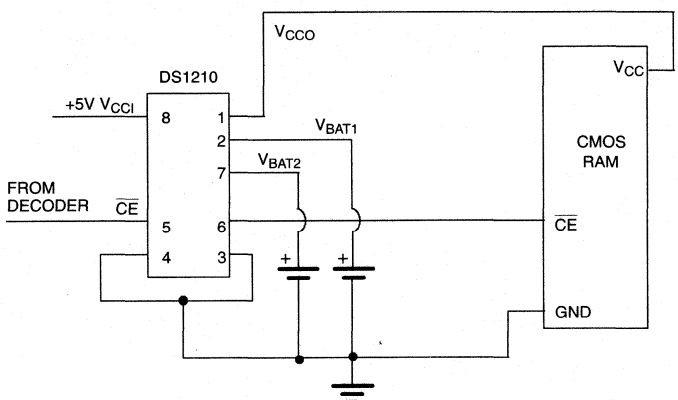
SECTION A – BATTERY BACKUP Figure 1

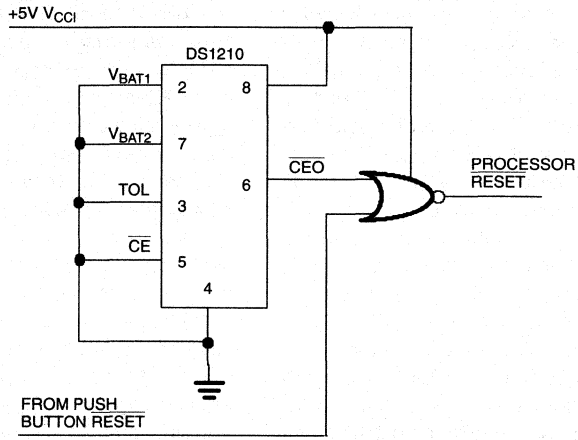


BATTERY BACKUP CURRENT DRAIN EXAMPLE

CONSUMPTION

DS1210 I_{BAT}	100 nA
RAM I_{CC02}	10 µA
Total Drain	10.1 µA

SECTION B - PROCESSOR RESET



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pin 3 = GND Supply Voltage	V_{CCI}	4.75	5.0	5.5	V	1
Pin 3 = V_{CCO} Supply Voltage	V_{CCI}	4.5	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.2		V_{CC}+0.3	V	1
Logic 0 Input	V_{IL}	-0.3		+0.8	V	1
Battery Input	V_{BAT1}, V_{BAT2}	2.0		4.0	V	1,2

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CCI} = 4.75V to 5.5V, PIN 3 = GND)
(V_{CCI} = 4.5 to 5.5V, PIN 3 = V_{CCO})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CCI}			5	mA	3
Supply Voltage	V_{CCO}	V_{CC}-0.2			V	1
Supply Current	I_{CCO1}			80	mA	4
Input Leakage	I_{IL}	-1.0		+1.0	µA	
Output Leakage	I_{LO}	-1.0		+1.0	µA	
$\overline{CEO}$ Output @2.4V	I_{OH}	-1.0			mA	5
$\overline{CEO}$ Output @0.4V	I_{OL}			4.0	mA	5
V_{CC} Trip Point (TOL=GND)	V_{CCTP}	4.50	4.62	4.74	V	1
V_{CC} Trip Point (TOL=V_{CCO})	V_{CCTP}	4.25	4.37	4.49	V	1

(0°C to 70°C; V_{CCI} = < V_{BAT})

$\overline{CEO}$ Output	V_{OHL}	V_{BAT}-0.2			V	7
V_{BAT1} or V_{BAT2} Battery Current	I_{BAT}			100	nA	2,3
Battery Backup Current @ V_{cco} = V_{BAT} - 0.3V	I_{CCO2}			50	µA	6,7

6

CAPACITANCE

(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CCI} = 4.75V to 5.5V, PIN 3 = GND)
(V_{CCI} = 4.5 to 5.5V, PIN3 = V_{CCO})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ Propagation Delay	t_{PD}	5	10	20	ns	5
$\overline{CE}$ High to Power Fail	t_{PF}			0	ns	

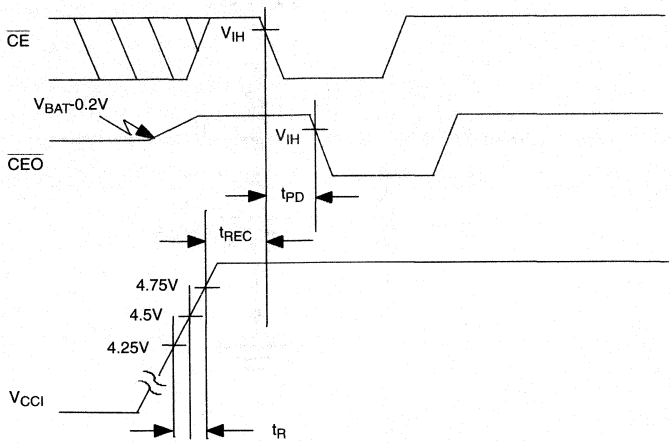
(0°C to 70°C; V_{CCI} < 4.75V, PIN 3 = GND; V_{CCI} < 4.5, PIN 3 = V_{CCO})

Recovery at Power Up	t_{REC}	2	80	125	ms	
V_{CC} Slew Rate Power Down	t_F	300			µs	
V_{CC} Slew Rate Power Down	t_{FB}	10			µs	
V_{CC} Slew Rate Power Up	t_R	0			µs	
$\overline{CE}$ Pulse Width	t_{CE}			1.5	µs	8

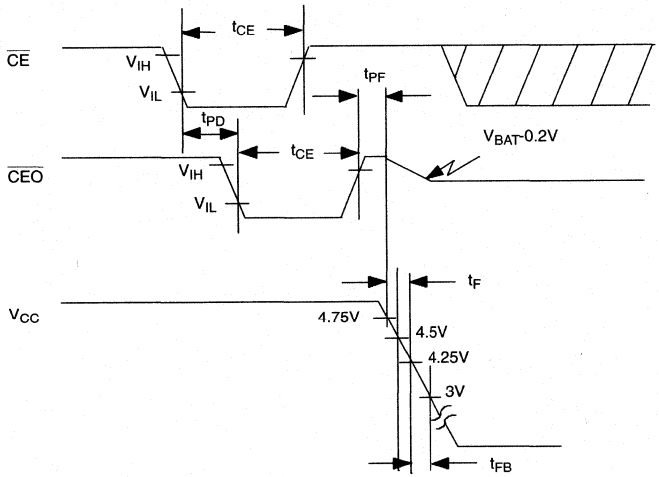
NOTES:

1. All voltages are referenced to ground.
2. Only one battery input is required. Unused battery inputs must be grounded.
3. Measured with V_{CCO} and $\overline{CEO}$ open.
4. I_{CC01} is the maximum average load which the DS1210 can supply to the memories.
5. Measured with a load as shown in Figure 2.
6. I_{CC02} is the maximum average load current which the DS1210 can supply to the memories in the battery backup mode.
7. t_{CE} max. must be met to ensure data integrity on power loss.
8. $\overline{CEO}$ can only sustain leakage current in the battery backup mode.

TIMING DIAGRAM: POWER UP



TIMING DIAGRAM: POWER DOWN



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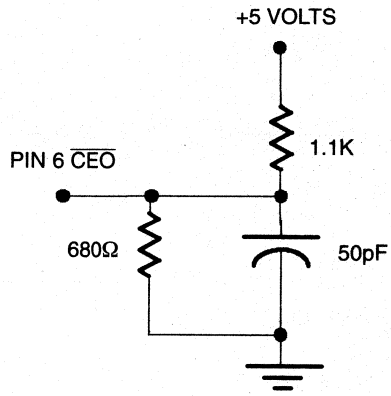
OUTPUT LOAD Figure 2



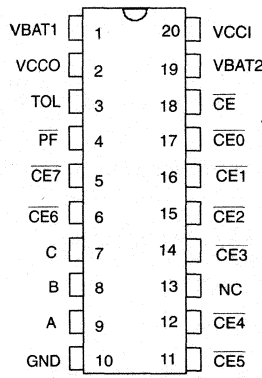
DALLAS SEMICONDUCTOR

DS1211
Nonvolatile Controller x 8 Chip

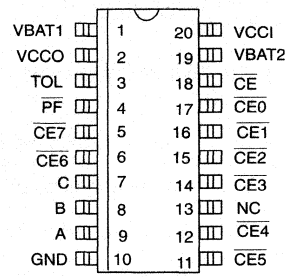
FEATURES

- Converts full CMOS RAMs into nonvolatile memories
- Unconditionally write protects when V_{CC} is out of tolerance
- Automatically switches to battery when power fail occurs
- 3 to 8 decoder provides control for up to eight CMOS RAMs
- Consumes less than 100 nA of battery current
- Tests battery condition on power-up
- Provides for redundant batteries
- Power fail signal can be used to interrupt processor on power failure
- Optional 5% or 10% power fail detection
- Optional 20-pin SOIC surface mount package
- Optional industrial temperature range of -40°C to +85°C

PIN ASSIGNMENT



20-Pin DIP (300 MIL)
See Mech. Drawings Section



20-Pin SOIC (300 MIL)
See Mech. Drawings Section

PIN DESCRIPTION

A, B, C	–	Address Inputs
$\overline{CE}$	–	Chip Enable Input
$\overline{CE0}$ - $\overline{CE7}$	–	Chip Enable Outputs
GND	–	Ground
V_{BAT1}	–	+ Battery 1
V_{BAT2}	–	+ Battery 2
TOL	–	Power Supply Tolerance
V_{CCI}	–	+5V Supply
V_{CCO}	–	RAM Supply
$\overline{PF}$	–	Power Fail
NC	–	No Connection

6

DESCRIPTION

The DS1211 Nonvolatile Controller x 8 Chip is a CMOS circuit which solves the application problem of converting CMOS RAMs into nonvolatile memories. Incoming power is monitored for an out-of-tolerance condition. When such a condition is detected, the chip enables are inhibited to accomplish write protection and the battery is switched on to supply RAMs with uninterrupted power. Special circuitry uses a low-leakage CMOS process which affords precise voltage detection at extremely low battery consumption.

By combining the DS1211 nonvolatile controller/decoder chip and lithium batteries, nonvolatile RAM operation can be achieved for up to eight CMOS memories.

See the data sheet for the DS1212 Nonvolatile Controller x 16 Chip for electrical specifications and operation.

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DALLAS SEMICONDUCTOR

DS1212
Nonvolatile Controller x 16 Chip

FEATURES

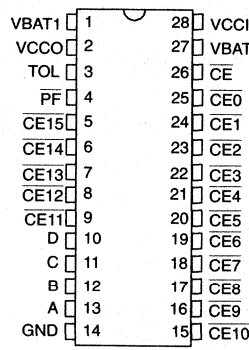
- Converts full CMOS RAM into nonvolatile memory
- Unconditionally write protects when V_{CC} is out of tolerance
- Automatically switches to battery when power fail occurs
- 4 to 16 decoder provides control for up to 16 CMOS RAMs
- Consumes less than 100 nA of battery current
- Tests battery condition on power-up
- Provides for redundant batteries
- Power fail signal can be used to interrupt processor on power failure
- Optional 5% or 10% power fail detection
- Optional 28-pin PLCC surface mount package
- Optional industrial temperature range of -40°C to +85°C

DESCRIPTION

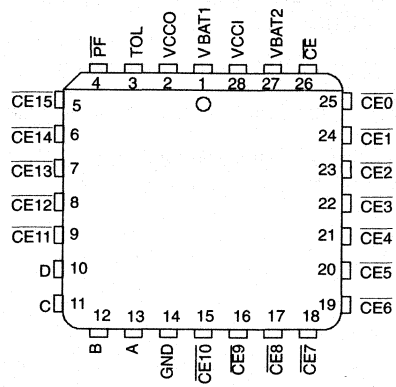
The DS1212 Nonvolatile Controller x16 Chip is a CMOS circuit that solves the application problem of converting CMOS RAMs into nonvolatile memories. Incoming power is monitored for an out-of-tolerance condition. When such a condition is detected, the chip enables are inhibited to accomplish write protection and the battery is switched on to supply the RAMs with uninterrupted power. Special circuitry uses a low-leakage CMOS process that affords precise voltage detection at extremely low battery consumption.

By combining the DS1212 Nonvolatile Controller chip and lithium batteries, nonvolatile RAM operation can be achieved for up to 16 CMOS memories.

PIN ASSIGNMENT



28-Pin DIP (600 MIL)
See Mech. Drawings Section



28-Pin PLCC
See Mech. Drawings Section

PIN DESCRIPTION

A, B, C, D	–	Address Inputs
$\overline{CE}$	–	Chip Enable
$\overline{CE0}$-$\overline{CE15}$	–	Chip Enable Outputs
GND	–	Ground
V_{BAT1}	–	+ Battery 1
V_{BAT2}	–	+ Battery 2
TOL	–	Power Supply Tolerance
V_{CCI}	–	+5V Supply
V_{CCO}	–	RAM Supply
$\overline{PF}$	–	Power Fail

OPERATION

The DS1212 performs six circuit functions required to decode and battery back up a bank of up to 16 RAMs. First, the 4 to 16 decoder provides selection of one of 16 RAMs. Second, a switch is provided to direct power from the battery or V_{CCI} supply, depending on which is greater. This switch has a voltage drop of less than 0.2V. The third function the DS1212 provides is power fail detection. It constantly monitors the V_{CCI} supply. When V_{CCI} falls below 4.75 volts, or 4.5 volts, depending o n the level of tolerance Pin 3, a precision comparator outputs a power fail detect signal to the decoder/chip enable logic and the $\overline{PF}$ signal is driven low. The $\overline{PF}$ signal will remain low until V_{CCI} is back in normal limits.

The fourth function of write protection is accomplished by holding all chip enable outputs ($\overline{CE0}$-$\overline{CE15}$) to within 0.2 volts of V_{CCI} or battery supply. If $\overline{CE}$ is low at the time power fail detection occurs, the chip enable outputs are kept in their present state until $\overline{CE}$ is driven high. The delay of write protection until the current memory cycle is completed prevents corruption of data. Power fail detection occurs in the range of 4.75 volts to 4.5 volts with tolerance Pin 3 grounded. If Pin 3 is connected to V_{CCO}, then power fail occurs in the range of 4.5 volts to 4.25 volts. During nominal supply conditions the chip enable outputs follow the logic of a 4-to-16 decoder, shown in Figure 1.

The fifth function the DS1212 performs is a battery status warning so that data loss is avoided. Each time the circuit is powered up, the battery voltage is checked with a precision comparator. If the battery voltage is less than 2 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in memory, verifying that memory location content. A subsequent write cycle can then be executed to the same memory location, altering the data. If the next read cycle fails to verify the written data, then the batteries are less than 2.0 volts and data is in danger of being corrupted.

The sixth function of the DS1212 provides for battery redundancy. In many applications, data integrity is paramount. In these applications it is often desirable to use two batteries to ensure reliability. The DS1212 provides an internal isolation switch which allows the connection of two batteries during battery backup operation. The battery with the highest voltage is selected for use. If one battery should fail, the other will then assume the load. The switch to a redundant battery is transparent to circuit operation and the user. A battery status warning will only occur if both batteries are less than 2.0 volts. For single battery applications the unused battery input must be grounded.

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NONVOLATILE CONTROLLER/DECODER Figure 1

INPUTS					OUTPUTS															
$\overline{CE}$	D	C	B	A	$\overline{CE0}$	$\overline{CE1}$	$\overline{CE2}$	$\overline{CE3}$	$\overline{CE4}$	$\overline{CE5}$	$\overline{CE6}$	$\overline{CE7}$	$\overline{CE8}$	$\overline{CE9}$	$\overline{CE10}$	$\overline{CE11}$	$\overline{CE12}$	$\overline{CE13}$	$\overline{CE14}$	$\overline{CE15}$	$\overline{PF}$
H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H

H = High Level
L = Low Level
X = Irrelevant
NOTE: V_{CCI} input is 250 mV lower when TOL PIN3 = V_{CCO}.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 3 = GND Supply Voltage	V_{CCI}	4.75	5.0	5.5	V	1
PIN 3 = V_{CCO} Supply Voltage	V_{CCO}	4.5	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.2		V_{CC}+0.3	V	1
Logic 0 Input	V_{IL}	-0.3		+0.8	V	1
Battery Input	V_{BAT1}, V_{BAT2}	2.0		4.0	V	1,2

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CCI} = 4.75 to 5.5V, PIN 3 = GND)
(0°C to 70°C; V_{CCI} = 4.5 to 5.5V, PIN3 = V_{CCO})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CCI}			5	mA	3
Supply Current @ V_{CCO}= V_{CCI}-0.2	I_{CCO1}			80	mA	1,4,10
Input Leakage	I_{IL}	-1.0		+1.0	µA	
Output Leakage	I_{LO}	-1.0		+1.0	µA	
$\overline{CE0}$-$\overline{CE15}$,$\overline{PF}$ Output @ 2.4V	I_{OH}	-1.0			mA	5
$\overline{CE0}$-$\overline{CE15}$,$\overline{PF}$ Output @ 0.4V	I_{OL}			4.0	mA	5
V_{CC} Trip Point (TOL = GND)	V_{CCTP}	4.50	4.62	4.74	V	1
V_{CC} Trip Point (TOL = V_{CCO})	V_{CCTP}	4.25	4.37	4.49	V	1

(0°C to 70°C; V_{CCI} < V_{BAT})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE0}$-CE15 Output	V_{OHL}	V_{BAT}-0.2			V	3,7
Battery Current	I_{BAT}			0.1	µA	2,3
Battery Backup Current @ V_{CCO}=V_{BAT1}-0.5V	I_{CC2}			100	µA	6,10,11

CAPACITANCE

(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CCI} = 4.75 to 5.5V, PIN 3 = GND)
(0°C to 70°C; V_{CCI} = 4.5 to 5.5V, PIN 3 = V_{CCO})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ Propagation Delay	t_{PD}	5	10	20	ns	5
$\overline{CE}$ High to Power Fail	t_{PF}			0	ns	
Address Setup	t_{AS}	20			ns	9

(0°C to 70°C; V_{CCI} < 4.75V, PIN 3 = GND)
(0°C to 70°C; V_{CCI} < 4.5V, PIN 3 = V_{CCO})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power-Up	t_{REC}	2	80	125	ms	
V_{CC} Slew Rate Power-Down	t_F	300			µs	
V_{CC} Slew Rate Power-Down	t_{FB}	10			µs	
V_{CC} Slew Rate Power-Up	t_R	0			µs	
$\overline{CE}$ Pulse Width	t_{CE}			1.5	µs	7,8
Power Fail to $\overline{PF}$ Low	t_{PFL}	300			µs	

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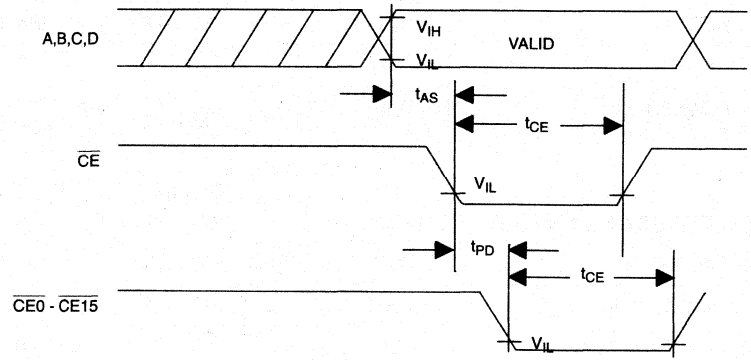
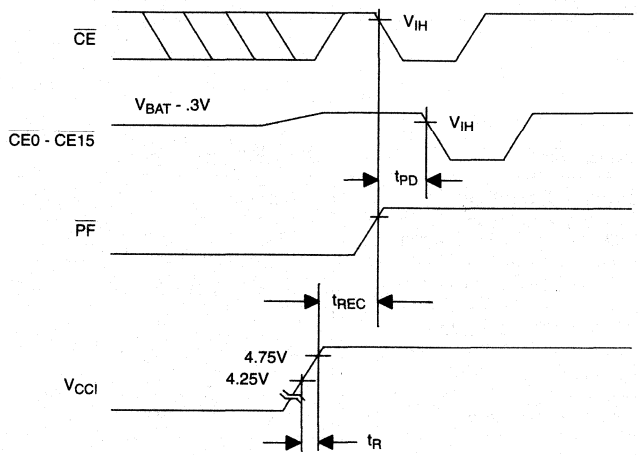
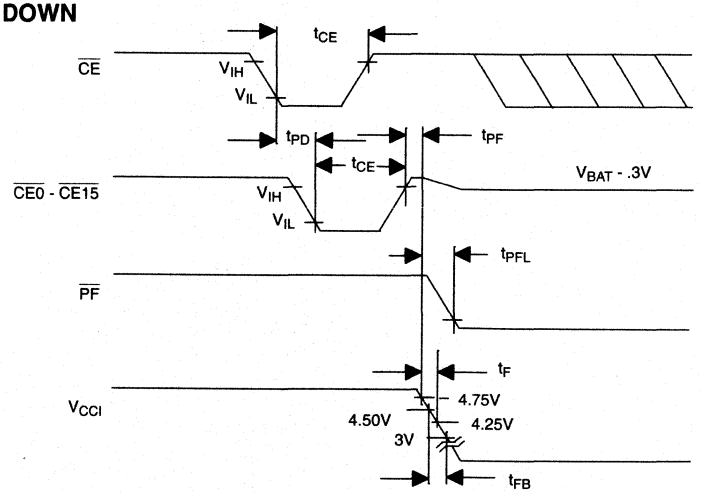
TIMING DIAGRAM: DECODER



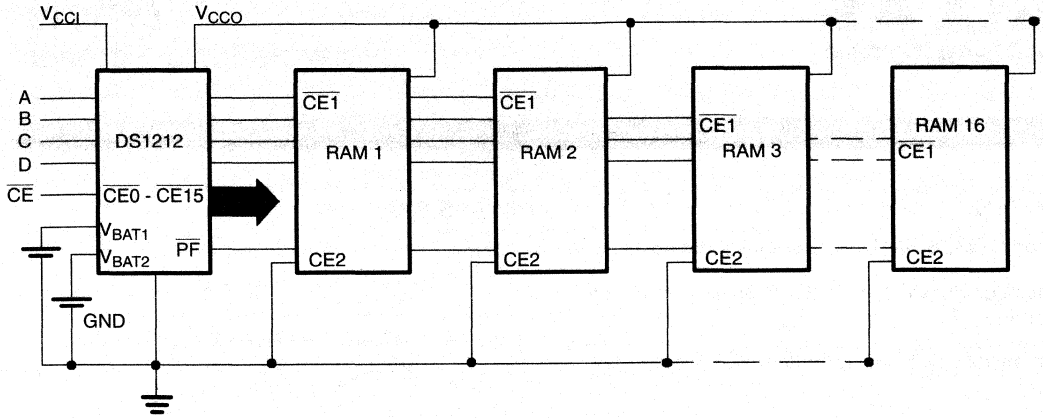
TIMING DIAGRAM: POWER UP



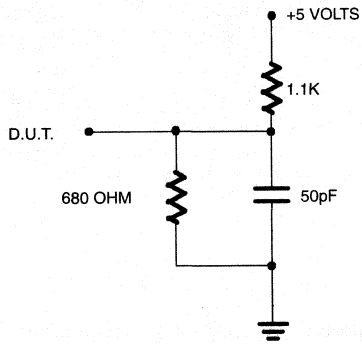
TIMING DIAGRAM: POWER DOWN



TYPICAL APPLICATION Figure 2



OUTPUT LOAD Figure 3



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NOTES:

1. All voltages referenced to ground.
2. Only one battery input is required.
3. Measured with V_{CCO} and $\overline{CE0}$-$\overline{CE15}$ open.
4. I_{CC01} is the maximum average load which the DS1212 can supply to the memories.
5. Measured with a load as shown in Figure 3.
6. I_{CC02} is the maximum average load current which the DS1212 can supply to the memories in the battery backup mode.
7. Chip enable outputs $\overline{CE0}$-$\overline{CE15}$ can only sustain leakage current in the battery backup mode.
8. t_{CE} max. must be met to ensure data integrity on power loss.
9. t_{AS} is only required to keep the decoder outputs glitch-free. While $\overline{CE}$ is low, the outputs ($\overline{CE0}$-$\overline{CE15}$) will be defined by inputs A through D with a propagation delay of t_{PD} from an A through D input change.
10. For applications where higher currents are required, please see the Battery Manager chip data sheet (DS1259).
11. The DS1212 has a 5K ohm resistor is series with the battery input. As current from the battery increases over 100 µA, the voltage drop will increase proportionately. The device cannot be damaged by higher currents in the battery path.

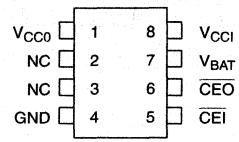
DALLAS SEMICONDUCTOR

DS1218
Nonvolatile Controller

FEATURES

- Converts CMOS RAM into nonvolatile memories
- Unconditionally write protects when V_{CC} is out of tolerance
- Automatically switches to battery when power fail occurs
- Space saving 8-pin mini-DIP/8-pin 150 mil SOIC
- Consumes less than 100 na of battery current

PIN ASSIGNMENT



PIN DESCRIPTION

V_{CCI}	-	Input +5 Volt Supply
V_{CCO}	-	RAM Power (V_{CC}) Supply
$\overline{CEI}$	-	Chip Enable Input
NC	-	No Connection
$\overline{CEO}$	-	Chip Enable Output
V_{BAT}	-	+ Battery
GND	-	Ground

DESCRIPTION

The DS1218 is a CMOS circuit which solves the application problems of converting CMOS RAM into nonvolatile memory. Incoming power is monitored for an out of tolerance condition. When such a condition is detected, the chip enable output is inhibited to accomplish write protection and the battery is switched on to supply RAM with uninterrupted power. Special circuitry uses a low-leakage CMOS process which affords precise voltage detection at extremely low battery consumption. The 8-pin mini-DIP package keeps PC board real estate requirements to a minimum. By combining the DS1218 nonvolatile controller chip with a full CMOS memory and lithium batteries, ten years of nonvolatile RAM operation can be achieved.

OPERATION

The DS1218 Nonvolatile Controller performs the circuit functions required to battery back up a RAM. First, a switch is provided to direct power from the battery or V_{CCI} supply depending on which is greater. This switch has a voltage drop of less than 0.2V. The second function which the nonvolatile controller provides is power fail detection. The DS1218 constantly monitors the V_{CC} supply. When V_{CCI} falls to 1.26 times the battery voltage a precision comparator outputs a power fail detect signal to the chip enable logic. The third function of write protection is accomplished by holding the chip enable output signal to within 0.2V of the V_{CCI} or battery supply, when a power fail condition is detected.

During nominal supply conditions, the chip enable output will follow chip enable input with a maximum propagation delay of 10 ns.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply	V_{CCI}	4.5	5.0	5.5	V	1
Logic 1	V_{IH}	2.0		5.5	V	1
Logic 0	V_{IL}	-0.3		0.8	V	1
Battery Supply	V_{BAT}	2.5	3.0	3.5	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CCI} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Current	I_{CCI}		2	5	mA	3
Battery Current	I_{BAT}			100	nA	3, 4
RAM Supply	V_{CCO}	V_{CC}-0.2			V	
RAM Current	I_{CCO}			70	mA	5
Input Leakage	I_{IL}	-1.0		1.0	µA	
$\overline{CEO}$ Output @ 2.4V	I_{OH}	-1.0			mA	
$\overline{CEO}$ Output @ 0.4V	I_{OL}			4.0	mA	
V_{CC} Trip Point	V_{CCTP}		1.26XV_{BAT}			

CAPACITANCE

(t_A = 25°C)

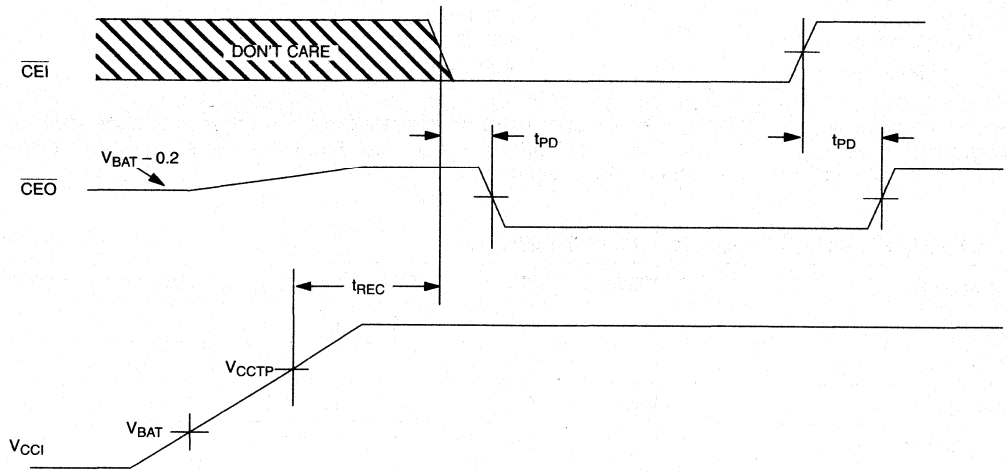
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

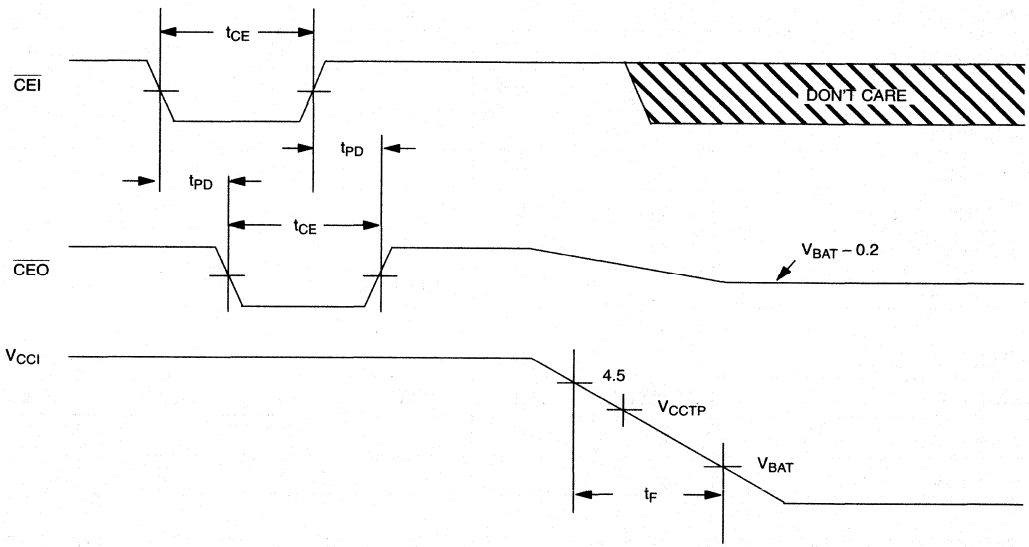
(0°C to 70°C; V_{CC} = 5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ Propagation Delay	t_{PD}		4	10	ns	2
Recovery at Power Up	t_{REC}	0.2		2	ms	
V_{CC} Slew Rate	t_F	500			µs	
$\overline{CE}$ Pulse Width	t_{CE}			1.5	µs	6, 7

TIMING DIAGRAM: POWER UP



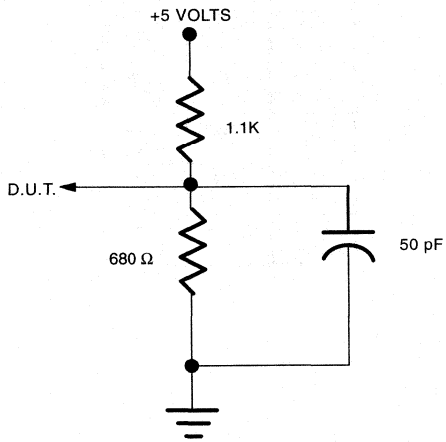
TIMING DIAGRAM: POWER DOWN



NOTES:

1. All voltages referenced to ground.
2. Measured with a load as shown in Figure 1.
3. Outputs open
4. Drain from battery when $V_{CC} < V_{BAT}$.
5. Maximum amount of current which can be drawn through pin 1 of the controller.
6. t_{CE} max must be met to ensure data integrity on power loss.
7. $\overline{CEO}$ can only sustain leakage current in the battery backup mode.

OUTPUT LOAD Figure 1



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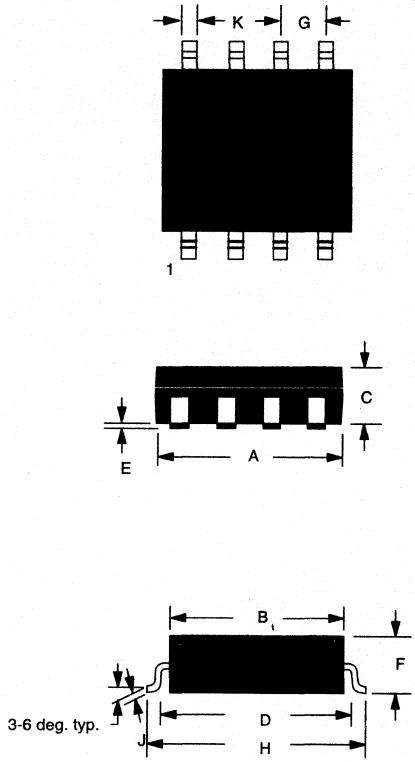
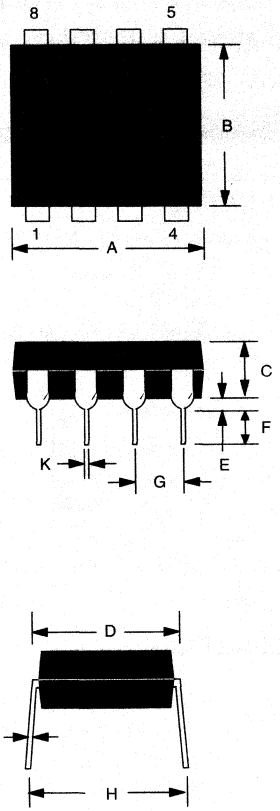
DS1218S NONVOLATILE CONTROLLER 8-PIN 150 MIL SOIC



PKG	8–PIN	
DIM	**MIN**	**MAX**
A IN. MM	0.188 4.78	0.195 4.95
B IN. MM	0.051 3.84	0.157 3.99
C IN. MM	0.052 1.32	0.061 1.55
D IN. MM	0.175 4.45	0.193 4.90
E IN. MM	0.004 0.10	0.010 0.25
F IN. MM	0.058 1.47	0.068 1.73
G IN. MM	0.046 1.17	0.054 1.37
H IN. MM	0.228 5.79	0.244 6.20
J IN. MM	0.006 0.15	0.011 0.28
K IN. MM	0.013 0.33	0.019 0.48

DS1218 NONVOLATILE CONTROLLER 8-PIN 300 MIL DIP



PKG	8-PIN	
DIM	**MIN**	**MAX**
A IN.	0.345	0.400
MM	8.76	10.16
B IN.	0.240	0.260
MM	6.10	6.60
C IN.	0.120	0.140
MM	3.05	3.56
D IN.	0.290	0.310
MM	7.37	7.87
E IN.	0.015	0.040
MM	0.38	1.02
F IN.	0.110	0.130
MM	2.79	3.30
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.320	0.370
MM	8.13	9.4
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

6

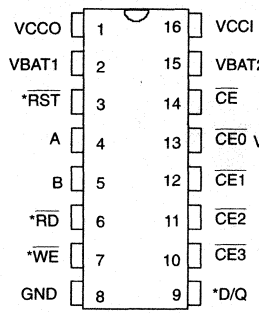
DALLAS SEMICONDUCTOR

DS1221
Nonvolatile Controller x 4 Chip

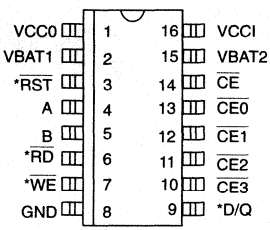
FEATURES

- Converts CMOS RAMs into nonvolatile memories
- Data is automatically protected during power loss
- 2-to-4 decoder provides for up to 4 CMOS RAMs
- Provides for redundant batteries
- Test battery condition on power-up
- Full ±10% operating range
- Unauthorized access can be prevented with optional security feature
- 16-pin 0.3-inch DIP saves PC board space
- Optional 16-pin SOIC surface mount package
- Optional industrial temperature range of -40°C to +85°C available

PIN ASSIGNMENT



DS1221 16–Pin DIP (300 MIL)
See Mech. Drawings Section



DS1221 16–Pin SOIC (300 MIL)
See Mech. Drawings Section

PIN DESCRIPTION

A, B	–	Address Inputs
$\overline{CE}$	–	Chip Enable Input
$\overline{CE0}$ - $\overline{CE3}$	–	Chip Enable Outputs
V_{BAT1}	–	+ Battery 1
V_{BAT2}	–	+ Battery 2
*$\overline{RST}$	–	Reset
V_{CCI}	–	+5V Supply
V_{CCO}	–	RAM Supply
*$\overline{RD}$	–	Read Input
*$\overline{WE}$	–	Write Input
*D/Q	–	Data Input/Output

*Used with optional security circuit only and must be connected to ground in all other cases.

DESCRIPTION

The DS1221 Nonvolatile Controller x 4 Chip is a CMOS circuit which solves the application problem of converting CMOS RAMs into nonvolatile memories. Incoming power is monitored for an out-of-tolerance condition. When such a condition is detected, the chip enable outputs are inhibited to accomplish write protection and the battery is switched on to supply RAMs with uninterrupted power. An optional security code prevents unauthorized users from obtaining access to the memory space. The nonvolatile controller/decoder circuitry uses a low-leakage CMOS process which affords precise voltage detection at extremely low battery consumption. By combining the DS1221 with up to four CMOS memories and lithium batteries, nonvolatile operation can be achieved.

CONTROLLER /DECODER OPERATION

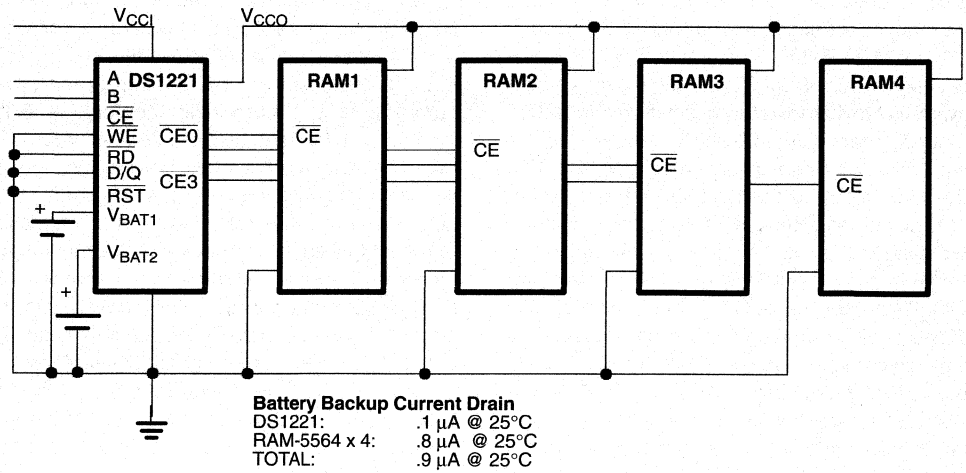
The DS1221 nonvolatile controller performs six circuit functions required to decode and battery back up a bank of up to four CMOS RAMs. First, a 2-to-4 decoder provides selection of one of four RAMs (see Figure 1). Second, a switch is provided to direct power from the battery or V_{CCI} supply, depending on which is greater, to the V_{CCO} pin. This switch has a voltage drop of less than 0.2V. The third function which the nonvolatile controller provides is power-fail detection. The DS1221 constantly monitors the V_{CCI} supply. When V_{CCI} falls below 4.5 volts, a precision comparator detects the condition and inhibits the RAM chip enables ($\overline{CE0}$ through $\overline{CE3}$). The fourth function of write protection is accomplished by holding all chip enable outputs ($\overline{CE0}$ through $\overline{CE3}$) to within 0.2 volts of V_{CCI} or battery supply. If the Chip Enable Input ($\overline{CE}$) is low at the time power-fail detection occurs, the chip enable outputs are kept in their present state until $\overline{CE}$ is driven high. The delay of write protection until the current memory cycle is completed prevents the corruption of data. Power failure detection occurs in the range of 4.5 to 4.25 volts. During nominal supply conditions the chip enable outputs follow the logic of a 2-to-4 decoder. The fifth function the DS1221 performs is to check battery status to warn of potential data loss. Each time that V_{CCI} power is restored the battery voltage is checked with a precision comparator. If the connected battery voltage is less than 2 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in memory, verifying that memory location content. A subsequent write cycle can then be executed to the same memory location, altering the data. If the next read cycle fails to verify the written data, the contents of the memories are questionable. The sixth function of the nonvolatile controller provides for battery redundancy. In many applications, data integrity is paramount. In these applications it is often desirable to use two batteries to ensure reliability. The DS1221 provides an internal isolation switch which provides for connection of two batteries. During battery back-up operation the battery with the highest voltage is selected for use. If one battery should fail, the other will automatically take over. The switch between batteries is transparent to the user. A battery status warning will occur if both batteries are less than 2.0 volts. If only one battery is used, the second battery input must be grounded. Figure 2 illustrates the connections required for the DS1221 in a typical application.

NONVOLATILE CONTROLLER/DECODER Figure 1

	INPUTS			OUTPUTS			
V_{CCI}	$\overline{CE}$	B	A	$\overline{CE0}$	$\overline{CE1}$	$\overline{CE2}$	$\overline{CE3}$
>=4.5	H	X	X	H	H	H	H
< 4.25	X	X	X	H	H	H	H
>=4.5	L	L	L	L	H	H	H
>=4.5	L	L	H	H	L	H	H
>=4.5	L	H	L	H	H	L	H
>=4.5	L	H	H	H	H	H	L

H = High Level
L = Low Level
X = Irrelevant

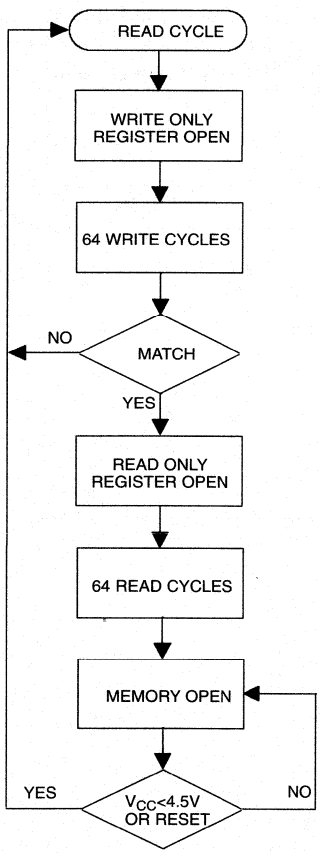
TYPICAL APPLICATION Figure 2



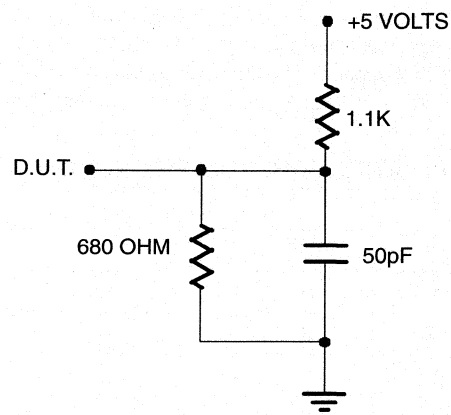
Battery Backup Current Drain

DS1221:	.1 µA @ 25°C
RAM-5564 x 4:	.8 µA @ 25°C
TOTAL:	.9 µA @ 25°C

SECURITY SEQUENCE Figure 3



OUTPUT LOAD Figure 4



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	20 mA

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CCI}	4.5	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.2		V_{CC}+0.3	V	1
Logic 0 Input	V_{IL}	-0.3		+0.8	V	1
Battery Input	V_{BAT1} V_{BAT2}	2.0		4.0	V	1, 2

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}= 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CCI}			5	mA	3
Supply Voltage	V_{CCO}	V_{CC}-0.2			V	1
Supply Current	I_{CCO1}			80	mA	4, 10
Input Leakage	I_{IL}	-1.0		+1.0	µA	
Output Leakage	I_{LO}	-1.0		+1.0	µA	
$\overline{CE0}$-$\overline{CE3}$, DQ Output @ 2.4V	I_{OH}	-1.0			mA	5
$\overline{CE0}$-$\overline{CE3}$, DQ Output @ 0.4V	I_{OL}			4.0	mA	5
V_{CC} Trip Point	V_{CCTP}	4.25	4.37	4.50	V	1

(0°C to 70°C; V_{CC}< 4.25V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE0}$-$\overline{CE3}$ Output	V_{OHL}	V_{CC}-0.2 V_{BAT}-0.2			V	
V_{BAT1} or V_{BAT2} Battery Current	I_{BAT}			0.1	µA	3
Battery Backup Current @ V_{CCO} = V_{BAT} - 0.5V	I_{CCO2}			100	µA	6, 7, 10

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}= 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ Propagation Delay	t_{PD}	5	10	20	ns	5
$\overline{CE}$ High to Power-Fail	t_{PF}			0	ns	
Address Setup	t_{AS}	20			ns	9

(0°C to 70°C; V_{CC}< 4.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power Up	t_{REC}	2	5	10	ms	
V_{CC} Slew Rate 4.5 - 4.25V	t_F	300			µs	
V_{CC} Slew Rate 4.25 - 3V	t_{FB}	10			µs	
V_{CC} Slew Rate 4.25 - 4.5V	t_R	0			µs	
$\overline{CE}$ Pulse Width	t_{CE}			1.5	µs	7, 8

NOTES:

1. All voltages are referenced to ground.
2. Only one battery input is required.
3. Measured with V_{CCO} and $\overline{CE0}$ - $\overline{CE3}$ open.
4. I_{CCO1} is the maximum average load which the DS1221 can supply to the memories.
5. Measured with a load as shown in Figure 4.
6. I_{CCO2} is the maximum average load current which the DS1221 can supply to the memories in the battery back-up mode.
7. Chip enable outputs $\overline{CE0}$ - $\overline{CE3}$ can only sustain leakage current in the battery back-up mode.
8. t_{CE} max. must be met to ensure data integrity on power loss.
9. t_{AS} is only required to keep the decoder outputs glitch-free. While $\overline{CE}$ is low, the outputs ($\overline{CE0}$ - $\overline{CE3}$) will be defined by inputs A and B with a propagation delay of t_{PD} from an A or B input change.
10. For applications where higher currents are required, please see the DS1259 Battery Manager Chip data sheet.

SECURITY OPTION

When activated by Dallas Semiconductor, the security option prevents unauthorized access. A sequence of events must occur to gain access to the memories (Figure 3). First, a dummy read cycle or a 200 ns active low reset pulse is executed to initialize the sequence. Second, a 64-bit access code must be consecutively written to the DS1221 using the write enable signal ($\overline{WE}$), the chip enable signal ($\overline{CE}$), and the data input/output signal (DQ). The code is written to the DS1221 without regard to the address. Actual RAM locations are not written, as the security option is intercepting the data path until access is granted. Instead, a special 64-bit write only register is written. Following the 64 write cycles, the register is compared to a 64-bit pattern uniquely defined by the user and programmed into the DS1221 by Dallas Semiconductor at the time of manufacture. This pattern can only be interrogated by an intelligent controller within the DS1221 and cannot be read by the user. If a read cycle occurs before 64 write cycles are completed, the security sequence is aborted. When a correct match for 64 bits is received, the third part of the security sequence begins by reading a 64-bit read only register. This register consists of 64 bits also defined by the user and programmed into the DS1221 by Dallas Semiconductor at the time of manufacture. For each of the 64 read cycles, one bit of the user-defined read only register is driven onto the DQ line. This phase also requires that the 64 read cycles be consecutive. The data being read from the read only register can be used by software to determine if the DS1221 will be permitted to be used with that particular system. After the 64th read cycle has been executed the DS1221 is unlocked and all subsequent memory cycles will be passed through and will become actual memory accesses based upon address inputs. If V_{CC} falls below 4.5 volts or the reset line is driven low, the entire security sequence must be executed again in order to access memory locations.

NOTE:
Contact Dallas Semiconductor sales office for code assignments.

SECURITY OPTION
AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
$\overline{CE}$ Access Time	t_{CO}			200	ns	
$\overline{RD}$ Access Time	t_{OE}			100	ns	
$\overline{CE}$ to Output Low Z	t_{COE}	10			ns	
$\overline{RD}$ to Output Low Z	t_{OEE}	10			ns	
$\overline{CE}$ to Output High Z	t_{OD}			100	ns	
$\overline{RD}$ to Output High Z	t_{ODO}			100	ns	
Read Recovery	t_{RR}	50			ns	
Write Cycle	t_{WC}	250			ns	
Write Pulse Width	t_{WP}	170			ns	
Write Recovery	t_{WR}	50			ns	
Data Setup	t_{DS}	100			ns	
Data Hold Time	t_{DH}	0			ns	
$\overline{CE}$ Pulse Width	t_{CW}	170			ns	
Reset Pulse Width	t_{RST}	200			ns	

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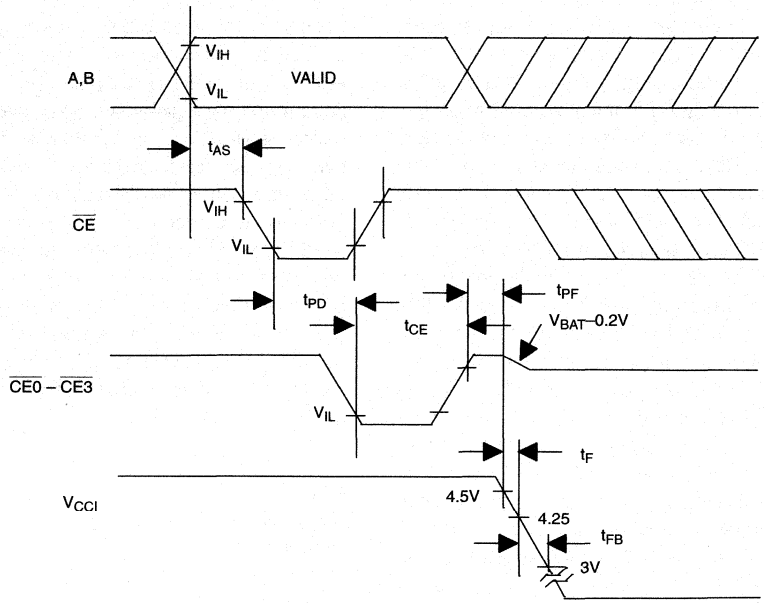
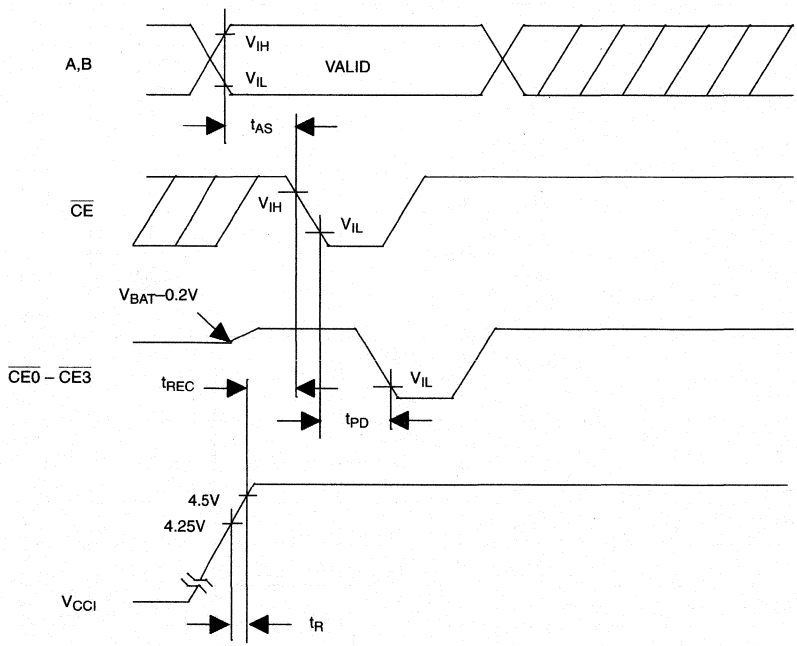
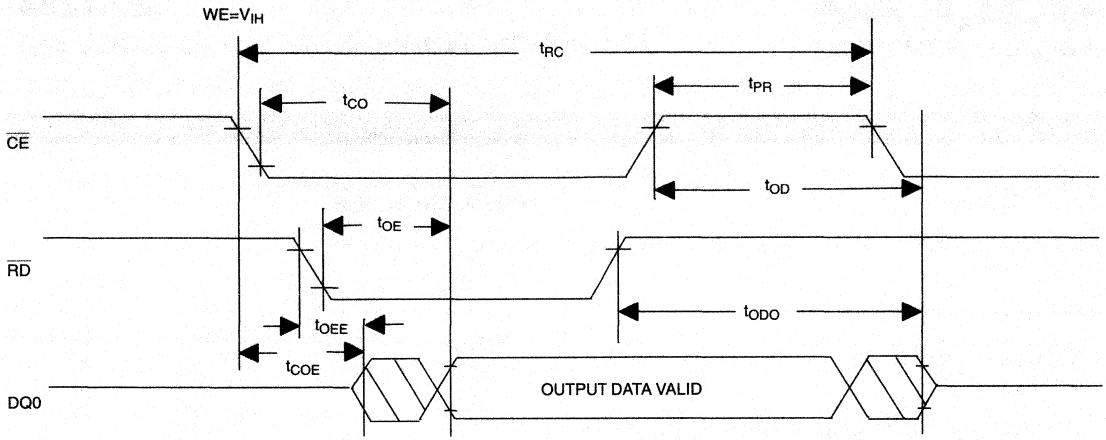
POWER-DOWN Figure 5



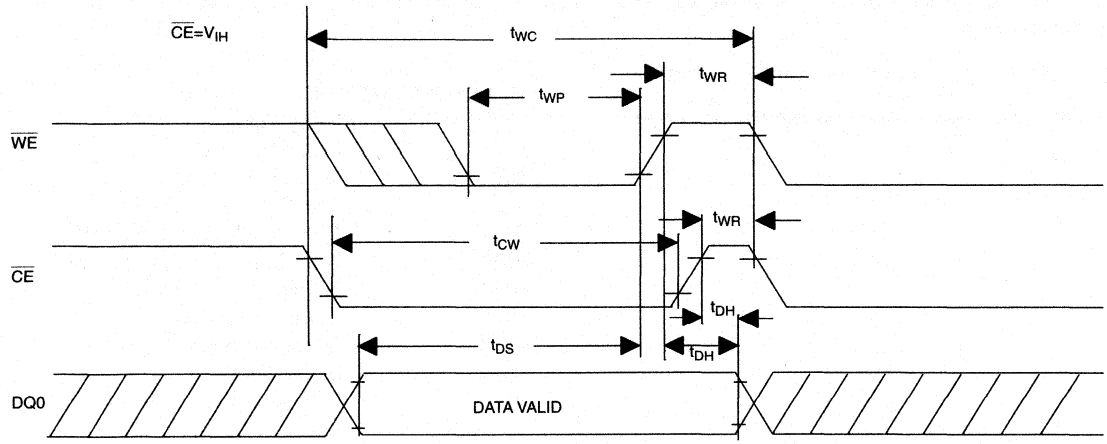
POWER-UP Figure 6



READ CYCLE TO SECURITY OPTION Figure 7



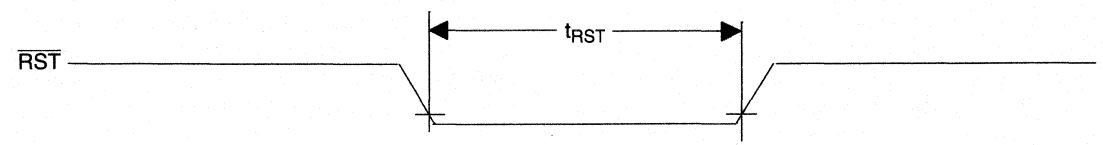
WRITE CYCLE TO SECURITY OPTION Figure 8



NOTES:

1. t_{DH} and t_{DS} are functions of the first occurring edge of $\overline{WE}$ or $\overline{CE}$.
2. t_{WR} is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CE}$.

RESET FOR SECURITY OPTION Figure 9



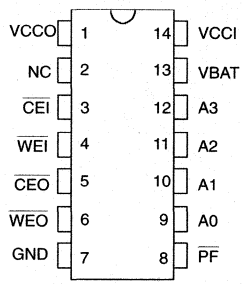
DALLAS SEMICONDUCTOR

DS1234
Conditional Nonvolatile Controller Chip

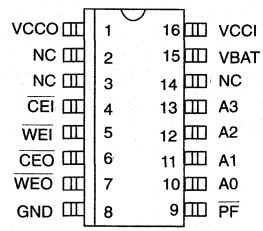
FEATURES

- Converts CMOS static RAMs into nonvolatile memories
- Software-controlled write inhibit
- Software-controlled battery disconnect extends battery life
- Unconditionally write protects when V_{CC} is out of tolerance
- Consumes less than 100 nA of battery current
- Power fail signal can be used to interrupt processor on power failure
- Low forward voltage drop on the V_{CC} switch
- Optional 16-pin SOIC surface mount package

PIN ASSIGNMENT



DS1234 14-Pin DIP (300 MIL)
See Mech. Drawings Section



DS1234S 16-Pin SOIC (300 MIL)
See Mech. Drawings Section

PIN DESCRIPTION

V_{CCO}	–	RAM Supply
NC	–	No Connection
$\overline{CEI}$	–	Chip Enable Input
$\overline{WEI}$	–	Write Enable Input
$\overline{CEO}$	–	Chip Enable Output to RAM
$\overline{WEO}$	–	Write Enable Output to RAM
GND	–	Ground
$\overline{PF}$	–	Power Fail Output
A0-A3	–	Address Inputs
V_{BAT}	–	Battery Input
V_{CCI}	–	+5V Supply

DESCRIPTION

The DS1234 is a CMOS circuit that converts CMOS RAM into nonvolatile memory and adds two software selectable switches. Incoming power is monitored for an out-of-tolerance condition. When such a condition is detected, chip enable and write enable to the RAM are inhibited to accomplish write protection, and the battery is switched on to supply the memory with uninterrupted power. The two software selectable switches provided by the DS1234 are capable of inhibiting both the write enable to the RAM and the battery backup circuitry by a pattern recognition sequence across four address lines. Inhibiting the write enable to the nonvolatile RAM provides data integrity by isolating the memory contents from external change. The second switch provides added flexibility and increases battery life to the system by enabling/disabling the battery for shipment or storage, or when battery backup is not needed.

OPERATION

The DS1234 Conditional Nonvolatile Controller performs three circuit functions required to battery back up a RAM. First, a switch is provided to direct power from the battery or the incoming supply (V_{CCI}), depending on which is greater. This switch has a voltage drop of less than 0.2V. The second function is power fail detection. The DS1234 constantly monitors the incoming supply. When the supply goes out-of-tolerance, a comparator detects power fail and inhibits chip enable and write enable. The threshold voltage, V_{TP}, at which power fail is detected is defined as 1.26 times V_{BAT}. The third function of write protection is accomplished by holding the $\overline{CEO}$ and $\overline{WEO}$ output signals to within 0.2 volts of the V_{CCI} or battery supply.

In addition to the nonvolatile controller functions, the DS1234 supplies two software-selectable switches for master control of the write enable and the nonvolatile controller itself. The switches are controlled by a 16-cycle pattern recognition sequence across four address lines (see Tables 1 and 2). Prior to entering the pattern recognition sequence that will define the two switch settings, a read cycle of 1111 on address inputs A0 through A3 should be executed to initialize the compare pointer of clock zero. Each four-bit compare word is clocked into the DS1234 on the negative edge of $\overline{CEI}$. A0, A1 and A2 must match the compare pattern on all 16 consecutive cycles while A3 must match only the first eleven; the last five are used to define the switch settings. The eleventh address cycle, starting at zero, defines the switch that inhibits the write enable to the RAM ($\overline{WEO}$). A logic one in this location allows read/write operations so that $\overline{WEO}$ will follow $\overline{WEI}$ and data can be updated. A zero on cycle eleven turns the RAM into a read-only memory (ROM). The next four address cycles, 12 thorough 15, define whether the nonvolatile controller operation is enabled or disabled. A bit pattern of 1010 activates the nonvolatile controller; data in the RAM is maintained on power loss. Any pattern other than 1010 will disable the nonvolatile controller operation.

At the completion of the 16th cycle, if the pattern recognition sequence is correct, the switch settings defined in cycles 11 though 15 are transferred and are active for the next memory cycle. When external battery power is applied for the first time, the DS1234 will come up with the nonvolatile controller off. Upon initial V_{CC} power, the write enable will be set in read/write operation ($\overline{WEI}$=$\overline{WEO}$).

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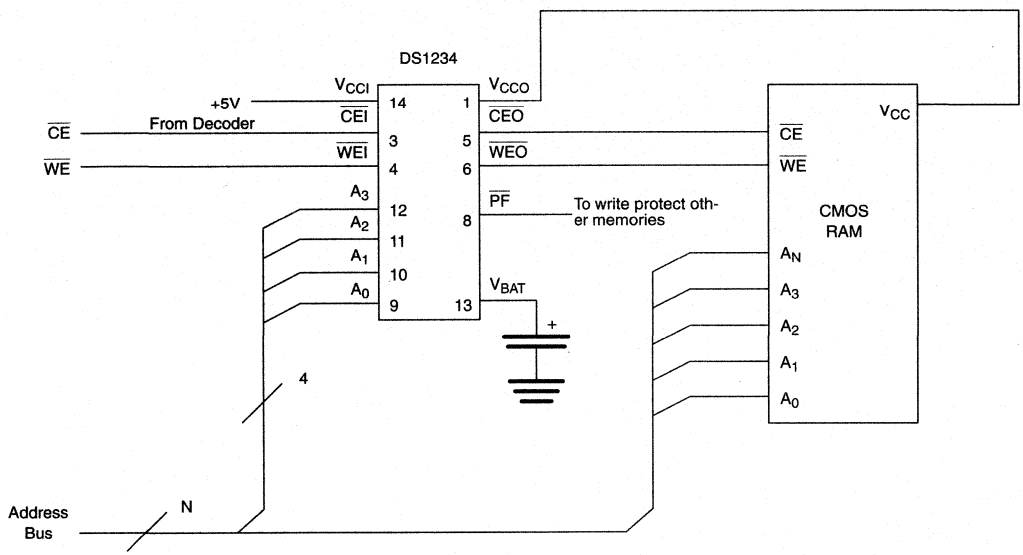
CONTROLLER TO MEMORY INTERFACE Figure 1



ADDRESS INPUT PATTERN Table 1

	CYCLE NUMBER															
Address Inputs	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
A3	1	0	1	0	0	0	1	1	0	1	0	*	*	*	*	*
A2	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1
A1	1	0	1	0	0	0	1	1	0	1	0	1	1	1	0	0
A0	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1

CONTROL SELECT Table 2

$\overline{\text{WE}}$ **Battery Control**					**Operation**
11	**12**	**13**	**14**	**15**	
0	X	X	X	X	Read Only Operation
1	X	X	X	X	Read/Write Operation
X	1	0	1	0	Enables Nonvolatile Controller*

X = Don't Care

*Any other combination turns controller off

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CCI}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.2		V_{CC}+0.3	V	1
Input Low Voltage	V_{IL}	-0.3		+0.8	V	1
Battery Voltage	V_{BAT}	2.5		3.5	V	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CCI}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CCI}			5	mA	2
Supply Current @ $V_{CCO} = V_{CCI} - 0.2$	I_{CCO}			80	mA	3
Input Leakage	I_{IL}	-1.0		+1.0	µA	
Output Leakage	I_{LO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	4
Output Current @ 0.4V	I_{OL}			4.0	mA	4

(0°C to 70°C; V_{CCI}=< V_{BAT})

$\overline{CEO}$, $\overline{WEO}$ Output	V_{OHL}	V_{BAT}-0.2			V	6
Battery Current	I_{BAT}			0.1	µA	7
Battery Backup Current @ $V_{CCO} = V_{BAT} - 0.3V$	I_{CCO1}			100	µA	5

CAPACITANCE

(T_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OU}			7	pF	

AC ELECTRICAL CHARACTERISTIC

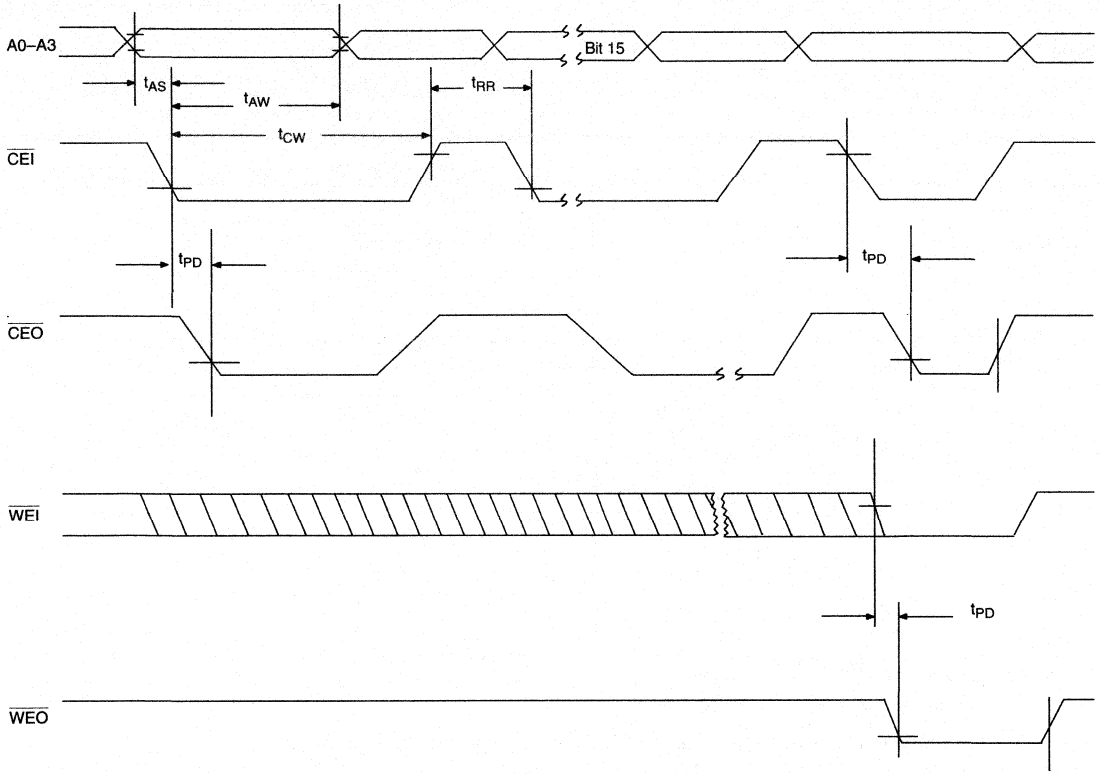
(0°C to 70°C; V_{CCI} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
Read Recovery	t_{RR}	40			ns	
$\overline{CEI}$ Pulse Width	t_{CW}	110			ns	
Propagation Delay	t_{PD}			20	ns	

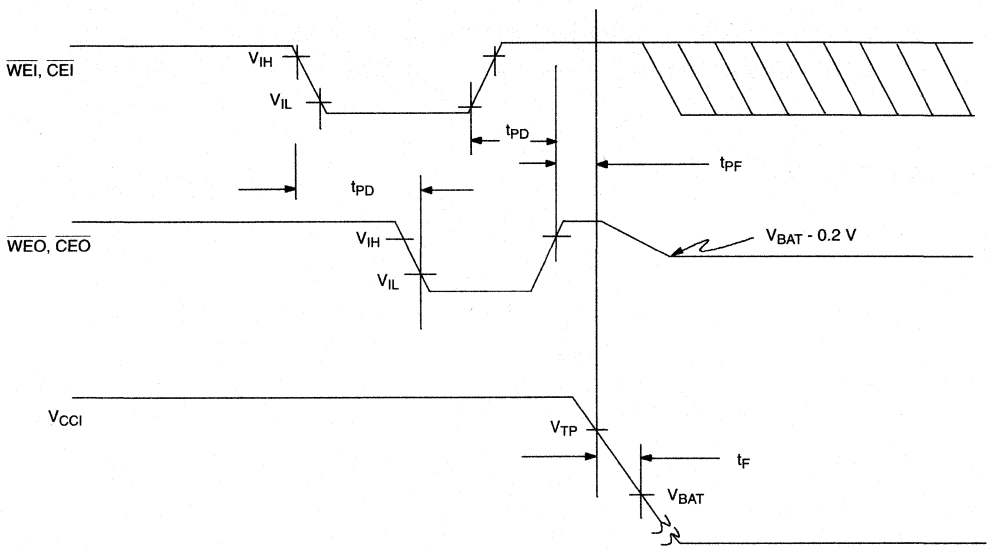
(0°C to 70°C; $V_{CCI} < V_{TP}$)

Recovery at Power Up	t_{REC}			2	ms	
V_{CC} Slew Rate Power Down	t_F	10			µs	
V_{CC} Slew Rate Power Up	t_R	0			µs	
$\overline{CEI}$ High to Power Fail	t_{PF}	0			ns	

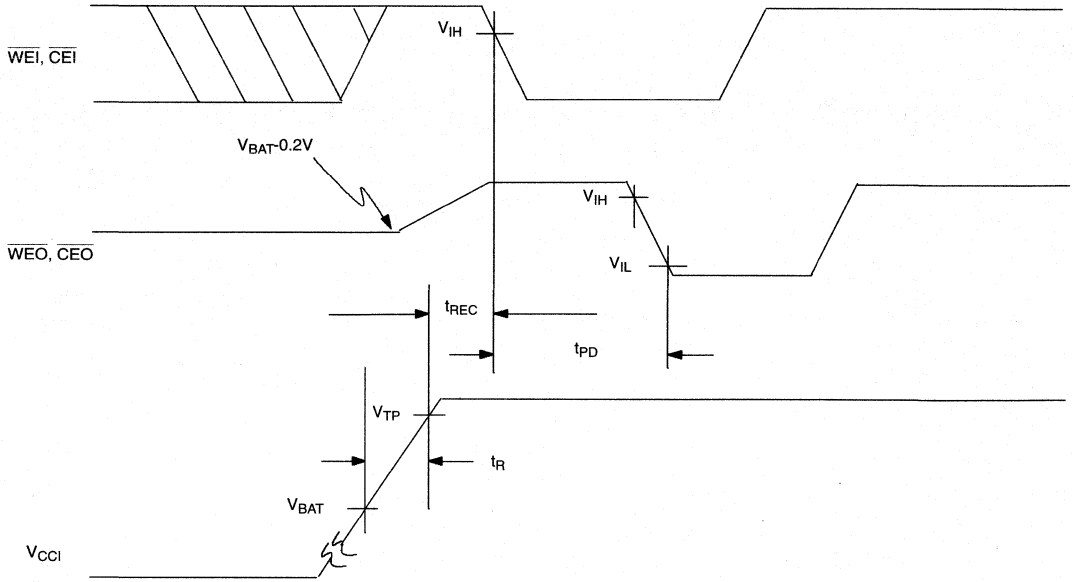
TIMING DIAGRAM: SWITCH SETTING



TIMING DIAGRAM: POWER DOWN



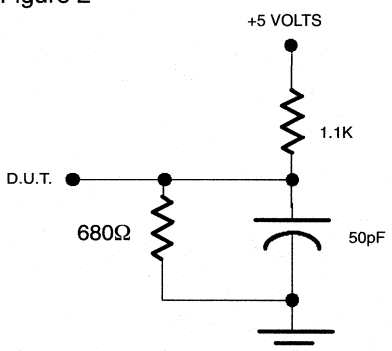
TIMING DIAGRAM: POWER-UP



NOTES:

1. All voltages are referenced to ground.
2. Measured with V_{CCO}, $\overline{CEO}$ and $\overline{WEO}$ open.
3. I_{CCO} is the maximum average load that the DS1234 can supply to the memories.
4. Measured with a load as shown in Figure 2.
5. I_{CC01} is the maximum average load current that the DS1234 can supply to the memories in the battery back-up mode.
6. $\overline{CEO}$ and $\overline{WEO}$, outputs can only sustain leakage current in the battery backup mode.
7. I_{BAT} is the total load current that the DS1234 uses from the battery input pin with V_{CCO}, $\overline{CEO}$, and $\overline{WEO}$ open.

OUTPUT LOAD Figure 2



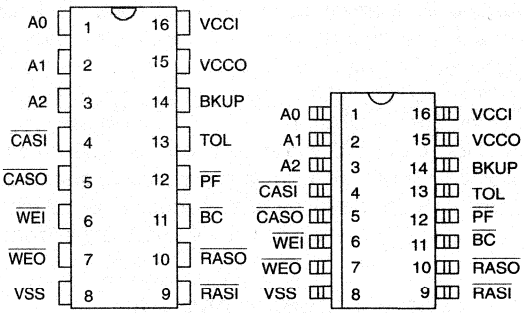
DALLAS SEMICONDUCTOR

DS1237
DRAM Nonvolatizer Chip

FEATURES

- Converts DRAM into nonvolatile RAM
- Controls any density of DRAM
- Wide backup supply voltage range
- Automatically refreshes when power fail detection occurs
- Power fail detection signal for hardwire interrupt
- Refresh is turned over to the processor after power-up under software control
- Space-saving 16-pin DIP and 16-pin SOIC for surface mounting
- Low-power CMOS
- Built-in backup condition circuit warns of impending backup supply failure
- Software-controlled backup supply disconnects switch for storage and shipment
- Software-controlled counter measures backup supply discharge time
- Optional refresh periods of 8 ms, 16 ms, 32 ms, and 64 ms are available to support extended refreshing at reduced power levels

PIN ASSIGNMENT



DS1237 16–Pin DIP (300 MIL) See Mech. Drawings Section

DS1237S 16–Pin SOIC (300 MIL) See Mech. Drawings Section

PIN DESCRIPTION

BKUP	–	Backup Supply
$\overline{BC}$	–	Backup Condition
TOL	–	V_{CCI} Trip Point Select
$\overline{PF}$	–	Power Fail Output
A0-A2	–	Address Inputs
V_{SS}	–	Ground
$\overline{WEI}$	–	Write Enable Input
$\overline{WEO}$	–	Write Enable Output
$\overline{CASI}$	–	$\overline{CAS}$ Input from System
$\overline{CASO}$	–	$\overline{CAS}$ Output to DRAM
$\overline{RASI}$	–	$\overline{RAS}$ Input from System
$\overline{RASO}$	–	$\overline{RAS}$ Output to DRAM
V_{CCO}	–	V_{CC} Output to DRAM
V_{CCI}	–	+5 Volt Input

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DESCRIPTION

The DS1237 DRAM Nonvolatizer Chip is a CMOS circuit designed to control DRAMs such that information stored in memory is retained and protected during power failure. The DS1237 accomplishes this by monitoring the power supply for an out-of-tolerance condition. When such a condition occurs, DRAM is isolated from system control and the power supply for the DRAM is switched from V_{CC} to the backup supply. Refresh control is maintained by the DS1237 until the power is within specification. At this time refresh is returned to the system after a highly structured serial sequence on address lines A0, A1, and A2. Other serial sequences are used to set switches which control a counter used to measure backup supply discharging and electrically connect or disconnect the backup supply.

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OPERATION – NORMAL POWER CONDITIONS

Under normal operation, system +5 volt power is supplied within the tolerance limits set by pin 13 (TOL). If pin 13 is connected to V_{CCO}, the DS1237 will operate in the normal mode down to 4.75 volts. When pin 13 is grounded, the DS1237 will operate in the normal mode down to 4.5 volts. During normal operation the $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ inputs are directly routed to the respective outputs with a maximum propagation delay of 15 ns. The backup supply input is normally connected to either a chargeable capacitor or battery; however, any backup supply with a voltage input between the limits of 6.0 volts and 10 volts is suitable. The power fail output ($\overline{PF}$) is at high level and address inputs A0, A1, and A2 are monitored for software-driven sequences. The backup condition output $\overline{BC}$ will be in an inactive (high) state provided that the backup input level is greater than 5.5 volts on V_{CCI} and the backup counter has not reached zero.

OPERATION – POWER LOSS AND DATA RETENTION

When the 5-volt V_{CC} power begins to drop, a precision band gap comparator senses this change. Depending on the level of the Tolerance Pin 13, a power fail signal will be generated as V_{CCI} falls below 4.75 volts or 4.5 volts. At this time, the DS1237 enters a data retention mode provided that the backup supply is enabled. The power fail output signal will remain low until V_{CCI} is restored to normal conditions. While entering the data retention mode, the DS1237 isolates all control inputs and starts driving the $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ outputs. In addition, if $\overline{RAS}$ = 1, the DS1237 immediately takes control and issues the first refresh burst 62.5 µs later. If $\overline{RAS}$ = 0, the DS1237 will wait for $\overline{RAS}$ to go to a logic 1 level and then take control and issue the first refresh burst 62.5 µs later. If $\overline{RAS}$ = 0 and remains low for more than 10 µs after Power Fail Detect, the DS1237 will take control and drive $\overline{RASO}$ = 1, then issue the first refresh burst 62.5 µs later. The V_{CCI} input is disconnected from V_{CCO} and the regulated backup supply is connected. A burst $\overline{CAS}$ before $\overline{RAS}$ refresh cycle is generated at a cycle time of 350 ns maximum. This burst refresh continues for 520 or 1032 consecutive cycles, depending on the dash number of the device (see Table 1). After the burst refresh is complete, subsequent burst refreshing continues at 8, 16, 32, or 64 ms intervals until V_{CCI} returns to normal levels and the system signals the DS1237 that it is ready to assume refresh duties. The $\overline{WE}$ output is held at the high (inactive) level from the time control is taken by the DS1237 until the system assumes refresh duties. If the DS1237 enters a power loss condition without the backup supply enabled, no refresh activity occurs and data stored into connected DRAMs is lost.

OPERATION – RETURN TO NORMAL POWER CONDITIONS

When the system +5 volt supply returns and exceeds the level determined by the TOL pin, the V_{CCI} input is immediately reconnected to the V_{CCO} output pin while the regulated backup supply is internally disconnected from V_{CCO}. Burst refreshing continues without interruption until the system signals that it is ready to assume the responsibility of refreshing the DRAMs. Refresh duties are shifted from the DS1237 to the system when a software-controlled switch is set by sending a specific pattern on address lines A0, A1, and A2 for 24 consecutive cycles. The address pattern which sets the software switch is shown in Figure 1. The address pattern is clocked, LSB first, into the DS1237 on the falling edge of $\overline{CAS}$ provided that setup and hold times are met. When the 24th cycle is correctly entered, the DS1237 will issue a final refresh burst and then return control to the host system. At this point, the host system will be responsible for handling all refresh requirements. RAM read and write cycles can resume without restrictions after the software switch is correctly set.

ACTIVATION OF BACKUP SUPPLY

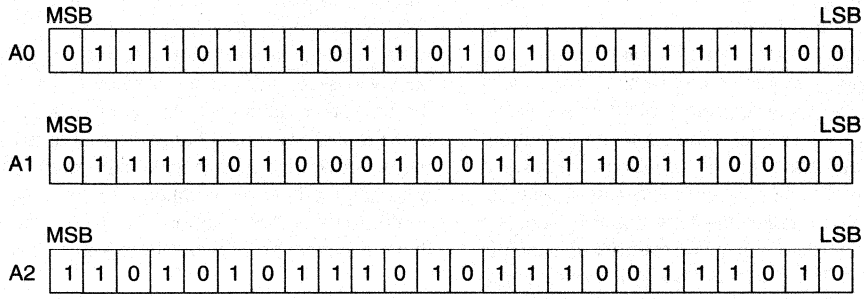
A software-controlled switch allows conservation of the backup supply when data retention is not required. The switch is controlled by the same method described for refresh except that the bit pattern is different. On the initial connection of the battery, the backup supply switch will be off. Under this condition, no refresh activity will occur when V_{CCI} is out of tolerance. The bit patterns presented in Figure 2 show how the backup supply can be activated or deactivated under software control.

REFRESH INTERVALS Table 1

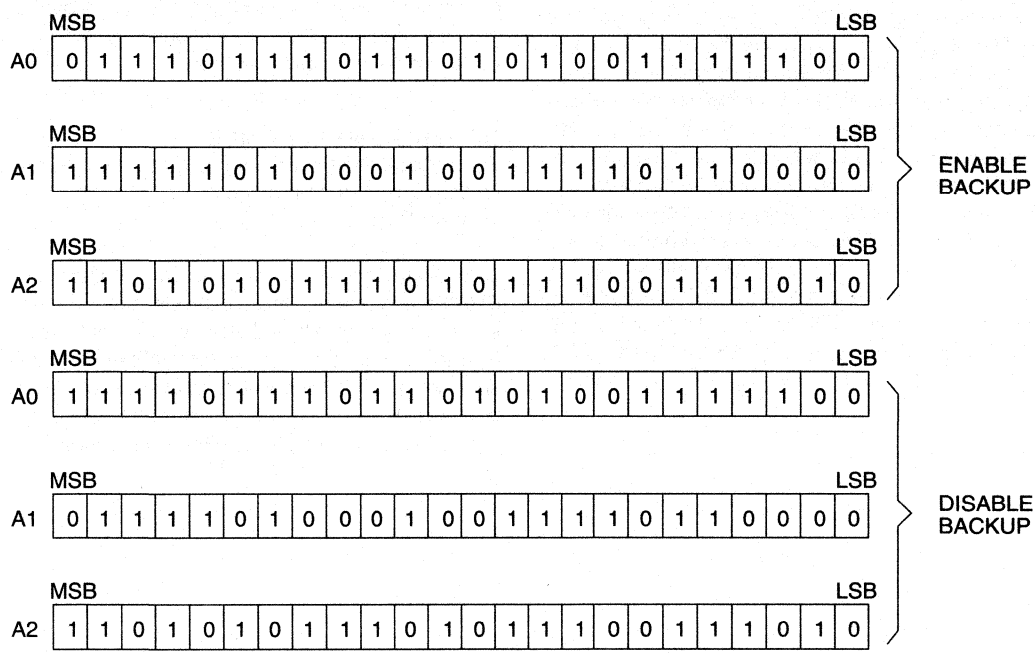
	REFRESH INTERVAL (ms)*			
NUMBER OF CYCLES	8	16	32	64
256K DRAM: 520	-1	-2	-3	-4
1 Meg DRAM: 1032	-5	-6	-7	-8

*Refresh intervals have a tolerance of ±12.5%.

SOFTWARE SWITCH FOR PROCESSOR CONTROL ON POWER-UP Figure 1



SOFTWARE CONTROLLED SWITCH FOR ACTIVATION OF BACKUP SUPPLY Figure 2



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BATTERY CONDITION

The DS1237 has two features which provide information about the condition of the backup supply. First, the DS1237 monitors the backup supply input condition. If this input is below V_{CCI}, the backup condition output pin ($\overline{BC}$) is driven to the active state (low) and will remain in this state until the backup supply voltage is restored to a level above V_{CCI}. This feature is active only while V_{CCI} is applied within nominal limits. Whenever the backup supply is supplying power, the $\overline{BC}$ pin remains at a logic 0 state. The second feature for monitoring the condition of the backup supply is a counter which is decremented on one-second intervals whenever the backup supply is supplying power. This counter is set with a number while V_{CCI} is within nominal limits. The value of the counter is entered by sending a 24-bit sequence on address lines A0, A1, and A2 in the same manner as described for refresh control. This sequence is shown in Figure 3. After the 24-bit sequence is correctly entered, the next 24 bits will define the time count in seconds which will start decrementing when the backup supply is supplying power. This count is 24 bits long and is entered LSB first on address line A0 when the $\overline{CASI}$ line goes low. The counter is a binary number representing the time allowed until the backup supply has been discharged. When the counter reaches zero, the $\overline{BC}$ pin will be low even though the V_{CCI} supply is within nominal limits. The $\overline{BC}$ pin will remain low until a new value is entered into the counter. This time can be calculated by dividing the capacity in ampere hours of the backup supply by the average load current of the DRAMs and converting this value into seconds (see Figure 5). The value in the counter can be read at any time while V_{CCI} is within nominal limits by sending the 24-bit sequence shown in Figure 4. This sequence is entered in the same manner as described for refresh control. After this sequence is correctly entered, the next 24 $\overline{CASI}$ cycles will cause the contents of the counter to be shifted out one bit at a time starting with the LSB on the $\overline{BC}$ pin. A logic 0 on $\overline{BC}$ while $\overline{CAS}$ is low is a logic 0 for that bit.

BACKUP CONDITION APPLICATIONS

The backup condition features of the DS1237 can supply the system valuable information about the backup supply. A simple application may only use the V_{CC} comparator to tell the system that a battery is weak and should be replaced. A more sophisticated system may use the backup condition counter to measure the time that a primary battery is used to supply power to DRAMs. By knowing the capacity of the battery and the requirements of the DRAM, the time for battery replacement can be predicted. In fact, if worst case primary supply outages can be estimated, the backup battery can be selected so that replacement can always occur prior to backup supply failure. If a rechargeable backup supply is used, such as a capacitor or a nicad battery, the backup condition counter can be used to measure both the charge and discharge time. Charge time can be measured by using a system time base and periodically adjusting the battery condition counter under software control to reflect the amount of time (amount of charge) that the system primary power is within nominal limits.

NOTE:

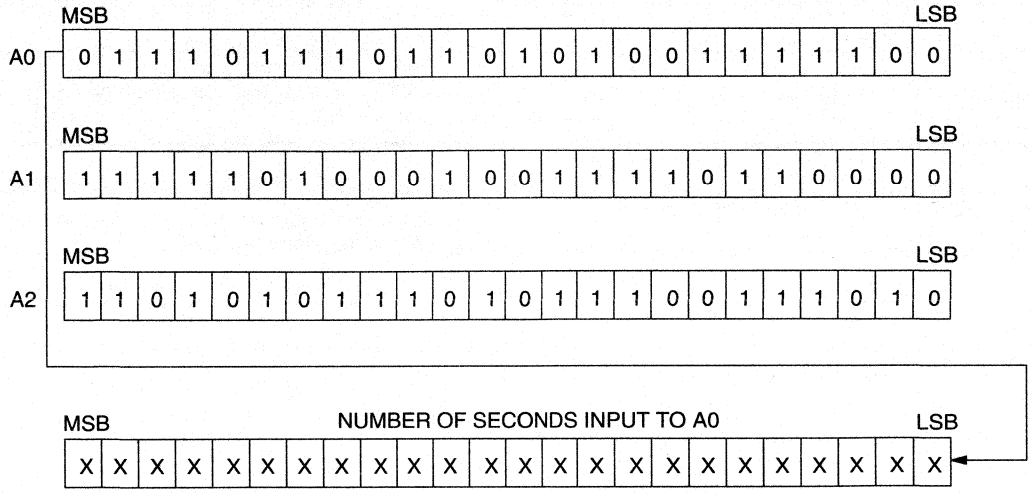
The DS1237 requires capacitive bypassing techniques between V_{CCO} and GND for proper operation. A bypass capacitor between V_{CCI} and BKUP is also essential for proper operation. While applications vary, a 10 µF capacitor value is typically required.

DATA RETENTION TIMES

The equations in Figure 5 are used to find the data retention time of DRAMs using the DS1237 DRAM Nonvolatizer Chip.

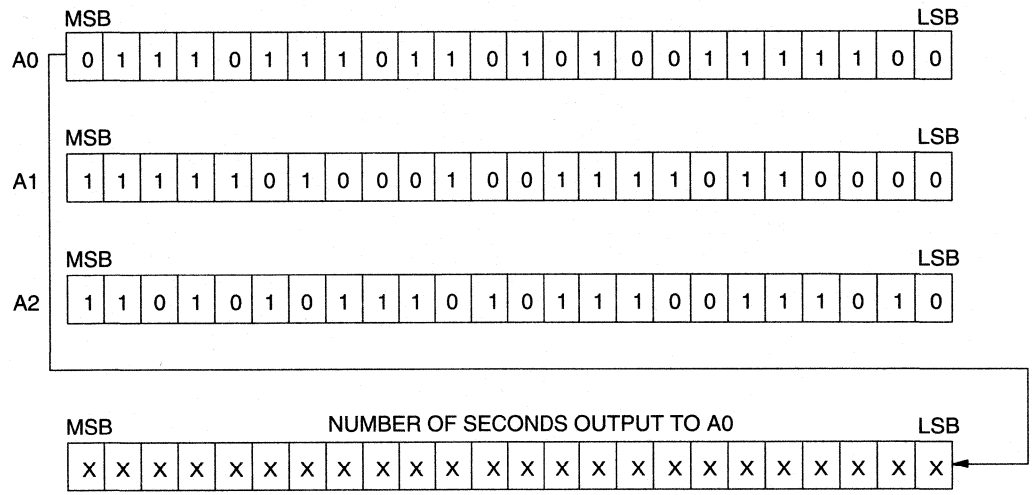
Calculating the actual current consumption of the DRAMs requires special attention since they are placed into the standby mode and then activated only when refreshing is required. This means that the current consumption of the DRAMs will be an average of the standby current and the active currents weighted in proportion to the refresh cycle time and duration.

SOFTWARE SEQUENCE FOR SETTING THE BACKUP CONDITION COUNTER Figure 3



NOTE:
The binary count which is entered into the backup condition counter is a calculated value based on application and has a range of 2^{24} seconds with an accuracy of ±20%.

SOFTWARE SEQUENCE FOR READING THE BACKUP CONDITION COUNTER Figure 4



DS1237 NONVOLATIZER DRAM DATA RETENTION TIMES Figure 5

$I_{datareten}$ = (# of DRAMs) X [(I_{act} + I_{std}) / 8E–3] + 4 mA

where,

I_{act} = 520 X 350E–9 X I_{active}

520 => number of refresh cycles (burst)

350E–9 => access cycle time of DRAM, and

I_{active} => active current draw of DRAM

I_{std} = (8E–3 – (520 X 350E–9)) X $I_{standby}$

8E–3 => refresh period

520 => number of refresh cycles (burst)

350E–9 => access cycle time of DRAM, and

$I_{standby}$ => standby current draw of DRAM

The foregoing equations can then be used to directly calculate the data retention time:

$$t_{datareten} = Q_{bat} / I_{datareten}$$

ABSOLUTE MAXIMUM RATINGS *

Voltage on Battery Input Pin Relative To Ground	-0.3V to +12V
Voltage on any Other Pin Relative to Ground	-0.3V to +7V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Primary Power Supply	V_{CCI}	4.5	5.0	5.5	V	1
Voltage Input Logic 1	V_{IH}	2.0		V_{CC}+0.3V	V	1
Voltage Input Logic 0	V_{IL}	-0.3		+0.8	V	1
Backup Supply	BKUP	6.0V	8.0V	10.0	V	2,3

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.50V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-2.0			mA	1,5
Output Current @ 0.4 V	I_{OL}	+8.0			mA	1,5
Input Supply Current	I_{CCI}		3	7	mA	6
Output Supply Current V_{CCO}=V_{CCI} -0.2 V	I_{CCO}			200	mA	4
$\overline{PF}$ Detect TOL = V_{CCO}	V_{TP}	4.5	4.62	4.75	V	7
$\overline{PF}$ Detect TOL = GND	V_{TP}	4.25	4.37	4.5	V	7
Output Supply Current V_{CCI} < V_{TP}	I_{CCOB}			30	mA	8
Backup Supply Leakage	I_{BKUP}			1	µA	9

CAPACITANCE

(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	7		pF	

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AC ELECTRICAL CHARACTERISTICS – RAPID REFRESH

(0°C to 70°C; $V_{CCI} < V_{TP}$)

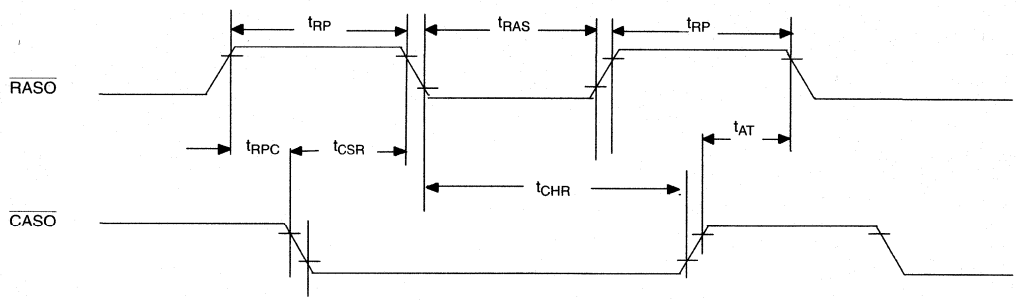
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{RASO}$ Precharge Time	t_{RP}	90			ns	
$\overline{RASO}$ Precharge to $\overline{CASO}$ Hold Time	t_{RPC}	60			ns	
$\overline{CASO}$ Setup Time	t_{CSR}	30			ns	
$\overline{CASO}$ Hold Time	t_{CHR}	60			ns	
$\overline{RASO}$ Pulse Width	t_{RAS}	0.120		10	µs	
Elapsed Time Between Rapid Refresh Burst	t_{AT}	SEE TABLE 1			ms	

AC ELECTRICAL CHARACTERISTICS

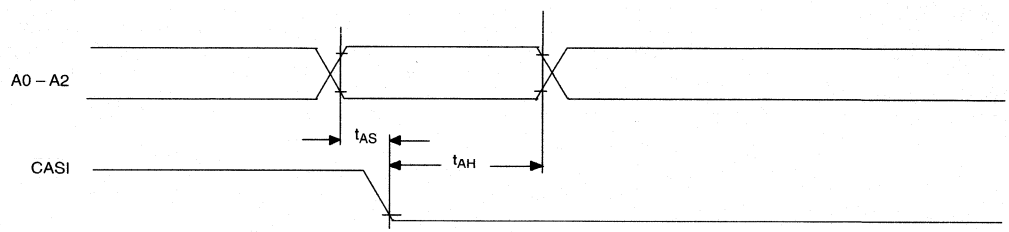
(0°C to 70°C; $V_{CCI} > V_{TP}$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup Time	t_{AS}	0			ns	
Address Hold Time	t_{AH}	20			ns	
Propagation Delay	t_{PD}		7	15	ns	

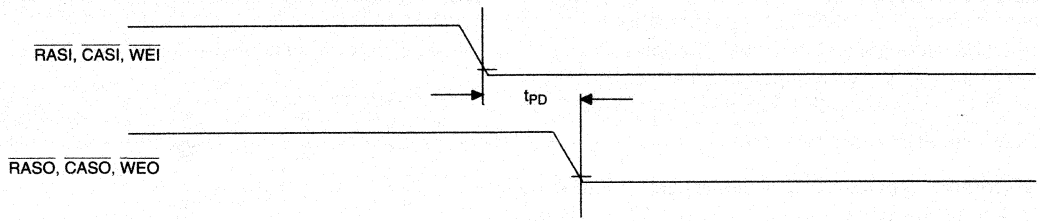
REFRESH CYCLE DURING BURST REFRESH RETENTION ($\overline{WEO}=V_{IH}$) Figure 6



SOFTWARE SEQUENCE ENTRY ($\overline{WEI}=V_{IH}$) Figure 7



PROPAGATION DELAY - NORMAL OPERATION Figure 8



NOTES:

1. All voltages are referenced to ground.
2. The $\overline{BC}$ pin will be driven active whenever V_{CC} is within nominal limits and the backup supply is below V_{CC}.
3. Backup input voltage is internally regulated within the DS1237 such that V_{CCO} is never below 4.5 volts for a backup input voltage of 6.0 volts minimum.
4. I_{CCO} is the maximum current which the DS1237 can supply to RAM through the V_{CCO} pin with a voltage drop of less than 0.2 volts.
5. Load capacity is 300 pF.
6. Measured with all outputs open.
7. V_{TP} is the trip point where the internal switching circuits disconnect V_{CCI} and connect the internally regulated backup supply to V_{CCO}. Rapid refresh is also initiated at this time, and the $\overline{PF}$ output is driven active.
8. I_{CCOB} is the maximum current the DS1237 can supply to RAM through the V_{CCO} pin from the internally regulated supply while in the data retention mode.
9. Backup leakage is the internal current consumed by the DS1237 in the data retention mode, with battery backup disabled.

APPLICATION NOTE: DIODE CONTROL OF BACKUP INPUT

The fabrication of the DS1237 produces an N well for the BKUP input (pin 14) that must be considered by the user. Because of this it is imperative that the BKUP input does not go more negative from V_{CCI} input (pin 16) than the amount of one silicon diode.

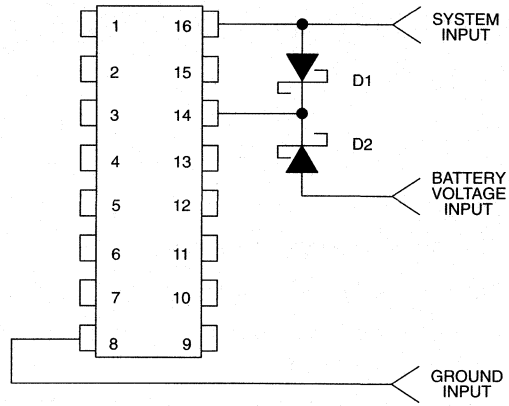
This requirement can be achieved by using a Schottky diode (D1) between the V_{CCI} input and BKUP input (see example below). This diode will limit the negative voltage level of BKUP input relative to the V_{CCI}.

A Shottky diode is required for D1.

Eventually the battery voltage that is applied to the BKUP input can decrease below the negative clamp voltage of D1. At this time, the battery should be disconnected from the circuit during the time that V_{CCI} input is present.

This can be achieved by using a diode (D2) between the battery positive supply lead and the BKUP input. Diode D2 will then disconnect the battery positive supply lead from the BKUP input when the battery output voltage has decreased.

A Shottky diode is suggested for D2.



NOTE: For circuits where the BKUP source is a primary battery, Underwriter Laboratories requires D2.

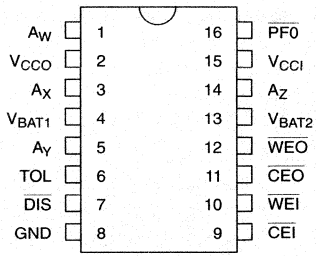
DALLAS SEMICONDUCTOR

DS1610
Partitioned NV Controller

FEATURES

- Converts CMOS RAMs into nonvolatile memories
- SOIC version is pin compatible with the Dallas Semiconductor DS1210 NV Controller
- Unconditionally write protects all of memory when V_{CC} is out of tolerance
- Write protects selected blocks of memory regardless of V_{CC} status when programmed
- Automatically switches to battery backup supply when power fail occurs
- Provides for multiple batteries
- Consumes less than 100 nA of battery current
- Test battery on power up by inhibiting the second memory cycle
- Optional 5% or 10% Power Fail Detection
- 16-pin DIP or 16-pin SOIC Surface Mount Package
- Low forward voltage drop on the V_{CC} switch with currents of up to 150 mA
- Optional industrial temperature range of -40°C to +85°C

PIN ASSIGNMENT



16-Pin DIP and 16-Pin SOIC

PIN DESCRIPTION

V_{CCI}	–	Input +5 Volt Supply
V_{BAT1}	–	+ Battery 1 Input
V_{BAT2}	–	+ Battery 2 Input
V_{CCO}	–	RAM Power (V_{CC}) Supply
GND	–	Ground
$\overline{CEI}$	–	Chip Enable Input
$\overline{CEO}$	–	Chip Enable Output
$\overline{WEI}$	–	Write Enable Input
$\overline{WEO}$	–	Write Enable Output
TOL	–	Power Supply Tolerance Select
A_W - A_Z	–	Address Inputs
$\overline{DIS}$	–	Memory Partition Disable
$\overline{PF0}$	–	Power Fail Output

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DESCRIPTION

The DS1610 is a low power CMOS circuit which solves the application problems of converting CMOS RAMS into nonvolatile memories. In addition the device has the ability to unconditionally write protect blocks of memory so that inadvertent write cycles do not corrupt program and special data space. The power supply incoming voltage at the V_{CCI} input pin is constantly monitored for an out of tolerance condition. When such a condition is detected, both the chip enable and write enable outputs are inhibited to protect stored data. The battery inputs are used to supply V_{CCO} with power when V_{CCI} is less than the battery input voltages. Special circuitry uses a low leakage CMOS process which affords precise voltage detection at extremely low current consumption. By combining the DS1610 Partitioned NV Controller chip with a CMOS memory and batteries, nonvolatile RAM operation can be achieved.

The DS1610 Partitioned NV Controller functions like the Dallas Semiconductor DS1210 NV controller when the ($\overline{DIS}$) disable pin is grounded. An internal pulldown resistor to ground on the $\overline{DIS}$ pin of the DS1610S allows it to retrofit into DS1210S applications. When the $\overline{DIS}$ pin is grounded the address inputs A_W - A_Z and the write enable input $\overline{WEI}$ are ignored. Also the power fail output $\overline{PFO}$ and the write enable output $\overline{WEO}$ are tristated.

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OPERATION – DISABLE PIN CONNECTED TO V_{CCO}

The DS1610 performs five circuit functions required to battery backup a RAM. First, a switch is provided to direct power from the battery or the incoming power supply (V_{CCI}) depending on which is greater. This switch has a voltage drop of less than 0.2 volts. The second function provided by the DS1610 is power fail detection. The incoming supply (V_{CCI}) is constantly monitored. When the supply goes out of tolerance a precision comparator detects power failure and inhibits both the chip enable output ($\overline{CEO}$) and the write enable output ($\overline{WEO}$). A third function of write protection is accomplished by holding both the chip enable output $\overline{CEO}$ and write enable output $\overline{WEO}$ to within 0.2 volts of V_{CCO} when V_{CCI} is out of tolerance. If $\overline{CEI}$ is low at the time that power fail detection occurs the $\overline{CEO}$ signal is kept low until $\overline{CEI}$ is brought high again. However, $\overline{CEO}$ is forced high after 1.5 µsec regardless of the state of $\overline{CEI}$. Similarly, if $\overline{WEI}$ is low at the time that power fail detection occurs, the $\overline{WEO}$ is signal will remain low until $\overline{WEI}$ is brought high or 1.5 µsec elapses. The delay of write protection until the current memory cycle is complete prevents corrupted data. Power fail detection occurs in the range of 4.75 to 4.5 volts with the tolerance pin TOL grounded. If the tolerance pin is connected to V_{CCO} then power fail detection occurs in the range of 4.5 volts to 4.25 volts. The $\overline{PF0}$ signal is driven low and remains low until V_{CCI} returns to nominal conditions. During nominal supply conditions $\overline{CEO}$ will follow $\overline{CEI}$ and $\overline{WEO}$ will follow $\overline{WEI}$. The fourth function which the DS1610 performs is a battery status warning so that potential data loss is avoided. Each time V_{CCI} is applied to the device battery status is checked with a precision comparator. If during battery backup, no switch occurred from one battery to the other, the voltage of the battery supplying power when V_{CCI} is applied is checked. If this voltage is less than 2.0 volts the second chip enable cycle after power is applied is inhibited. If any switch from one battery to another did occur the voltage of both batteries is checked. If either voltage is less than 2.0 volts the second chip enable cycle will be inhibited. Battery status can therefore be determined by performing a read cycle after power up to any location in memory, verifying that memory location's contents. A subsequent write cycle can then be executed to the same memory location altering the data. If the next read cycle fails to verify the written data then the data is in danger of being corrupted. The fifth function of the DS1610 provides for battery redundancy. When data integrity is extremely important it is wise to use two batteries to insure reliability. The DS1610 controller provides an internal isolation switch which allows the connection of two batteries. When entering battery backup operation, the battery with the highest voltage is selected for use. If one battery should fail, the other would then supply energy to the connected load. The switch to a redundant battery is transparent to circuit operation and to the user. In applications where battery redundancy is not a major concern a single battery should be connected to the BAT1 pin. The BAT2 battery pin must be grounded. When batteries are first connected to one or both of the V_{BAT} pins V_{CCO} will not show the battery potential until V_{CCI} is applied and removed for the first time.

OPERATION – WRITE PROTECTION PROGRAMMING MODE

When the disable pin is connected to V_{CCI} or V_{CCO}, the DS1610 performs all of the functions described earlier with the addition of a partition switch which selectively write protects blocks of memory. The state of the $\overline{DIS}$ pin is strobed and latched as V_{CCI} crosses the power fail trip point so that the DS1610 maintains its configuration during power loss. If the strobed value of $\overline{DIS}$ is a high the internal pulldown resistor on the $\overline{DIS}$ pin will be disconnected in the power fail state to eliminate the possibility of battery discharge. The register controlling the partition switch is selected by recognition of a specific binary pattern which is sent on address lines A_W-A_Z. These address lines are normally the four upper order address lines being sent to RAM. The pattern is sent by 20 consecutive read cycles with the exact pattern as shown in Table 1. Pattern matching must be accomplished using read cycles; any write cycles will reset the pattern matching circuitry. If this pattern is matched perfectly, then the 21st through 24th read cycle will load the partition switch. Since there are 16 possible write protected partitions, the size of each partition is determined by the size of the memory. For example, a 128K X 8 memory would be divided into 16 partitions of 128K/16 or 8K X 8. Each partition is represented by one of the 16 bits contained in the 21st through 24th read cycle as defined by A_W through A_Z and shown in Table 2. A logical 1 in a bit location sets that partition to write protect. A logical 0 in a bit location disables write protection. For example, if during the pattern match sequence bit 22 on address pin A_X was a 1, this would cause the partition register location for partition 5 to be set to a 1. This in turn would cause the DS1610 to inhibit $\overline{WEO}$ from going low as $\overline{WEI}$ goes low whenever $A_Z A_Y A_X A_W$=0101. Note that while setting the partition register, data which is be-

ing accessed from the RAM should be ignored as the purpose of the 24 read cycles is to set the partition switch and not for the purpose of accessing data from RAM. Also note that on initial battery attach the partition register can power up in any state.

PATTERN MATCH TO WRITE PARTITION REGISTER Table 1

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A_W	1	0	1	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	1	X	X	X	X
A_X	1	1	1	1	1	0	0	1	1	1	0	0	1	0	1	1	0	0	0	0	X	X	X	X
A_Y	1	1	1	1	0	0	1	1	1	0	0	1	0	1	0	1	0	0	0	1	X	X	X	X
A_Z	1	1	0	0	0	1	1	1	0	0	1	0	0	0	1	0	1	0	0	0	X	X	X	X

PARTITION REGISTER MAPPING Table 2

Address Pin	Bit number in pattern match sequence	Partition Number	Address State Affected (A_Z A_Y A_X A_W)
A_W	BIT 21	PARTITION 0	0000
A_X	BIT 21	PARTITION 1	0001
A_Y	BIT 21	PARTITION 2	0010
A_Z	BIT 21	PARTITION 3	0011
A_W	BIT 22	PARTITION 4	0100
A_X	BIT 22	PARTITION 5	0101
A_Y	BIT 22	PARTITION 6	0110
A_Z	BIT 22	PARTITION 7	0111
A_W	BIT 23	PARTITION 8	1000
A_X	BIT 23	PARTITION 9	1001
A_Y	BIT 23	PARTITION 10	1010
A_Z	BIT 23	PARTITION 11	1011
A_W	BIT 24	PARTITION 12	1100
A_X	BIT 24	PARTITION 13	1101
A_Y	BIT 24	PARTITION 14	1110
A_Z	BIT 24	PARTITION 15	1111

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pin 6 = GND Supply Voltage	V_{CCI}	4.75	5.0	5.5	V	1
Pin 6 = V_{CCO} Supply Voltage	V_{CCI}	4.5	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.0		V_{CC} + 0.3	V	1
Logic 0 Input	V_{IL}	-0.3		+0.8	V	1
Battery Input	V_{BAT1} V_{BAT2}	2.0		4.0	V	1, 2

DC ELECTRICAL CHARACTERISTICS ($0°C$ TO $70°C$, V_{CCI} WITHIN DC OPERATING CONDITIONS)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Operating Current	I_{CC1}			5	mA	3, 14
Standby Current	I_{CC2}			200	µA	3, 15
Supply Voltage	V_{CCO}	V_{CC} -0.2			V	1
Supply Current	I_{CCO1}			150	mA	4
Input Leakage	I_{IL}	-1.0		+1.0	µA	
Output Leakage	I_{LO}	-1.0		+1.0	µA	
V_{CC} Trip Point (TOL=GND)	V_{CCTP}	4.50	4.62	4.75	V	1, 16
V_{CC} Trip Point (TOL=V_{CC})	V_{CCTP}	4.25	4.37	4.50	V	1, 16
$\overline{CEI}$ to $\overline{CEO}$ Impedance	Z_{CE}			30	Ω	5
$\overline{DIS}$ Pulldown Resistance	R_{DIS}	50K		250K	Ω	
$\overline{PFO}$, $\overline{WEO}$ Output @ 2.4V	I_{OH}	–1.0			mA	10, 16
$\overline{PFO}$, $\overline{WEO}$ Output @ 0.4V	I_{OH}			4.0	mA	10, 16

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CCI}<V_{BAT})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CEO}$ Output	V_{OHL}	V_{BAT}-0.2			V	
$\overline{WEO}$ Output	V_{OHL}	V_{BAT}-0.2			V	
V_{BAT1} or V_{BAT2} Battery Current	I_{BAT}			100	nA	2, 3
Battery Backup Current @ V_{CCO} = V_{BAT} -0.2V	I_{CCO2}			150	µA	6, 7, 8

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CCI}=4.75V to 5.50V, TOL=GND
V_{CCI}=4.50V to 5.50V, TOL–V_{CCO})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t_{AS}	0			ns	9
Address Hold	t_{AH}	50			ns	9
Read Recovery	t_{RR}	10			ns	9
$\overline{CEI}$, $\overline{WEI}$ Pulse Width	t_{CW}	75			ns	9
$\overline{CEI}$ to $\overline{CEO}$ Falling Propagation Delay	t_{PDF}			5	ns	10
Later of $\overline{CEI}$, $\overline{WEI}$ to $\overline{WEO}$ Falling Propagation Delay	t_{PDF}			20	ns	10, 11
$\overline{CEI}$ to $\overline{CEO}$ Rising Propagation Delay	t_{PDR}			5	ns	10
Earlier of $\overline{CEI}$, $\overline{WEI}$ to $\overline{WEO}$ Rising Propagation Delay	t_{PDR}			5	ns	10, 11
Write Recovery	t_{WR}	10			ns	9, 11

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}<4.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power Up	t_{REC}	25		125	ms	12
V_{CC} Slew Rate Power Down	t_F	300			µs	
V_{CC} Slew Rate Power Down	t_{FB}	10			µs	
V_{CC} Slew Rate Power Up	t_F	0			µs	13
$\overline{CEO}$ Pulse Width	t_{WP}, t_{CE}			1.5	µs	7, 8
$\overline{WEO}$ Pulse Width	t_{WP}, t_{CE}			1.5	µs	7, 8

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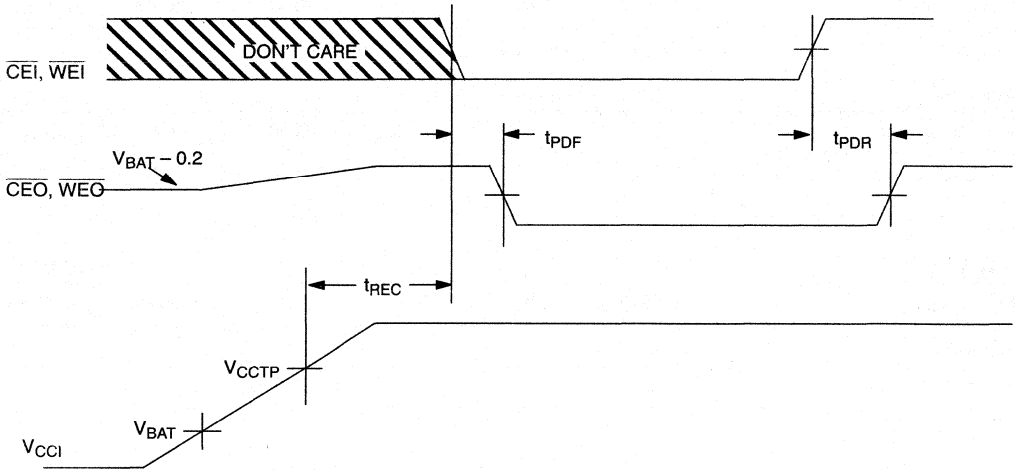
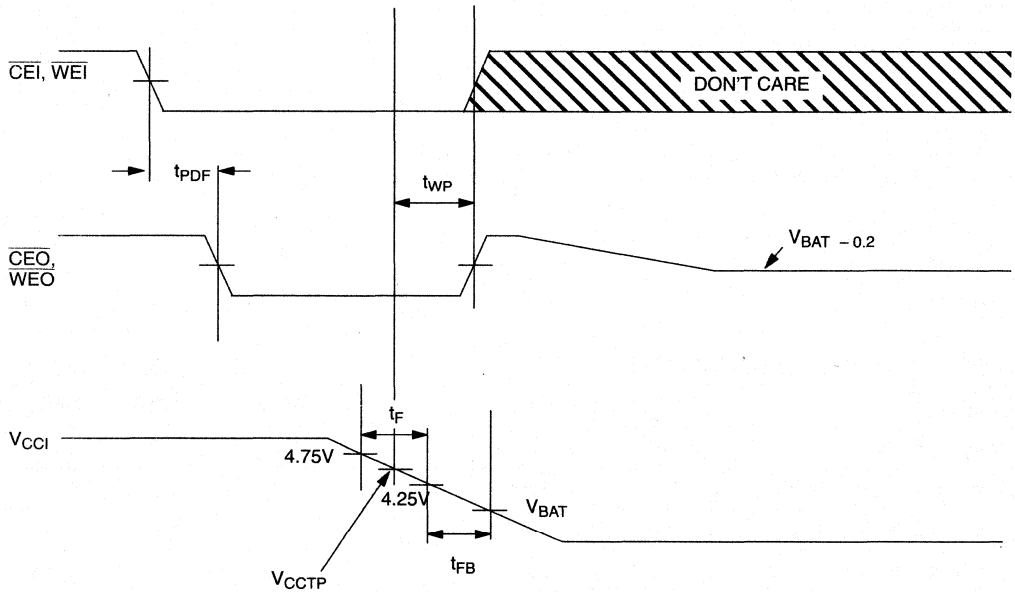
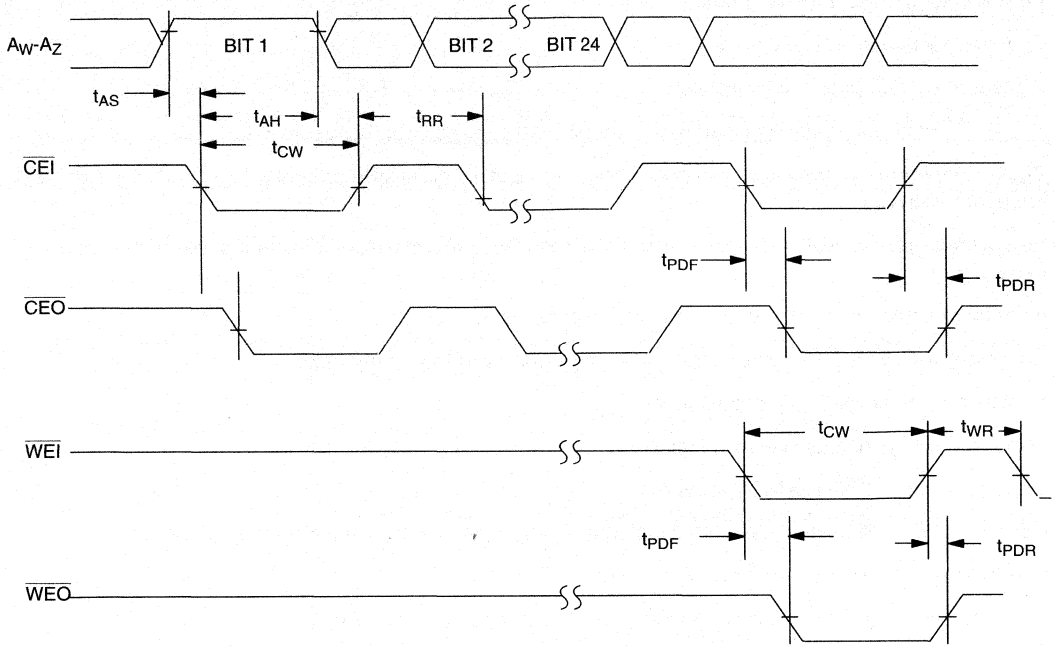
TIMING DIAGRAM: POWER UP



TIMING DIAGRAM: POWER DOWN



TIMING DIAGRAM: LOADING PARTITION REGISTER



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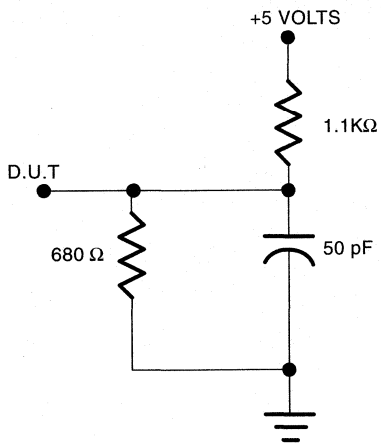
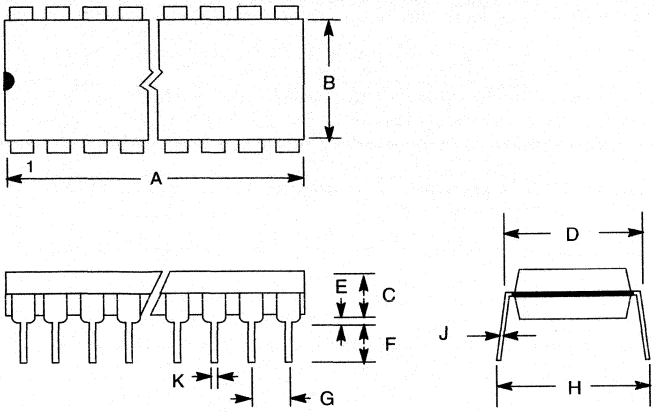
OUTPUT LOAD Figure 1



NOTES:

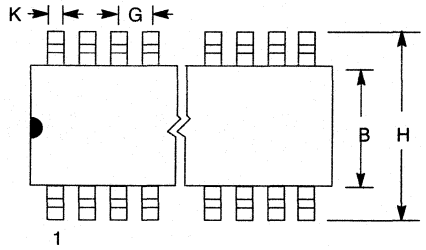
1. All voltages are reference to ground
2. Only one battery input is required.
3. Measured with outputs open circuited.
4. I_{CC01} is the maximum average load which the DS1610 can supply to the memories.
5. Z_{CE} is an average input-to-output impedance as the input is swept from ground to V_{CCI} and less than 4 mA is forced through Z_{CE}.
6. I_{CC02} is the maximum average load current which the DS1610 can supply to the memories in the battery backup mode.
7. t_{CE} max must be met to insure data integrity on power loss.
8. Chip Enable Output $\overline{CEO}$ can only sustain leakage current in the battery mode.
9. Applies only when loading partition switch.
10. Measured with a load as shown in Figure 1.
11. Measured with $\overline{DIS}$ at a logic high level.
12. $\overline{CEO}$ and $\overline{WEO}$ will be held high for a time equal to t_{REC} (max = 125 msec) after V_{CCI} crosses V_{CCTP}.
13. t_R is the slew rate of V_{CCI} from 4.25V to 4.75V.
14. $\overline{CEI}$, $\overline{WEI}$, A_W - A_Z run at minimum timing set and at voltage levels of 0V to 3V.
15. All inputs within 0.3V of ground or V_{CCI} and $\overline{CEI}$ within 0.3V of V_{CCI}.
16. The power fail output signal ($\overline{PFO}$) is driven active (V_{OL} = 0.4V) when the V_{CC} trip point occurs. While active, the $\overline{PFO}$ pin can sink 4 mA and will maintain a maximum output voltage of 0.4 volts. When inactive, the voltage output of $\overline{PFO}$ is 2.4 volts minimum and will source a current of 1 mA.

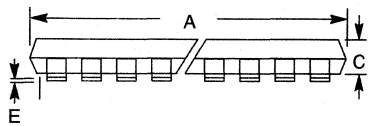
DS1610 16–PIN DIP (300 MIL)

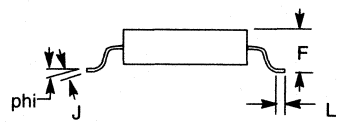


PKG	16-PIN	
DIM	MIN	MAX
A IN. MM	0.740 18.80	0.780 19.81
B IN. MM	0.240 6.10	0.260 6.60
C IN. MM	0.120 3.05	0.140 3.56
D IN. MM	0.300 7.62	0.325 8.26
E IN. MM	0.015 0.38	0.040 1.02
F IN. MM	0.120 3.04	0.140 3.56
G IN. MM	0.090 2.29	0.110 2.79
H IN MM	0.320 8.13	0.370 9.40
J IN MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53

DS1610 16–PIN SOIC (300 MIL)







PKG	16-PIN	
DIM	MIN	MAX
A IN. MM	0.402 10.21	0.412 10.46
B IN. MM	0.290 7.37	0.300 7.65
C IN. MM	0.089 2.26	0.095 2.41
E IN. MM	0.004 0.102	0.012 0.30
F IN. MM	0.094 2.38	0.105 2.68
G IN. MM	.050 BSC 1.27 BSC	
H IN MM	0.398 10.11	0.416 10.57
J IN MM	0.009 0.229	0.013 0.33
K IN. MM	0.013 0.33	0.019 0.48
L IN MM	.016 .40	.040 1.02
PHI	0°	8°

DALLAS SEMICONDUCTOR

DS1710
Partitioned NV Controller

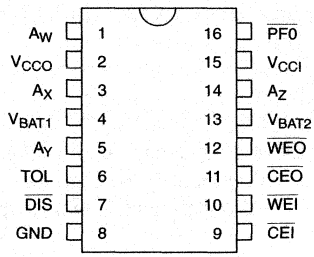
FEATURES

- Converts CMOS RAMs into nonvolatile memories
- Automatically selects +3.0V or +5.0V operation
- SOIC version is pin compatible with the Dallas Semiconductor DS1210S and DS1610S NV Controllers
- Unconditionally write protects all of memory when V_{CC} is out of tolerance
- Write protects selected blocks of memory regardless of V_{CC} status when programmed
- Automatically switches to battery backup supply when power fail occurs
- Provides for multiple batteries
- Consumes less than 100 nA of battery current
- Tests battery on power up by inhibiting the second memory cycle
- Optional 5% or 10% Power Fail Detection
- 16-pin DIP or 16-pin SOIC surface mount package or 20–pin TSSOP package
- Low forward voltage drop on the V_{CC} switch with currents of up to 150 mA
- Optional industrial temperature range of -40°C to +85°C

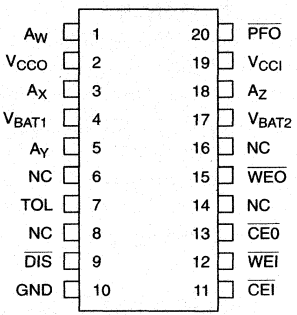
DESCRIPTION

The DS1710 is a low power CMOS circuit which solves the application problems of converting CMOS RAMS into nonvolatile memories. In addition the device has the ability to unconditionally write protect blocks of memory so that inadvertent write cycles do not corrupt program and special data space. The incoming power supply voltage at the V_{CCI} input pin is constantly monitored for an out of tolerance condition. When such a condition is detected, both the chip enable and write enable outputs are inhibited to protect stored data. The battery inputs are used to supply V_{CCO} with power when

PIN ASSIGNMENT



16-Pin DIP and 16-Pin SOIC



20–Pin TSSOP

PIN DESCRIPTION

V_{CCI}	–	Input 2.7 to 5.5 Volt Supply
V_{BAT1}	–	+ Battery 1 Input
V_{BAT2}	–	+ Battery 2 Input
V_{CCO}	–	RAM Power (V_{CC}) Supply
GND	–	Ground
$\overline{CEI}$	–	Chip Enable Input
$\overline{CEO}$	–	Chip Enable Output
$\overline{WEI}$	–	Write Enable Input
$\overline{WEO}$	–	Write Enable Output
TOL	–	Power Supply Tolerance Select
A_W - A_Z	–	Address Inputs
$\overline{DIS}$	–	Memory Partition Disable
$\overline{PF0}$	–	Power Fail Output
NC	–	No Connect

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V_{CCI} is less than the battery input voltages. Special circuitry uses a low leakage CMOS process which affords precise voltage detection at extremely low current consumption. By combining the DS1710 Partitioned NV Controller chip with a CMOS memory and batteries, nonvolatile RAM operation can be achieved.

The DS1710 Partitioned NV Controller incorporates all the functions of the DS1610 with the additional feature of either +3.0V or +5.0V operation. The DS1710 functions like the Dallas Semiconductor DS1210 NV controller when the ($\overline{DIS}$) disable pin is grounded and also incorporates the power–up auto sensing. An internal pulldown resistor to ground on the $\overline{DIS}$ pin of the DS1710S allows it to retrofit into DS1210S applications. When the $\overline{DIS}$ pin is grounded the address inputs A_W - A_Z and the write enable input $\overline{WEI}$ are ignored. Also the power fail output $\overline{PFO}$ and the write enable output $\overline{WEO}$ are tristated.

POWER–UP AUTO SENSING

V_{CCI} will accept either +3.0V or +5.0V input. Selection of 3V operation is automatically invoked when V_{CC} rises and remains between V_{CCTP2} and V_{CCTP1} for t_{REC}. 5V operation is automatically selected if V_{CC} rises and remains above both V_{CCTP2} and V_{CCTP1} for t_{REC}. In either case, t_{REC} is measured from the time V_{CC} first rises above V_{CCTP2}. The DS1710 will not change modes until V_{CC} falls below V_{CCTP2}.

OPERATION – DISABLE PIN CONNECTED TO V_{CCO}

The DS1710 performs five circuit functions required to battery back up a RAM. First, a switch is provided to direct power from the battery or the incoming power supply (V_{CCI}) depending on which is greater. This switch has a voltage drop of less than 0.2 volts. The second function provided by the DS1710 is power fail detection. The incoming supply (V_{CCI}) is constantly monitored. When the supply goes out of tolerance a precision comparator detects power failure and inhibits both the chip enable output ($\overline{CEO}$) and the write enable output ($\overline{WEO}$). A third function of write protection is accomplished by holding both the chip enable output $\overline{CEO}$ and write enable output $\overline{WEO}$ to within 0.2 volts of V_{CCO} when V_{CCI} is out of tolerance. If $\overline{CEI}$ is low at the time that power fail detection occurs the $\overline{CEO}$ signal is kept low until $\overline{CEI}$ is brought high again. However, $\overline{CEO}$ is forced high after 1.5 µsec regardless of the state of $\overline{CEI}$. Similarly, if $\overline{WEI}$ is low at the time that power fail detection occurs, the $\overline{WEO}$ is signal will remain low until $\overline{WEI}$ is brought high or 1.5 µsec elapses. The delay of write protection until the current memory cycle is complete prevents corrupted data. Power fail detection occurs in the range of 4.75 to 4.5 volts with the tolerance pin TOL grounded and in 5 volt mode. If the tolerance pin is connected to V_{CCO} while in 5 volt mode, then power fail detection occurs in the range of 4.5 volts to 4.25 volts. If in 3 volt mode, the power fail detection will occur in the range of 2.7 to 2.5 volts. The $\overline{PFO}$ signal is driven low and remains low until V_{CCI} returns to nominal conditions. During nominal supply conditions $\overline{CEO}$ will follow $\overline{CEI}$ and $\overline{WEO}$ will follow $\overline{WEI}$. The fourth function which the DS1710 performs is a battery status warning so that potential data loss is avoided. Each time V_{CCI} is applied to the device battery status is checked with a precision comparator. If during battery backup, no switch occurred from one battery to the other, the voltage of the battery supplying power when V_{CCI} is applied is checked. If this voltage is less than 2.0 volts the second chip enable cycle after power is applied is inhibited. If any switch from one battery to another did occur the voltage of both batteries is checked. If either voltage is less than 2.0 volts the second chip enable cycle will be inhibited. Battery status can therefore be determined by performing a read cycle after power up to any location in memory, verifying that memory location's contents. A subsequent write cycle can then be executed to the same memory location altering the data. If the next read cycle fails to verify the written data then the data is in danger of being corrupted. The fifth function of the DS1710 provides for battery redundancy. When data integrity is extremely important it is wise to use two batteries to insure reliability. The DS1710 controller provides an internal isolation switch which allows the connection of two batteries. When entering battery backup operation, the battery with the highest voltage is selected for use. If one battery should fail, the other would then supply energy to the connected load. The switch to a redundant battery is transparent to circuit operation and to the user. In applications where battery redundancy is not a major concern a single battery should be connected to the BAT1 pin. The BAT2 battery pin must be grounded. When batteries are first connected to one or both of the V_{BAT} pins V_{CCO} will not show the battery potential until V_{CCI} is applied and removed for the first time.

OPERATION – WRITE PROTECTION PROGRAMMING MODE

When the disable pin is connected to V_{CCI} or V_{CCO}, the DS1710 performs all of the functions described earlier with the addition of a partition switch which selectively write protects blocks of memory. The state of the $\overline{DIS}$ pin is strobed and latched as V_{CCI} crosses the power fail trip point so that the DS1710 maintains its configuration during power loss. If the strobed value of $\overline{DIS}$ is high, the internal pulldown resistor on the $\overline{DIS}$ pin will be disconnected in the power fail state to eliminate the possibility of battery discharge. The register controlling the partition switch is selected by recognition of a specific binary pattern which is sent on address lines A_W-A_Z. These address lines are normally the four upper order address lines being sent to RAM. The pattern is sent by 20 consecutive read cycles with the exact pattern as shown in Table 1. Pattern matching must be accomplished using read cycles; any write cycles will reset the pattern matching circuitry. If this pattern is matched perfectly, then the 21st through 24th read cycle will load the partition switch. Since there are 16 possible write protected partitions, the size of each partition is determined by the size of the memory. For example, a 128K X 8 memory would be divided into 16 partitions of 128K/16 or 8K X 8. Each partition is represented by one of the 16 bits contained in the 21st through 24th read cycle as defined by A_W through A_Z and shown in Table 2. A logical 1 in a bit location sets that partition to write protect. A logical 0 in a bit location disables write protection. For example, if during the pattern match sequence bit 22 on address pin A_X was a 1, this would cause the partition register location for partition 5 to be set to a 1. This in turn would cause the DS1710 to inhibit $\overline{WEO}$ from going low as $\overline{WEI}$ goes low whenever $A_ZA_YA_XA_W$=0101. Note that while setting the partition register, data which is being accessed from the RAM should be ignored as the purpose of the 24 read cycles is to set the partition switch and not for the purpose of accessing data from RAM. Also note that on initial battery attach the partition register can power up in any state.

PATTERN MATCH TO WRITE PARTITION REGISTER Table 1

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A_W	1	0	1	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	1	X	X	X	X
A_X	1	1	1	1	1	0	0	1	1	1	0	0	1	0	1	1	0	0	0	0	X	X	X	X
A_Y	1	1	1	1	0	0	1	1	1	0	0	1	0	1	0	1	0	0	0	1	X	X	X	X
A_Z	1	1	0	0	0	1	1	1	0	0	1	0	0	0	1	0	1	0	0	0	X	X	X	X

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PARTITION REGISTER MAPPING Table 2

Address Pin	Bit number in pattern match sequence	Partition Number	Address State Affected (A_Z A_Y A_X A_W)
A_W	BIT 21	PARTITION 0	0000
A_X	BIT 21	PARTITION 1	0001
A_Y	BIT 21	PARTITION 2	0010
A_Z	BIT 21	PARTITION 3	0011
A_W	BIT 22	PARTITION 4	0100
A_X	BIT 22	PARTITION 5	0101
A_Y	BIT 22	PARTITION 6	0110
A_Z	BIT 22	PARTITION 7	0111
A_W	BIT 23	PARTITION 8	1000
A_X	BIT 23	PARTITION 9	1001
A_Y	BIT 23	PARTITION 10	1010
A_Z	BIT 23	PARTITION 11	1011
A_W	BIT 24	PARTITION 12	1100
A_X	BIT 24	PARTITION 13	1101
A_Y	BIT 24	PARTITION 14	1110
A_Z	BIT 24	PARTITION 15	1111

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pin 6=GND Supply Voltage (5V Operation)	V_{CCI}	4.75	5.0	5.5	V	1
Pin 6 = V_{CCO} Supply Voltage (5V Operation)	V_{CCI}	4.5	5.0	5.5	V	1
Pin 6=GND Supply Voltage (3V Operation)	V_{CCI}	2.7	3.0	4.0	V	1
Logic 1 Input	V_{IH}	2.0		V_{CC} + 0.3	V	1
Logic 0 Input	V_{IL}	-0.3		+0.8	V	1
Battery Input	V_{BAT1} V_{BAT2}	2.0		4.0	V	1, 2

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CCI}<V_{BAT}, V_{CCI}<V_{CCTP2})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CEO}$ Output	V_{OHL}	V_{BAT}-0.2			V	
$\overline{WEO}$ Output	V_{OHL}	V_{BAT}-0.2			V	
V_{BAT1} or V_{BAT2} Battery Current	I_{BAT}			100	nA	2, 3
Battery Backup Current @ V_{CCO} = V_{BAT} -0.2V	I_{CCO2}			150	µA	6, 8

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CCI}=4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Operating Current	I_{CC1}			5	mA	3, 14
Standby Current	I_{CC2}			200	µA	3, 15
Supply Voltage	V_{CCO}	V_{CC} -0.2			V	1
Supply Current	I_{CCO1}			150	mA	4
Input Leakage	I_{IL}	-1.0		+1.0	µA	
Output Leakage	I_{LO}	-1.0		+1.0	µA	
$\overline{PFO}$, $\overline{WEO}$ Output @ 2.4V	I_{OH}	–1.0			mA	10, 16
$\overline{PFO}$, $\overline{WEO}$ Output @ 0.4V	I_{OL}			4.0	mA	10, 16
V_{CC} Trip Point (TOL=GND)	V_{CCTP1}	4.50	4.62	4.75	V	1, 16
V_{CC} Trip Point (TOL=V_{CC})	V_{CCTP1}	4.25	4.37	4.50	V	1, 16
V_{CC} Trip Point	V_{CCTP2}	2.50	2.60	2.70	V	1, 16
$\overline{CEI}$ to $\overline{CEO}$ Impedance	Z_{CE}			30	Ω	5
$\overline{DIS}$ Pulldown Resistance	R_{DIS}	50K		250K	Ω	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CCI}=4.75V to 5.50V, TOL=GND
V_{CCI}=4.50V to 5.50V, TOL=V_{CCO})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
Read Recovery	t_{RR}	20			ns	9
$\overline{CEI}$, $\overline{WEI}$ Pulse Width	t_{CW}	75			ns	
$\overline{CEI}$ to $\overline{CEO}$ Falling Propagation Delay	t_{PDF}			5	ns	10
Later of $\overline{CEI}$, $\overline{WEI}$ to $\overline{WEO}$ Falling Propagation Delay	t_{PDF}			20	ns	10, 11
$\overline{CEI}$ to $\overline{CEO}$ Rising Propagation Delay	t_{PDR}			5	ns	10
Earlier of $\overline{CEI}$, $\overline{WEI}$ to $\overline{WEO}$ Rising Propagation Delay	t_{PDR}			5	ns	10, 11
Write Recovery	t_{WR}	10			ns	11

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; 5V Operation)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power Up	t_{REC}	100		200	ms	12
V_{CC} Slew Rate Power Down	t_F	300			µs	
V_{CC} Slew Rate Power Down	t_{FB}	10			µs	
V_{CC} Slew Rate Power Up	t_R	0			µs	13
$\overline{CEI}$ Pulse Width	t_{CE}			1.5	µs	7, 8
$\overline{WEI}$ Pulse Width	t_{CE}			1.5	µs	7, 8

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CCI}=2.7V to 4.0V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Operating Current	I_{CC1}			3	mA	3, 14
Standby Current	I_{CC2}			200	µA	3, 15
Supply Voltage	V_{CCO}	V_{CC} -0.2			V	1
Supply Current	I_{CCO1}			100	mA	4
Input Leakage	I_{IL}	-1.0		+1.0	µA	
Output Leakage	I_{LO}	-1.0		+1.0	µA	
$\overline{PFO}$, $\overline{WEO}$ Output @ 2.4V	I_{OH}	–1.0			mA	10, 16
$\overline{PFO}$, $\overline{WEO}$ Output @ 0.4V	I_{OL}			4.0	mA	10, 16
V_{CC} Trip Point	$V_{CCTP}2$	2.50	2.60	2.70	V	1, 16
$\overline{CEI}$ to $\overline{CEO}$ Impedance	Z_{CE}			60	Ω	5
$\overline{DIS}$ Pulldown Resistance	R_{DIS}	50K		250K	Ω	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CCI}=2.7V to 4.0V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
Read Recovery	t_{RR}	20			ns	9
$\overline{CEI}$, $\overline{WEI}$ Pulse Width	t_{CW}	75			ns	
$\overline{CEI}$ to $\overline{CEO}$ Falling Propagation Delay	t_{PDF}			5	ns	10
Later of $\overline{CEI}$, $\overline{WEI}$ to $\overline{WEO}$ Falling Propagation Delay	t_{PDF}			50	ns	10, 11
$\overline{CEI}$ to $\overline{CEO}$ Rising Propagation Delay	t_{PDR}			5	ns	10
Earlier of $\overline{CEI}$, $\overline{WEI}$ to $\overline{WEO}$ Rising Propagation Delay	t_{PDR}			20	ns	10, 11
Write Recovery	t_{WR}	10			ns	11

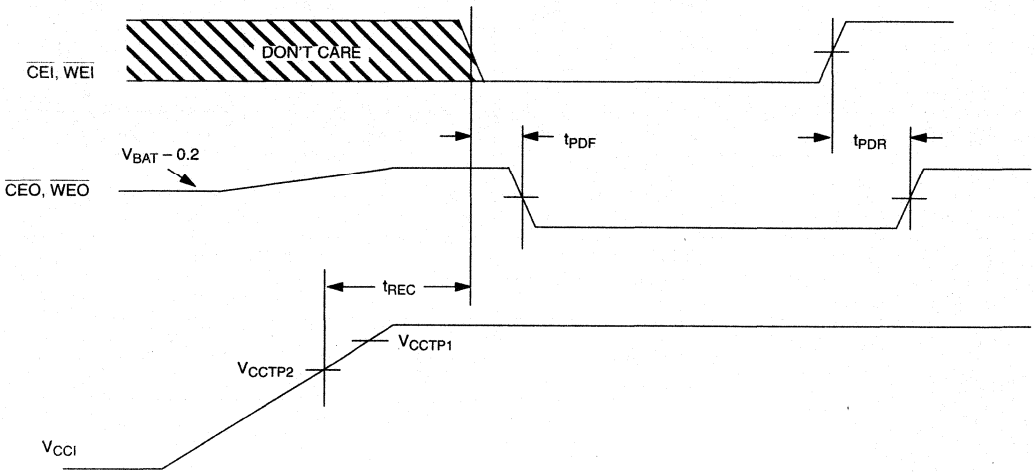
AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; 3V Operation)

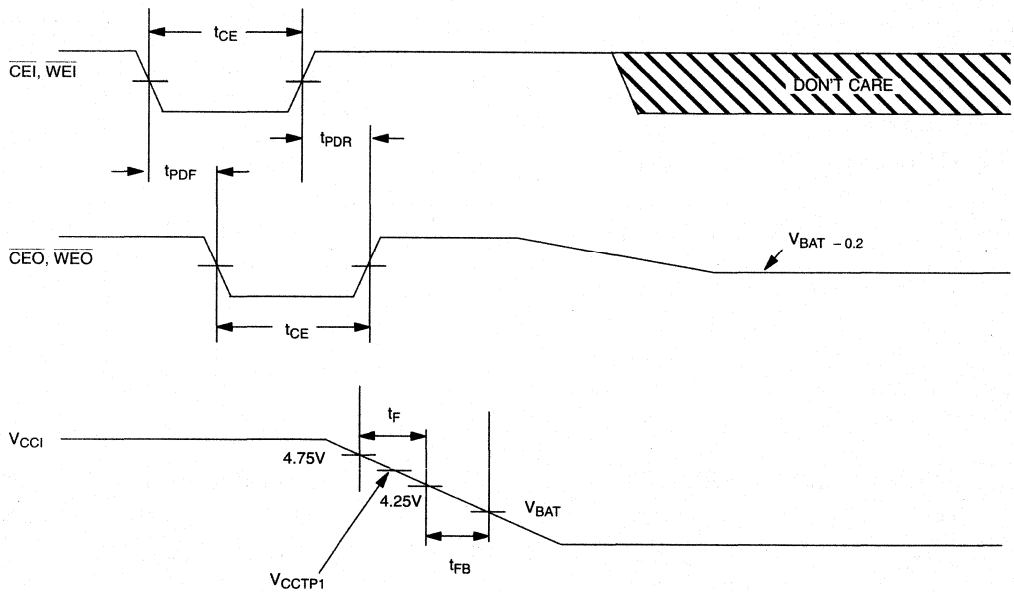
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power Up	t_{REC}	100		200	ms	12
V_{CC} Slew Rate Power Down	t_F	300			µs	
V_{CC} Slew Rate Power Up	t_R	0			µs	13
$\overline{CEI}$ Pulse Width	t_{CE}			1.5	µs	7, 8
$\overline{WEI}$ Pulse Width	t_{CE}			1.5	µs	7, 8

6

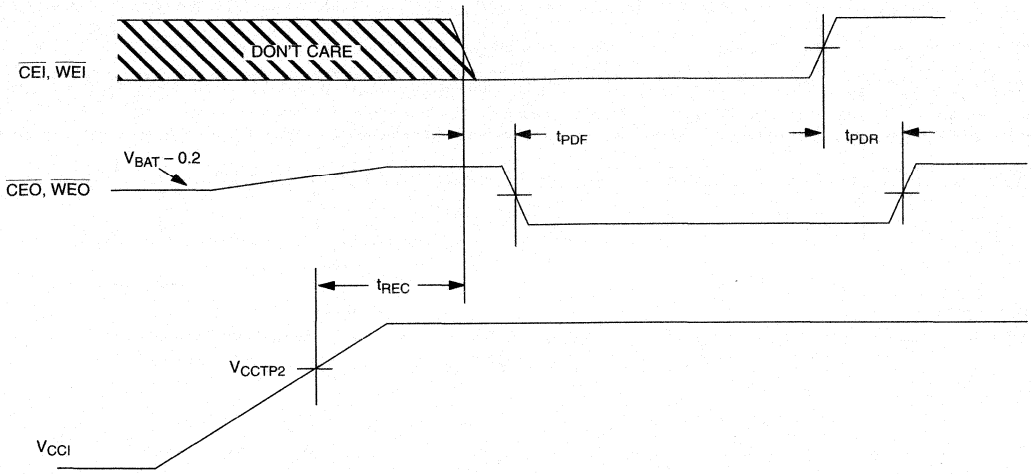
TIMING DIAGRAM: POWER UP (5 VOLT)



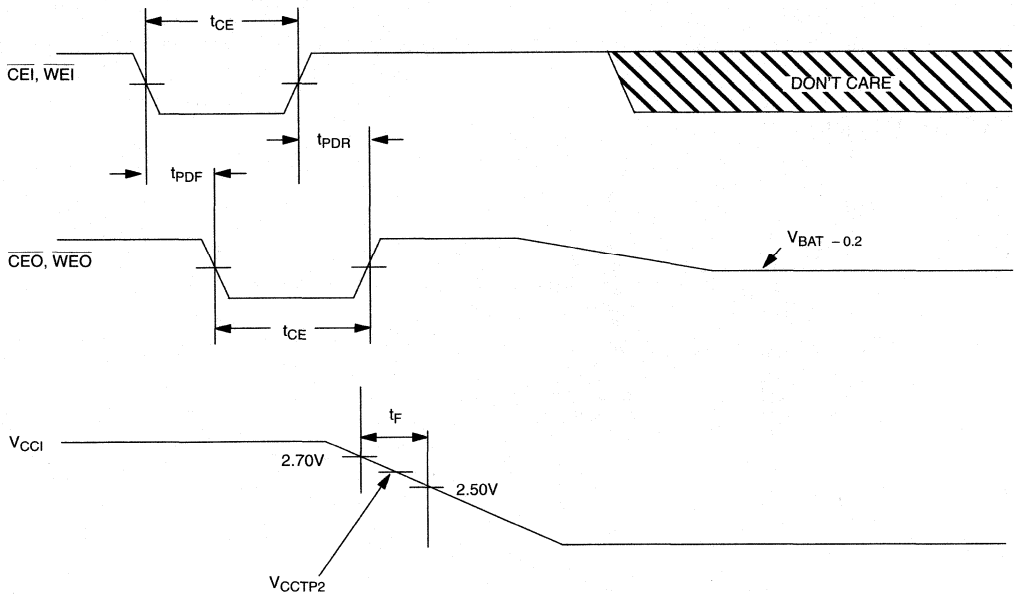
TIMING DIAGRAM: POWER DOWN (5 VOLT)



TIMING DIAGRAM: POWER UP (3 VOLT)

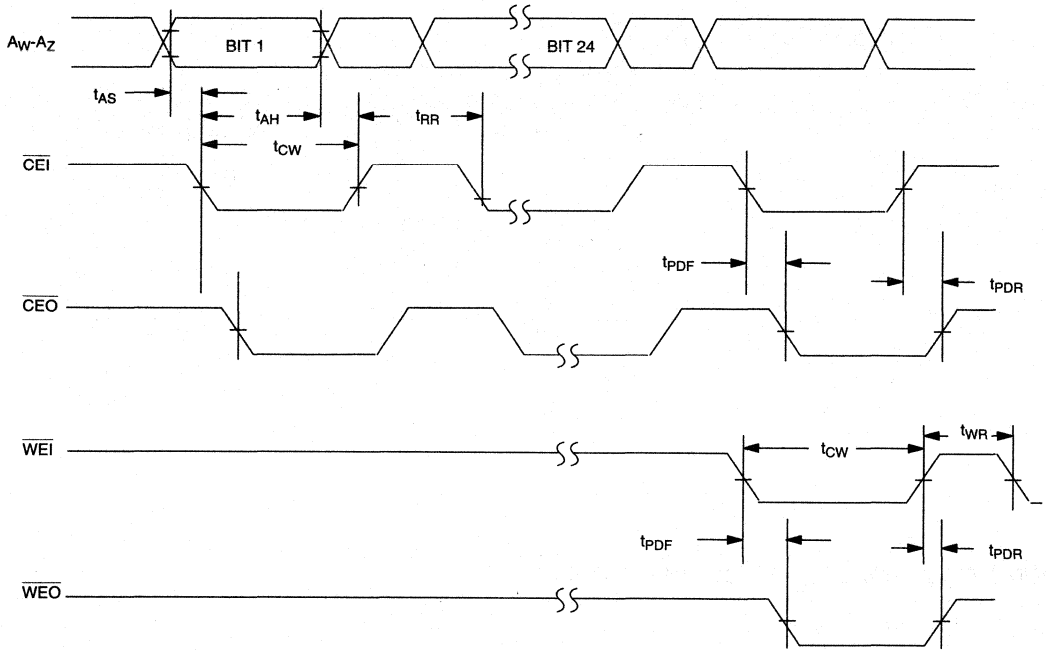


TIMING DIAGRAM: POWER DOWN (3 VOLT)

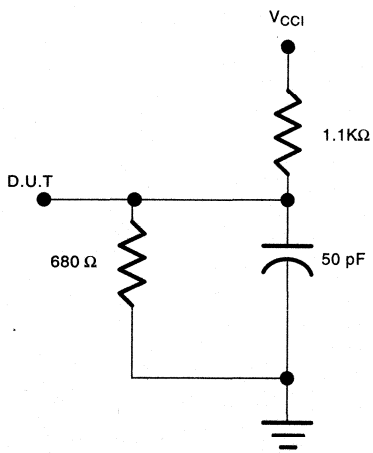


6

TIMING DIAGRAM: LOADING PARTITION REGISTER



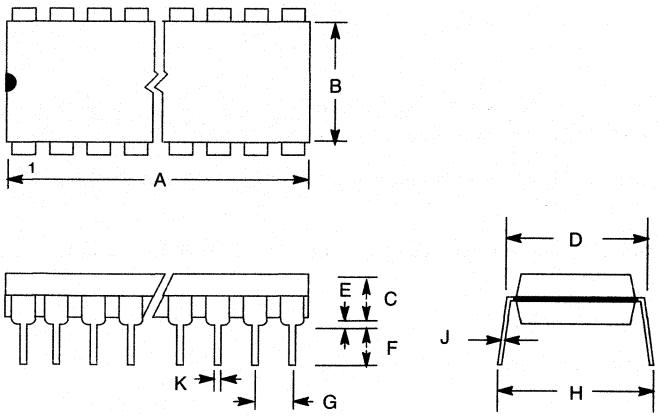
OUTPUT LOAD Figure 1



NOTES:

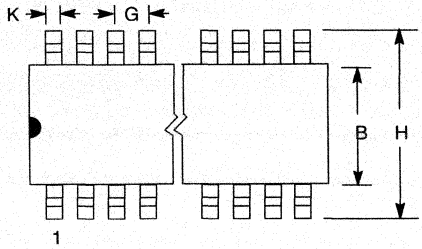
1. All voltages are reference to ground
2. Only one battery input is required.
3. Measured with outputs open circuited.
4. I_{CC01} is the maximum average load which the DS1710 can supply to the memories.
5. Z_{CE} is an average input-to-output impedance as the input is swept from ground to V_{CCI} and less than 4 mA is forced through Z_{CE}.
6. I_{CC02} is the maximum average load current which the DS1710 can supply to the memories in the battery backup mode.
7. t_{CE} max must be met to insure data integrity on power loss.
8. Chip Enable Output $\overline{CEO}$ can only sustain leakage current in the battery mode.
9. Applies only when loading partition switch.
10. Measured with a load as shown in Figure 1.
11. Measured with $\overline{DIS}$ at a logic high level.
12. $\overline{CEO}$ and $\overline{WEO}$ will be held high for a time equal to t_{REC} after V_{CCI} crosses V_{CCTP2}.
13. t_R is the slew rate of V_{CCI} from 4.25V to 4.75V or 2.50 to +2.70 volts.
14. $\overline{CEI}$, $\overline{WEI}$, A_W - A_Z run at minimum timing set and at voltage levels of 0V to 3V.
15. All inputs within 0.3V of ground or V_{CCI} and $\overline{CEI}$ within 0.3V of V_{CCI}.
16. The power fail output signal ($\overline{PFO}$) is driven active (V_{OL} = 0.4V) when the V_{CC} trip point occurs. While active, the $\overline{PFO}$ pin can sink 4 mA and will maintain a maximum output voltage of 0.4 volts. When inactive, the voltage output of $\overline{PFO}$ is 2.4 volts minimum and will source a current of 1 mA.

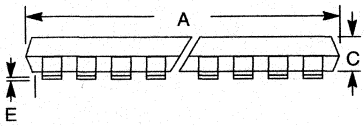
DS1710 16–PIN DIP (300 MIL)

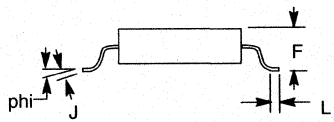


PKG	16-PIN	
DIM	MIN	MAX
A IN. MM	0.740 18.80	0.780 19.81
B IN. MM	0.240 6.10	0.260 6.60
C IN. MM	0.120 3.05	0.140 3.56
D IN. MM	0.300 7.62	0.325 8.26
E IN. MM	0.015 0.38	0.040 1.02
F IN. MM	0.120 3.04	0.140 3.56
G IN. MM	0.090 2.29	0.110 2.79
H IN MM	0.320 8.13	0.370 9.40
J IN MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53

DS1710 16–PIN SOIC (300 MIL)

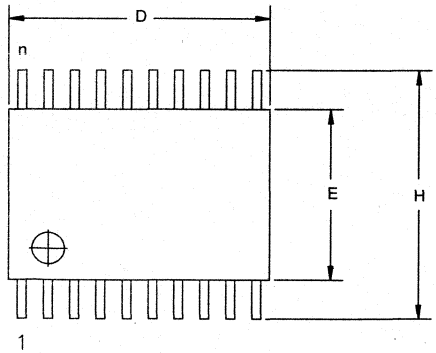


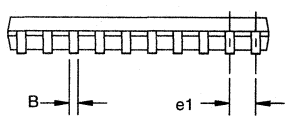


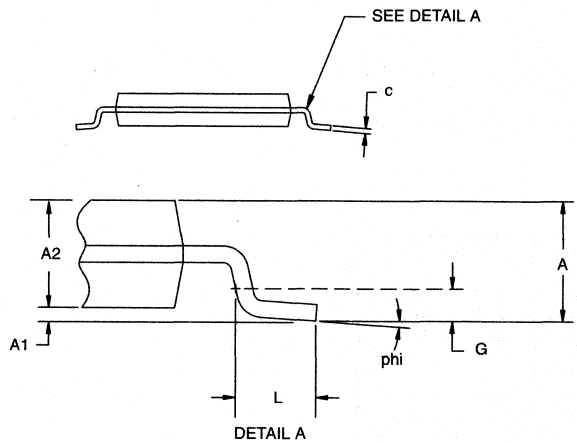


PKG	16-PIN	
DIM	MIN	MAX
A IN. MM	0.402 10.21	0.412 10.46
B IN. MM	0.290 7.37	0.300 7.65
C IN. MM	0.089 2.26	0.095 2.41
E IN. MM	0.004 0.102	0.012 0.30
F IN. MM	0.094 2.38	0.105 2.68
G IN. MM	.050 BSC 1.27 BSC	
H IN MM	0.398 10.11	0.416 10.57
J IN MM	0.009 0.229	0.013 0.33
K IN. MM	0.013 0.33	0.019 0.48
L IN MM	.016 .40	.040 1.02
PHI	0°	8°

DS1710 20-PIN TSSOP







DIM	MIN	MAX
A MM	–	1.10
A1 MM	0.05	–
A2 MM	0.75	1.05
C MM	0.09	0.18
L MM	0.50	0.70
e1 MM	0.65 BSC	
B MM	0.18	0.30
D MM	6.40	6.90
E MM	4.40 NOM	
G MM	0.25 REF	
H MM	6.25	6.55
phi	0°	8°

SILICON TIMED CIRCUITS

7

SILICON TIMED CIRCUITS

DELAY LINES (HYBRID REPLACEMENTS)

Multiple Tap Delays

# TAPS	PART #	PACKAGES	FEATURES
5	DS1000	DIP, SO	4 to 500 ns delays Pin–compatible with standard hybrids
	DS1000–IND	DIP, SO	4 to 500 ns delays Industrial temperature range
	DS1004	DIP, SO	2 to 5 ns tap–to–tap increments Temperature and voltage compensation
	DS1005	DIP, SO	12 to 250 ns delays Temperature and voltage compensation
10	DS1010	DIP, SO	5 to 500 ns delays Pin–compatible with standard hybrids

Multiple Independent Delays

# DELAYS	PART #	PACKAGES	FEATURES
3	DS1013	DIP, SO	10 to 200 ns delays Pin–compatible with standard hybrids
	DS1033	DIP, SO, TSSOP	8 to 30 ns delays 3V operation
	DS1035	DIP, SO, TSSOP	6 to 30 ns delays High speed, low power
4	DS1044	DIP, SO	5 to 25 ns delays Pin–compatible with standard hybrids
7	DS1007	DIP, SO	3 to 40 ns

DELAY LINES (SYSTEM ENHANCEMENT)

# DELAYS	PART #	PACKAGES	FEATURES
1	DS1003	DIP	4–tap delay for RISC processors ±0.75 ns tap–to–tap tolerance
1	DS1020	DIP, SO	8–bit programmable 0.15 to 2 ns steps
1	DS1021	SO	8–bit programmable 0.25 and 0.50 ns steps
2	DS1012	DIP, SO	3 to 50 ns delays On–chip logic, can be used as frequency doubler
2	DS1045	DIP, SO	4–bit programmable 9 to 84 ns delays

SYSTEM TIMING FUNCTIONS

DESCRIPTION	PART #	PACKAGES	KEY FEATURES
Programmable one–shot	DS1040	DIP, SO	5 to 500 ns pulse width No external components

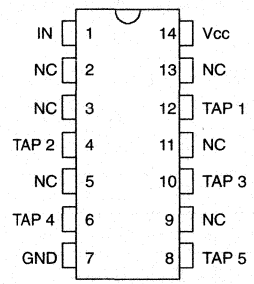
DALLAS SEMICONDUCTOR

DS1000
5-Tap Silicon Delay Line

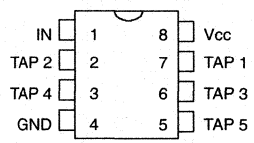
FEATURES

- All-silicon time delay
- 5 taps equally spaced
- Delays are stable and precise
- Both leading and trailing edge accuracy
- Delay tolerance ±5% or ±2 ns, whichever is greater
- Low-power CMOS
- TTL/CMOS-compatible
- Vapor phase, IR and wave solderable
- Custom delays available
- Fast turn prototypes
- Extended temperature range available (DS1000–IND)

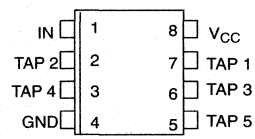
PIN ASSIGNMENT



DS1000 14-PIN DIP (300 MIL)
See Mech. Drawings Section



DS1000M 8-PIN DIP (300 MIL)
See Mech. Drawings Section



DS1000Z 8-PIN SOIC
(150 MIL)
See Mech. Drawings Section

7

PIN DESCRIPTION

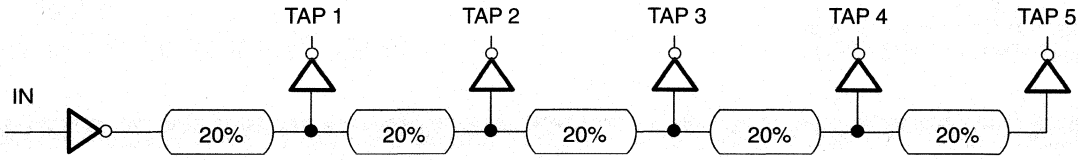
TAP 1-TAP 5	–	TAP Output Number
V_{CC}	–	+5 Volts
GND	–	Ground
NC	–	No Connection
IN	–	Input

DESCRIPTION

The DS1000 series delay lines have five equally spaced taps providing delays from 4 ns to 500 ns. These devices are offered in a standard 14-pin DIP that is pin-compatible with hybrid delay lines. Alternatively, 8-pin DIPs and surface mount packages are available to save PC board area. Low cost and superior reliability over hybrid technology is achieved by the combination of a 100% silicon delay line and industry standard DIP and SOIC packaging. In order to maintain complete pin compatibility, DIP packages are available with hybrid lead configurations. The DS1000 series delay lines provide a nominal accuracy of ±5% or ±2 ns, whichever is greater. The DS1000 5-Tap Silicon Delay Line reproduces the input logic state at the output after a fixed delay as specified by the extension of the part number after the dash. The DS1000 is designed to reproduce both leading and trailing edges with equal precision. Each tap is capable of driving up to ten 74LS loads.

Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (214) 450-5348.

LOGIC DIAGRAM Figure 1



DS1000 PART NUMBER DELAY TABLE (all values in ns) Table 1

PART # DS1000–	TAP 1			TAP 2			TAP 3			TAP 4			TAP 5		
	Nom	TOLERANCE		Nom	TOLERANCE		Nom	TOLERANCE		Nom	TOLERANCE		Nom	TOLERANCE	
		Init	Temp		Init	Temp		Init	Temp		Init	Temp		Init	Temp
–20	4	2	1	8	2	1	12	2	1	16	2	1	20	2	1
–25	5	2	1	10	2	1	15	2	1	20	2	1	25	2	1
–30	6	2	1	12	2	1	18	2	1	24	2	1	30	2	1
–35	7	2	1	14	2	1	21	2	1	28	2	1	35	2	1.1
–40	8	2	1	16	2	1	24	2	1	32	2	1	40	2	1.2
–45	9	2	1	18	2	1	27	2	1	36	2	1.1	45	2.3	1.4
–50	10	2	1	20	2	1	30	2	1	40	2	1.2	50	2.5	1.5
–60	12	2	1	24	2	1	36	2	1.1	48	2.4	1.5	60	3	1.8
–75	15	2	1	30	2	1	45	2.3	1.4	60	3	1.8	75	3.8	2.3
–100	20	2	1	40	2	1.2	60	3	1.8	80	4	2.4	100	5	3
–125	25	2	1	50	2.5	1.5	75	3.8	2.3	100	5	3	125	6.3	3.8
–150	30	2	1	60	3	1.8	90	4.5	2.7	120	6	3.6	150	7.5	4.5
–175	35	2	1.1	70	3.5	2.1	105	5.3	3.2	140	7	4.2	175	8.8	5.3
–200	40	2	1.2	80	4	2.4	120	6	3.6	160	8	4.8	200	10	6
–250	50	2.5	1.5	100	5	3	150	7.5	4.5	200	10	6	250	12.5	7.5
–500	100	5	3	200	10	6	300	15	9	400	20	12	500	25	15

NOTES:

1. Initial tolerances are ± with respect to the nominal value at 25°C and 5V.
2. Temperature tolerance is ± with respect to the initial delay value over a range of 0°C to 70°C.
3. The delay will also vary with supply voltage, typically by less than 4% over the range 4.75 to 5.25V.
4. All tap delays tend to vary unidirectionally with temperature or voltage changes. For example, if TAP 1 slows down, all other taps also slow down; TAP3 can never be faster than TAP2.
5. Intermediate delay values and packaging variations are available on a custom basis. For further information, call (214) 450–5348.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5.0V ± 5%)

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	6
High Level Input Voltage	V_{IH}		2.2		V_{CC} + 0.5	V	6
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	6
Input Leakage Current	I_I	$0.0V \le V_I \le V_{CC}$	-1.0		1.0	uA	
Active Current	I_{CC}	V_{CC}= Max; Period= Min.		35	75	mA	7, 9
High Level Output Current	I_{OH}	V_{CC}=Min. V_{OH}=4			-1	mA	
Low Level Output Current	I_{OL}	V_{CC}=Min. V_{OL}=0.5	12			mA	

AC ELECTRICAL CHARACTERISTICS

(T_A = 25°C; V_{CC} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}	40% of Tap 5 t_{PLH}			ns	8
Input to Tap Delay (leading edge)	t_{PLH}		Table 1		ns	1, 2, 3, 4, 5, 10
Input to Tap Delay (trailing edge)	t_{PHL}		Table 1		ns	1, 2, 3, 4, 5, 10
Power-up Time	t_{PU}			100	ms	
Input Period	Period	4 (t_{WI})			ns	8

CAPACITANCE

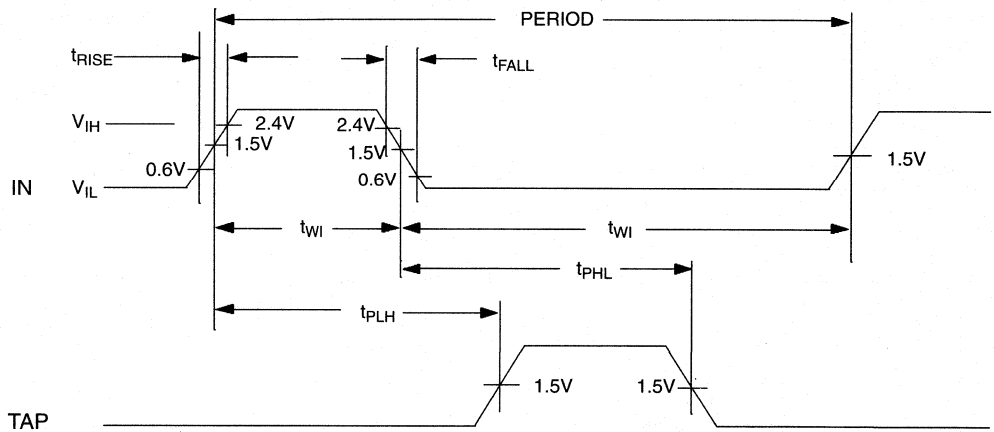
(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	

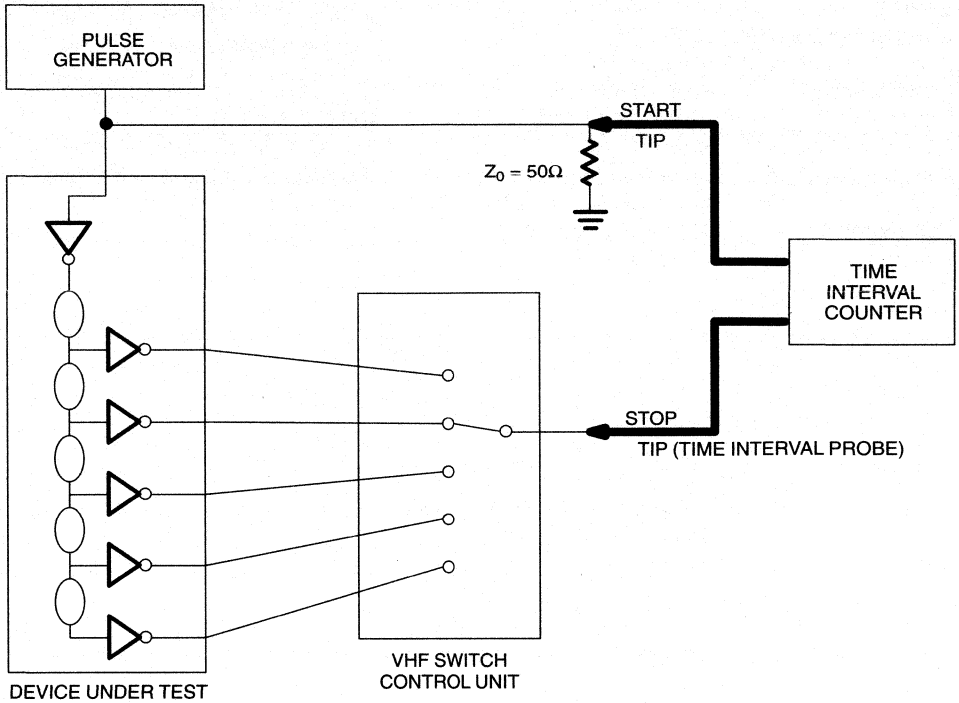
NOTES:

6. All voltages are referenced to ground.
7. Measured with outputs open.
8. Pulse width and period specifications may be exceeded; however, accuracy may be impaired depending on application (decoupling, layout, etc.). The device will remain functional with pulse widths down to 20% of Tap 5 delay, and input periods as short as $2(t_{WI})$.
9. I_{CC} is a function of frequency and TAP 5 delay. Only a -25 operating with a 40 ns period and V_{CC} = 5.25V will have an I_{CC} = 75 mA. For example a -100 will never exceed 30 mA, etc.
10. See "Test Conditions" section at the end of this data sheet.

TIMING DIAGRAM: SILICON DELAY LINE Figure 2



TEST CIRCUIT Figure 3



TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any tap output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any tap output pulse.

TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1000. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each tap. Each tap is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

INPUT :

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V
	Low = 0.0V ± 0.1V
Source Impedance:	50 ohm Max.
Rise and Fall Time:	3.0 ns Max. (measured between 0.6V and 2.4V)
Pulse Width:	500 ns (1 µs for -500)
Period:	1 µs (2 µs for -500)

OUTPUT:

Each output is loaded with the equivalent of one 74F04 input gate. Delay is measured at the 1.5V level on the rising and falling edge.

NOTE:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

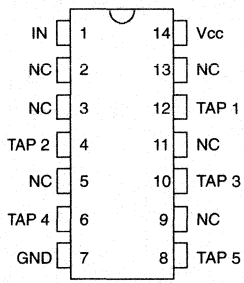
DALLAS SEMICONDUCTOR

DS1000–IND
Industrial Temperature Range 5-Tap Silicon Delay Line

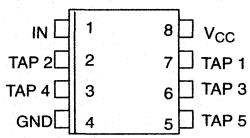
FEATURES

- All-silicon time delay
- 5 taps equally spaced
- Delays are stable and precise
- Both leading and trailing edge accuracy
- Delay tolerance ±5% or ±2 ns, whichever is greater (@25°C)
- Delays characterized over –40°C to +85°C temperature range (±2 ns or ±8%)
- Low-power CMOS
- TTL/CMOS-compatible
- Vapor phase, IR and wave solderable
- Custom delays available
- Fast turn prototypes

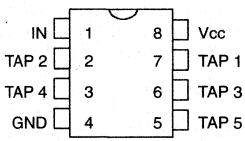
PIN ASSIGNMENT



DS1000–IND 14-PIN DIP (300 MIL)
See Mech Drawings Section



DS1000Z–IND 8-PIN SOIC
(150 MIL)
See Mech. Drawings Section



DS1000M–IND 8-PIN DIP
(300 MIL)
See Mech. Drawings Section

7

PIN DESCRIPTION

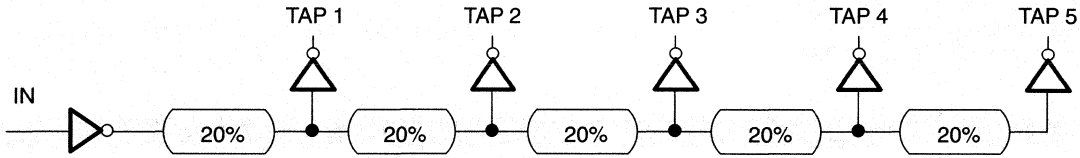
TAP 1-TAP 5	- TAP Output Number
V_{CC}	- +5 Volts
GND	- Ground
NC	- No Connection
IN	- Input

DESCRIPTION

The DS1000–IND series delay lines have five equally spaced taps providing delays from 4 ns to 500 ns. These devices are offered in standard 8– and 14-pin DIPs that are pin-compatible with hybrid delay lines. Alternatively, 8-pin SOICs are available to save PC board area. Low cost and superior reliability over hybrid technology is achieved by the combination of a 100% silicon delay line and industry standard DIP and SOIC packaging. In order to maintain complete pin compatibility, DIP packages are available with hybrid lead configurations. The DS1000–IND series delay lines provide a nominal accuracy of ±5% or ±2 ns, whichever is greater. The DS1000–IND 5-Tap Silicon Delay Line reproduces the input logic state at the output after a fixed delay as specified by the extension of the part number after the dash. The DS1000–IND is designed to reproduce both leading and trailing edges with equal precision. Each tap is capable of driving up to ten 74LS loads.

Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (214) 450-5348.

LOGIC DIAGRAM Figure 1



DS1000–IND PART NUMBER DELAY TABLE Table 1

PART # DS1000–	TAP 1			TAP 2			TAP 3			TAP 4			TAP 5		
	Nom	TOLERANCE		Nom	TOLERANCE		Nom	TOLERANCE		Nom	TOLERANCE		Nom	TOLERANCE	
		Init	T&V		Init	T&V		Init	T&V		Init	T&V		Init	T&V
–20	4	2	2	8	2	2	12	2	2	16	2	2	20	2	2
–25	5	2	2	10	2	2	15	2	2	20	2	2	25	2	2
–30	6	2	2	12	2	2	18	2	2	24	2	2	30	2	2.4
–35	7	2	2	14	2	2	21	2	2	28	2	2.2	35	2	2.8
–40	8	2	2	16	2	2	24	2	2	32	2	2.6	40	2	3.2
–45	9	2	2	18	2	2	27	2	2.2	36	2	2.9	45	2.3	3.6
–50	10	2	2	20	2	2	30	2	2.4	40	2	3.2	50	2.5	4
–60	12	2	2	24	2	2	36	2	2.9	48	2.4	3.9	60	3	4.8
–75	15	2	2	30	2	2.4	45	2.3	3.6	60	3	4.8	75	3.8	6
–100	20	2	2	40	2	3.2	60	3	4.8	80	4	6.4	100	5	8
–125	25	2	2	50	2.5	4	75	3.8	6	100	5	8	125	6.3	10
–150	30	2	2.4	60	3	4.8	90	4.5	7.2	120	6	9.6	150	7.5	12
–175	35	2	2.8	70	3.5	5.6	105	5.3	8.4	140	7	11.2	175	8.8	14
–200	40	2	3.2	80	4	6.4	120	6	9.6	160	8	12.8	200	10	16
–250	50	2.5	4	100	5	8	150	7.5	12	200	10	16	250	12.5	20
–500	100	5	8	200	10	16	300	15	24	400	20	32	500	25	40

NOTES:

1. Initial tolerances are ± with respect to the nominal value at 25°C and 5V.
2. Temperature tolerance is ± with respect to the initial delay value over a range of -40°C to 85°C, and a supply voltage range of 4.75 to 5.25V.
3. All tap delays tend to vary unidirectionally with temperature or voltage changes. For example, if TAP 1 slows down, all other taps also slow down; TAP3 can never be faster than TAP2.
4. Intermediate delay values and packaging variations are available on a custom basis. For further information, call (214) 450–5348.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–1.0V to +7.0V
Operating Temperature	–40°C to +85°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC} = 5.0V ± 5%)

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	5
High Level Input Voltage	V_{IH}		2.2		V_{CC} + 0.5	V	5
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	5
Input Leakage Current	I_I	$0.0V \le V_I \le V_{CC}$	-1.0		1.0	uA	
Active Current	I_{CC}	V_{CC}= Max; Period= Min.		35	75	mA	6, 8
High Level Output Current	I_{OH}	V_{CC}=Min. V_{OH}=4			-1	mA	
Low Level Output Current	I_{OL}	V_{CC}=Min. V_{OL}=0.5	12			mA	

AC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}	40% of Tap 5 t_{PLH}			ns	7
Input to Tap Delay (leading edge)	t_{PLH}		Table 1		ns	1, 2, 3, 4, 9
Input to Tap Delay (trailing edge)	t_{PHL}		Table 1		ns	1, 2, 3, 4, 9
Power-up Time	t_{PU}			100	ms	
Input Period	Period	4 (t_{WI})			ns	7

CAPACITANCE

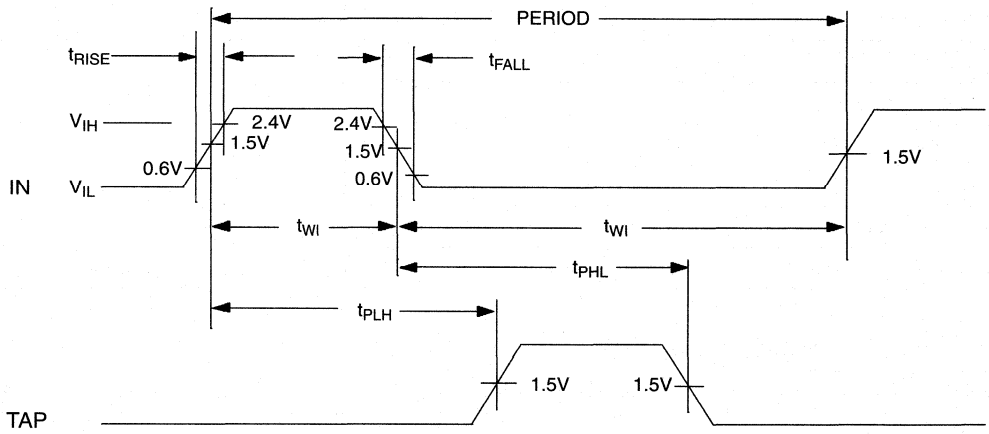
(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	

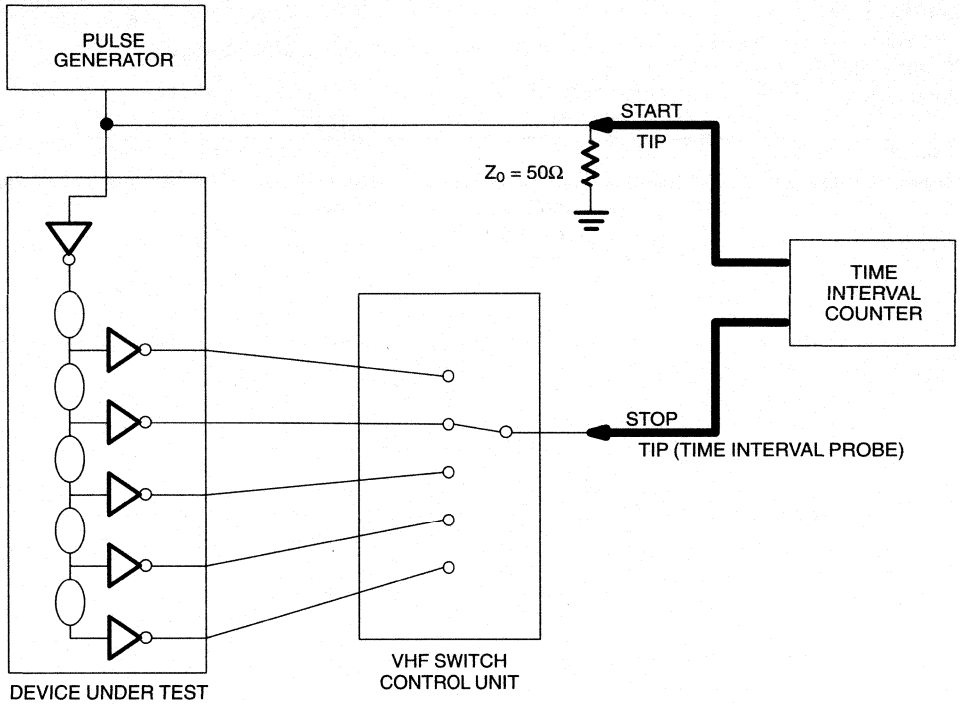
NOTES:

5. All voltages are referenced to ground.
6. Measured with outputs open.
7. Pulse width and period specifications may be exceeded; however, accuracy may be impaired depending on application (decoupling, layout, etc.). The device will remain functional with pulse widths down to 20% of Tap 5 delay, and input periods as short as $2(t_{WI})$.
8. I_{CC} is a function of frequency and TAP 5 delay. Only a -25 operating with a 40 ns period and V_{CC} = 5.25V will have an I_{CC} = 75 mA. For example a -100 will never exceed 30 mA, etc.
9. See "Test Conditions" section at the end of this data sheet.

TIMING DIAGRAM: SILICON DELAY LINE Figure 2



TEST CIRCUIT Figure 3



TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any tap output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any tap output pulse.

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TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1000–IND. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each tap. Each tap is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

INPUT :

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V Low = 0.0V ± 0.1V
Source Impedance:	50 ohm Max.
Rise and Fall Time:	3.0 ns Max. (measured between 0.6V and 2.4V)
Pulse Width:	500 ns (1 µs for -500)
Period:	1 µs (2 µs for -500)

OUTPUT:

Each output is loaded with the equivalent of one 74F04 input gate. Delay is measured at the 1.5V level on the rising and falling edge.

NOTE:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

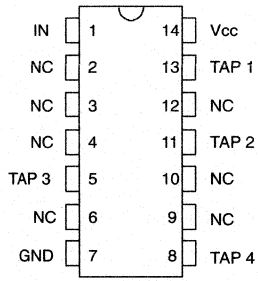
DALLAS SEMICONDUCTOR

DS1003
4-Tap Silicon Delay Line for RISC Applications

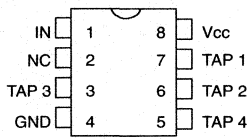
FEATURES

- All-silicon time delay
- Four delayed clock phases from input
- Input frequency independent
- Precise tap-to-tap delays
- Leading and trailing edge precision
- Preserves input symmetry
- Output rise time minimizes ringing
- Economical
- 8- and 14-pin packages available in DIP and surface mount
- TTL/CMOS-compatible
- Vapor phase, IR and wave solderable
- Custom delays and pinouts available
- Fast turn prototypes

PIN ASSIGNMENT



DS1003 14-PIN DIP
(300 MIL)
See Mech. Drawings Section



DS1003M 8-PIN DIP
(300 MIL)
See Mech. Drawings Section

PIN DESCRIPTION

TAP 1 – TAP 4	– TAP Output Number
V_{CC}	– +5 Volts
GND	– Ground
NC	– No Connection
IN	– Input

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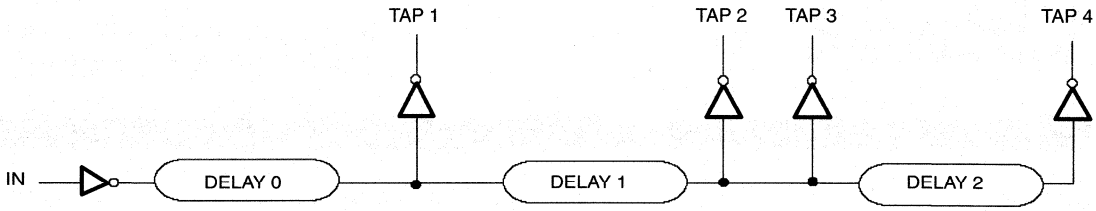
DESCRIPTION

The DS1003 Delay Line has been specifically designed to supply the four independent clock timing phases required by some RISC microprocessors and their related coprocessors. For optimum compatibility, the DS1003 accepts TTL input levels and supplies CMOS and TTL compatible output levels. The DS1003 is offered in 8- and 14-pin DIP packages. Low cost and superior reliability is achieved by the combination of a 100% silicon delay line and industry standard packaging. The DS1003 series of delay lines provides precise tap-to-tap delays while preserving input waveform symmetry.

Since the DS1003 is not based on Phase Locked Loop (PLL) technology, timing is input frequency-independent. Each tap is capable of driving a minimum of four LSTTL or CMOS loads. Tap-to-tap timing accuracy is not affected by the addition of equal capacitive loads (e.g. coprocessors).

Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (214) 450–5348.

LOGIC DIAGRAM Figure 1



PART NUMBER DELAY TABLE (t_{PLH}) Table 1

PART NO.		DS1003-16	DS1003-20	DS1003-25	DS1003-33	DS1003-40
INPUT - TAP 1	Delay 0	8 ns ± 2 ns	8 ns ± 2 ns	8 ns ± 2 ns	6 ns ± 2 ns	6 ns ± 2 ns
TAP 1 - TAP 2	Delay 1	6 ns ± .75 ns	6 ns ± .75 ns	6 ns ± .5 ns	4.5 ns ± .5 ns	4.0 ns ± .5 ns
TAP 1 - TAP 4	Delay 1+ Delay 2	16 ns ± 1 ns	14 ns ± 1 ns	12 ns ± .75 ns	9 ns ± .75 ns	8 ns ± .75 ns
TAP 2 - TAP 3 (Note 10)	——	0.2 ns ± .2 ns	0.2 ns ± .2 ns	0.2 ns ± .2 ns	0.2 ns ± .2 ns	0.2 ns ± .2 ns
TAP 3 - TAP 4	Delay 2	10 ns ± .75 ns	8 ns ± .75 ns	6 ns ± .5 ns	4.5 ns ± .5 ns	4.0 ns ± .5 ns

PERIOD AND WIDTH TABLE Table 2

PART NO.	PERIOD			t_{WI}		
	MIN	NOM	MAX	MIN	NOM	MAX
DS1003-16	29 ns	30 ns	∞	12 ns	15 ns	∞
DS1003-20	24 ns	25 ns	∞	10 ns	12.5 ns	∞
DS1003-25	19 ns	20 ns	∞	8 ns	10 ns	∞
DS1003-33	14 ns	15 ns	∞	6 ns	7.5 ns	∞
DS1003-40	12 ns	12.5 ns	∞	5 ns	6.25 ns	∞

I_{CC} TABLE Table 3

PART NO.	I_{CC}	
	TYP	MAX
DS1003-16	65 mA	75 mA
DS1003-20	75 mA	85 mA
DS1003-25	85 mA	95 mA
DS1003-33	100 mA	110 mA
DS1003-40	115 mA	125 mA

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5.0V ± 5%)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC} + 0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0.0V \le V_I \le V_{CC}$	-1.0		1.0	µA	
Active Current	I_{CC}	V_{CC} = Max; Period = Min.		Table 3	Table 3	mA	2
High Level Output Current	I_{OH}	V_{CC} = Min. V_{OH} = 4			-1	mA	
Low Level Output Current	I_{OL}	V_{CC} = Min V_{OH} = 0.5	12			mA	

AC ELECTRICAL CHARACTERISTICS

(T_A = 25°C; V_{CC} = 5.0V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}	Table 2	Table 2	Table 2	ns	6
TAP to TAP Delay (leading edge)	t_{PLH}	Table 1	Table 1	Table 1	ns	3,4,5,6,7
TAP to TAP Delay (trailing edge)	t_{PHL}		Note 9		ns	9
Output Symmetry (Input: 50%±5%)		40	50	60	%	3,5
Output Rise Time	t_{OR}		2.0	2.5	ns	8,10
Output Fall Time	t_{OF}		2.0	2.5	ns	8,10
Power-up Time	t_{PU}			100	ms	
Period	Period	Table 2	Table 2	Table 2	ns	

CAPACITANCE

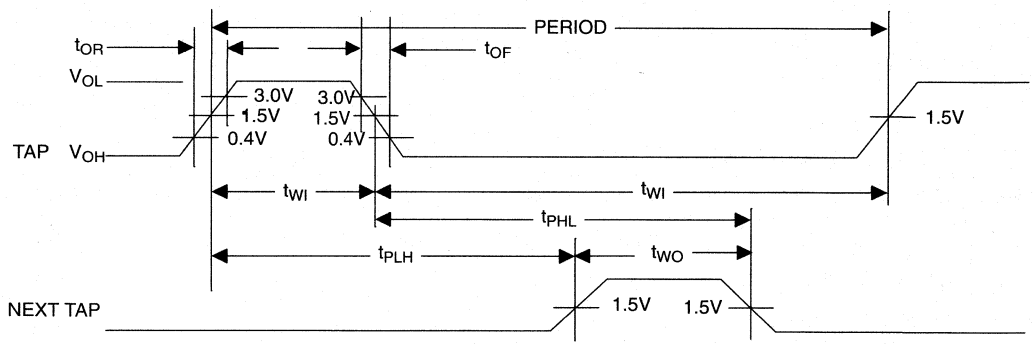
(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	10

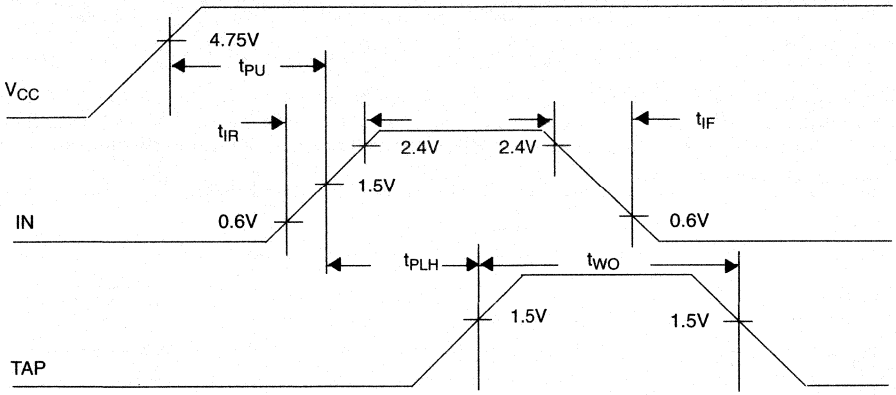
NOTES:

1. All voltages are reference to ground.
2. Measured with outputs open, minimum period.
3. V_{CC} = 5V @ 25°C.
4. Temperature variations from 25°C to 0°C or 70°C may produce an additional tap-to-tap delay shift of ±0.5 ns. Voltage variations from 5.0V to 4.75V or 5.25V produce a worst case tap-to-tap delay shift of 5%.
5. All tap-to-tap delays vary unidirectionally over temperature or voltage range. For example, if the TAP 1 - TAP 2 delay, t_{PLH}, slows down, the TAP2 - TAP 4 delay, t_{PLH}, will also slow down. Since t_{PHL} tracks t_{PLH}, symmetry is preserved.
6. See "Test Conditions" section at the end of this data sheet.
7. Since all four taps have identical output stages, tap-to-tap delays and waveform symmetry will exhibit minimal variation when capacitive loading is increased identically on all taps at the same time (e.g., the addition of one or more RISC coprocessors).
8. V_{CC} = Min; C_L = 30 pF
9. Trailing edge delays, t_{PHL}, are adjusted to maintain waveform symmetry.
10. Guaranteed by design. Periodically tested.

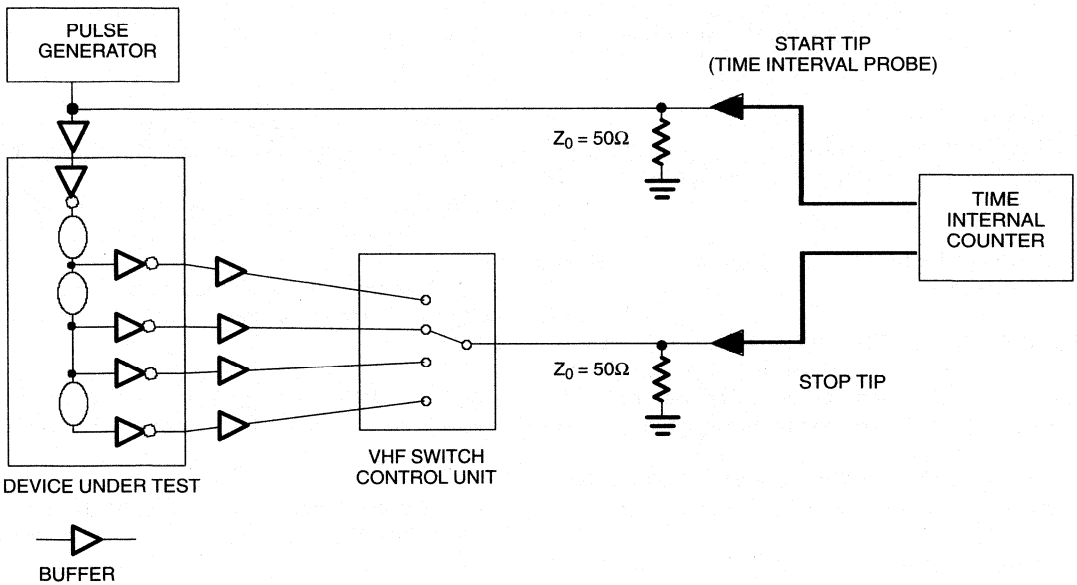
TIMING DIAGRAM: SILICON DELAY LINE Figure 2



POWER-UP TIMING DIAGRAM Figure 3



TEST CIRCUIT Figure 4



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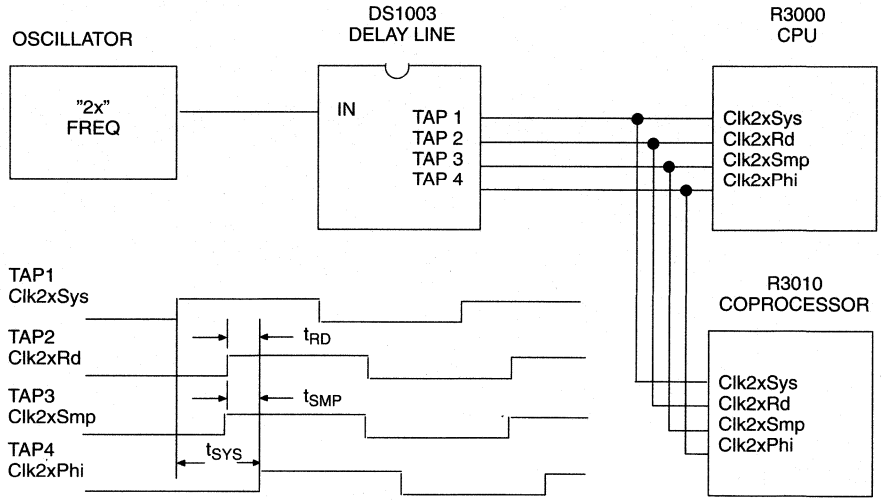
TYPICAL APPLICATION Figure 5



NOTE: TAP 2 can be used for Clk2xSmp with TAP 3 as Clk2xRd.

TERMINOLOGY

Period: The time elapsed between the leading edge of the first trigger pulse and the leading edge of the following pulse.

Symmetry: That percent of the Period when the input or output is above 1.5V.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{IR} (Input Rise Time): The elapsed time between 0.6V and 2.4V on the leading edge of the input pulse.

t_{IF} (Input Fall Time): The elapsed time between 2.4V and 0.6V on the trailing edge of the input pulse.

t_{OR} (Output Rise Rime): The elapsed time between 0.4V and 3.0V on the leading edge of the output pulse.

t_{OF} (Output Fall Time): The elapsed time between 3.0V and 0.4V of the trailing edge output pulse.

t_{PLH} (Time Delay, Rising): Input-to-tap or tap-to-tap delay measured between the 1.5V points on the leading edges.

t_{PHL} (Time Delay, Falling): Input-to-tap or tap-to-tap delay measured between the 1.5V points on the trailing edges.

t_{PU} (Power-up Time): After V_{CC} is valid, the time required before timing specifications are within tolerance.

TEST SETUP DESCRIPTION

Figure 4 illustrates the hardware configuration used for measuring the timing parameters on the DS1003. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution connected between the input and each tap). Each tap is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

Input:

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V Low = 0.0V ± 0.1
Source Impedance:	50 ohm max.
Rise and Fall Time:	3.0 ns max. (measured between 0.6V and 2.4)
Pulse Width:	500 ns
Period:	1000 ns

Output:

Each output is loaded with the equivalent of one 74F04 input. Delays are measured at the 1.5V level.

Note:

Above conditions are for test only. The adjusted test limits and guardbands used assure operation to data sheet timing specifications.

7

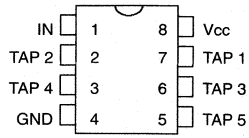
DALLAS SEMICONDUCTOR

DS1004
5-Tap High–Speed Silicon Delay Line

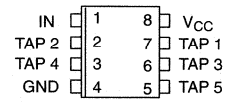
FEATURES

- All–silicon timing circuit
- Five equally delayed clock phases per input
- Precise tap–to–tap delay tolerances of ±0.5, ±0.75, or ±1 ns
- Input–to–tap 1 delay of 5 ns
- Delay tolerances of ±1.5 ns over temperature and voltage
- Leading and trailing edge precision preserves the input symmetry
- CMOS design with TTL compatibility
- Standard 8–pin DIP and 150 mil 8–pin SOIC
- Vapor phasing, IR and wave solderable
- Available in Tape and Reel

PIN ASSIGNMENT



DS1004M 8-PIN DIP
(300 MIL)
See Mech. Drawings
Section



DS1004Z 8-PIN SOIC
(150 MIL)
See Mech. Drawings
Section

PIN DESCRIPTION

TAP 1–5	–	TAP Output Number
V_{CC}	–	+5 Volt Supply
GND	–	Ground
IN	–	Input

DESCRIPTION

The DS1004 is a 5–tap all silicon delay line which can provide 2, 3, 4, or 5 ns tap–to–tap delays within a standard part family. The device is Dallas Semiconductor's fastest 5–tap delay line. It is available in a standard 8–pin DIP and 150 mil 8–pin mini–SOIC. The device features precise leading and trailing edge accuracies and has the inherent reliability of an all–silicon delay line solution.

The DS1004 is specified for tap–to–tap tolerances as shown in Table 1. Each device has a minimum input–to–tap 1 delay of 5 ns. Subsequent taps (taps 2 through 5) are precisely delayed by 2, 3, 4, or 5 ns. See Table 1 for details. Tolerance over temperature and voltage is ±1.5 ns. Nominal tap–to–tap tolerances range from ±0.5 ns to ±1.0 ns. Each output is capable of driving up to 10 LS loads.

For customers needing non–standard delay values, the Late Package Program (LPP) is available. Customers may contact Dallas Semiconductor at 214–450–5348 for further details.

PART NUMBER TOLERANCE TABLE Table 1

PART NUMBER	INPUT–TO–TAP		TAP–TO–TAP		
	TOLERANCE NOMINAL	VARIATION OVER TEMP & VOLTAGE	INCREMENT	TOLERANCE NOMINAL	VARIATION OVER TEMP & VOLTAGE
DS1004M–2	5 ± 1.5 ns	±1.5 ns	2 ns	±0.5 ns	±0.75 ns
DS1004M–3	5 ± 1.5 ns	±1.5 ns	3 ns	±0.75 ns	±0.75 ns
DS1004M–4	5 ± 1.5 ns	±1.5 ns	4 ns	±1.0 ns	±0.75 ns
DS1004M–5	5 ± 1.5 ns	±1.5 ns	5 ns	±1.0 ns	±0.75 ns
DS1004Z–2	5 ± 1.5 ns	±1.5 ns	2 ns	±0.5 ns	±0.75 ns
DS1004Z–3	5 ± 1.5 ns	±1.5 ns	3 ns	±0.75 ns	±0.75 ns
DS1004Z–4	5 ± 1.5 ns	±1.5 ns	4 ns	±1.0 ns	±0.75 ns
DS1004Z–5	5 ± 1.5 ns	±1.5 ns	5 ns	±1.0 ns	±0.75 ns

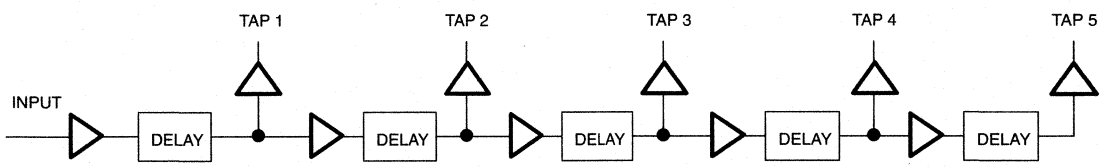
NOTES:

1. Nominal conditions are +25°C and V_{CC}=+5.0 volts.
2. Temperature and voltage variations cover the range from V_{CC}=5.0 volts ± 5% and temperature range from 0°C to +70°C.
3. Delay accuracy for both leading and trailing edges.

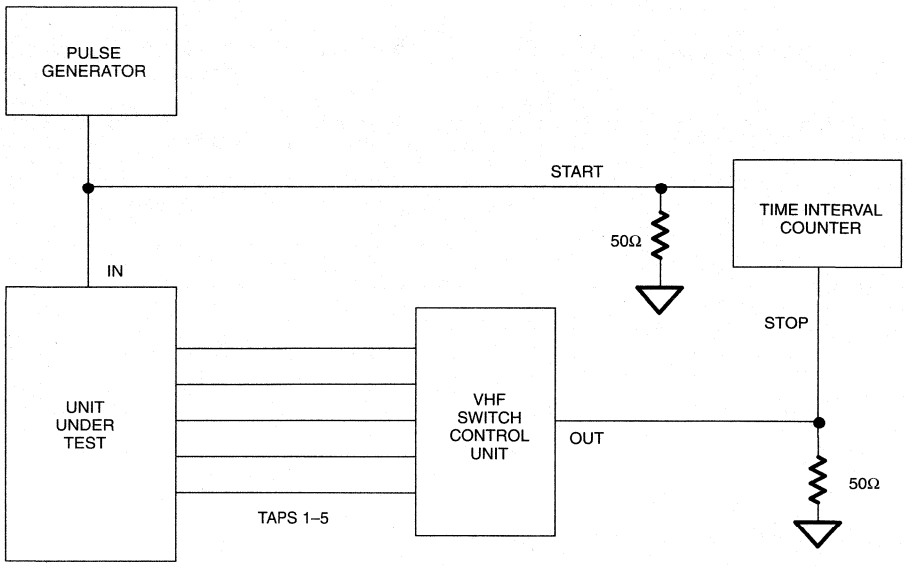
PART NUMBER DELAY TABLE Table 2

PART NUMBER	NOMINAL VALUES (FOR REFERENCE ONLY)				
	INPUT–TO–TAP1	INPUT–TO–TAP2	INPUT–TO–TAP3	INPUT–TO–TAP 4	INPUT–TO–TAP 5
DS1004M–2	5 ns	7 ns	9 ns	11 ns	13 ns
DS1004M–3	5 ns	8 ns	11 ns	14 ns	17 ns
DS1004M–4	5 ns	9 ns	13 ns	17 ns	21 ns
DS1004M–5	5 ns	10 ns	15 ns	20 ns	25 ns
DS1004Z–2	5 ns	7 ns	9 ns	11 ns	13 ns
DS1004Z–3	5 ns	8 ns	11 ns	14 ns	17 ns
DS1004Z–4	5 ns	9 ns	13 ns	17 ns	21 ns
DS1004Z–5	5 ns	10 ns	15 ns	20 ns	25 ns

LOGIC DIAGRAM



DS1004 TEST CIRCUIT Figure 1



TEST SETUP DESCRIPTION

Figure 1 illustrates the hardware configuration used for measuring the timing parameters of the DS1004. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected to the output. The DS1004 output taps are selected and connected to the interval counter by a VHF switch control unit. All measurements are fully automated with each instrument controlled by the computer over an IEEE 488 bus.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5.0V ± 5%)

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
Active Current	I_{CC}	V_{CC}=5.25V PERIOD=1 µs		35	75	mA	
High Level Input Voltage	V_{IH}		2.2		V_{CC} + 0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage	I_I	$0.0V \le V_I \le V_{CC}$	-1.0		1.0	µA	
High Level Output Current	I_{OH}	V_{CC}=4.75V V_{OH} = 4V			-1.0	mA	
Low Level Output Current	I_{OL}	V_{CC}=4.75V V_{OL} = 0.5V	12			mA	

AC ELECTRICAL CHARACTERISTICS

(T_A = 25°C; V_{CC} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Period	t_{PERIOD}	4 (t_{WI})			ns	3
Input Pulse Width	t_{WI}	40% of tap 5 t_{PLH}			ns	3
Input to Tap 1 Output Delay	t_{PLH}, t_{PHL}		Table 1		ns	2
Tap–to–Tap Delays	t_{PLH}		Table 1		ns	2
Output Rise or Fall Time	t_{OR}, t_{OF}		2.0	2.5	ns	
Power-up Time	t_{PU}			100	ms	

CAPACITANCE

(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			10	pF	

NOTES:

1. All voltages are referenced to ground.
2. V_{CC}=5 volts and 25°C. Delay accuracy on both the rising and falling edges within tolerances given in Table 1.
3. Pulse width and duty cycle specifications may be exceeded, however, accuracy will be application sensitive with respect to decoupling, layout, etc.

TEST CONDITIONS

INPUT:

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V
	Low = 0.0V ± 0.1V
Source Impedance:	50 ohm max.
Rise and Fall Time:	3.0 ns max. (measured between 0.6V and 2.4V)
Pulse Width:	500 ns
Pulse Period:	1 µs
Output Load Capacitance:	15 pF

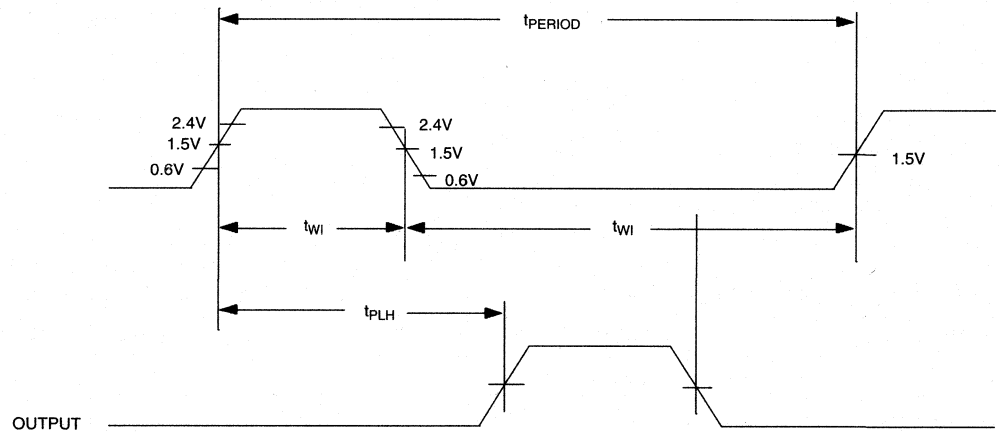
OUTPUT:

Each output is loaded with the equivalent of one 74F04 input gate. Data is measured at the 1.5V level on the rising and falling edge.

NOTE:

Above conditions are for test only and do not restrict the devices under other data sheet conditions.

TIMING DIAGRAM: DS1004 INPUT TO OUTPUTS



TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of the output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5V point on the falling edge of the input pulse and the 1.5V point on the falling edge of the output pulse.

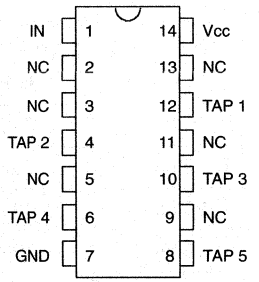
DALLAS SEMICONDUCTOR

DS1005
5-Tap Silicon Delay Line

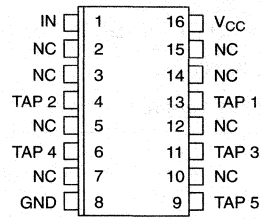
FEATURES

- All-silicon time delay
- 5 taps equally spaced
- Delay tolerance ±2 ns or ±3%, whichever is greater
- Stable and precise over temperature and voltage range
- Leading and trailing edge accuracy
- Economical
- Auto-insertable, low profile
- Standard 14-pin DIP, 8-pin DIP, or 16-pin SOIC
- Tape and reel available for surface-mount
- Low-power CMOS
- TTL/CMOS compatible
- Vapor phase, IR and wave solderability
- Custom delays available
- Quick turn prototypes
- Extended temperature range available

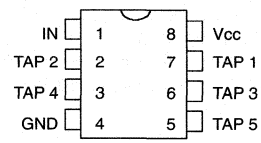
PIN ASSIGNMENT



DS1005 14-PIN DIP (300 MIL)
See Mech. Drawings Section



DS1005S 16-PIN SOIC
(300 MIL)
See Mech. Drawings Section



DS1005M 8-PIN DIP (300 MIL)
See Mech. Drawings Section

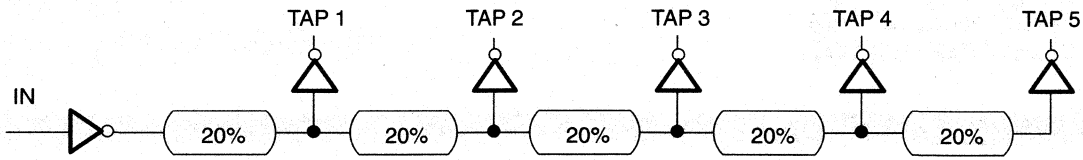
PIN DESCRIPTION

TAP 1 – TAP 5	– TAP Output Number
V_{CC}	– +5 Volts
GND	– Ground
NC	– No Connection
IN	– Input

DESCRIPTION

The DS1005 5-Tap Silicon Delay Line provides five equally spaced taps with delays ranging from 12 ns to 250 ns, with an accuracy of ±2 ns or ±3%, whichever is greater. This device is offered in a standard 14-pin DIP making it compatible with existing delay line products. Space-saving 8-pin DIPs and 16-pin SOICs are also available. Both enhanced performance and superior reliability over hybrid technology is achieved by the combination of a 100% silicon delay line and industry standard DIP and SOIC packaging. In order to maintain complete pin compatibility, DIP packages are available with hybrid lead configurations. The DS1005 reproduces the input logic level at each tap after the fixed delay specified by the dash number in Table 1. The device is designed with both leading and trailing edge accuracy. Each tap is capable of driving up to ten 74LS loads. Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (214) 450-5348.

LOGIC DIAGRAM Figure 1



PART NUMBER DELAY TABLE (t_{PHL}, t_{PLH}) Table 1

PART NO.	TAP 1	TAP 2	TAP 3	TAP 4	TAP 5
DS1005-60	12 ns	24 ns	36 ns	48 ns	60 ns
DS1005-75	15 ns	30 ns	45 ns	60 ns	75 ns
DS1005-100	20 ns	40 ns	60 ns	80 ns	100 ns
DS1005-125	25 ns	50 ns	75 ns	100 ns	125 ns
DS1005-150	30 ns	60 ns	90 ns	120 ns	150 ns
DS1005-175	35 ns	70 ns	105 ns	140 ns	175 ns
DS1005-200	40 ns	80 ns	120 ns	160 ns	200 ns
DS1005-250	50 ns	100 ns	150 ns	200 ns	250 ns

Custom delays available

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5.0V ± 5%)

PARAMETER	SYMBOL	TEST COND.	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC}+0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0.0V \le V_I \le V_{CC}$	-1.0		1.0	u A	
Active Current	I_{CC}	V_{CC} = Max; Period = Min.		40	70	mA	2
High Level Output Current	I_{OH}	V_{CC} = Min. V_{OH} = 4			-1.0	mA	
Low Level Output Current	I_{OL}	V_{CC} = Min. V_{OL} = 0.5	12			mA	

AC ELECTRICAL CHARACTERISTICS

(T_A = 25°C; V_{CC} = 5.0V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}	40% of TAP 5 t_{PLH}			ns	7
Input to Tap Delay (leading edge)	t_{PLH}		Table 1		ns	3,4,5,6
Input to Tap Delay (trailing edge)	t_{PHL}		Table 1		ns	3,4,5,6
Power-up Time	t_{PU}			100	ms	
	Period	4 (t_{WI})			ns	7

CAPACITANCE

(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	

7

NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open.
3. V_{CC} = 5V @ 25°C. Delays accurate on both rising and falling edges within ±2 ns or ±3%, whichever is greater.
4. See Test Conditions.
5. The combination of temperature variations from 25°C to 0°C or 25°C to 70°C and voltage variations from 5.0V to 4.75V or 5.0V to 5.25V may produce an additional input-to-tap delay shift of ±1.5 ns or ±4%, whichever is greater.
6. All tap delays tend to vary unidirectionally with temperature or voltage. For example, if TAP 1 slows down, all other taps will also slow down; TAP 3 can never be faster than TAP 2.
7. Pulse width and duty cycle specifications may be exceeded; however, accuracy will be application-sensitive (decoupling, layout, etc.).

TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any tap output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any tap output pulse.

TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1005. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each tap. Each tap is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

INPUT:

Ambient Temperature	25°C ± 3°C
Supply Voltage (V_{CC})	5.0V ± 0.1V
Input Pulse	High = 3.0V ± 0.1V Low = 0.0V ± 0.1V
Source Impedance	50 ohm maximum
Rise and Fall Time	3.0 ns maximum
Pulse Width	500 ns
Period	1 µs

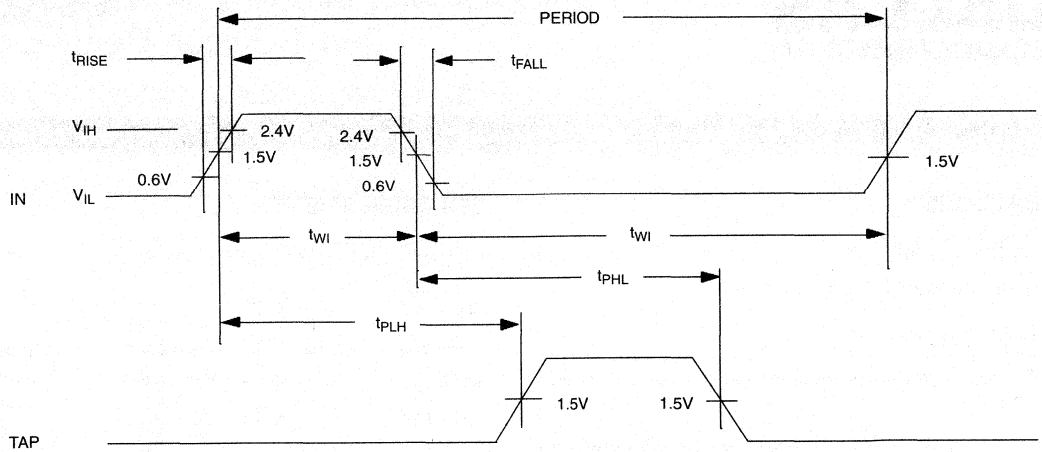
OUTPUT:

Each output is loaded with the equivalent of a 74F04 input gate. Delay is measured at the 1.5V level on the rising and falling edge.

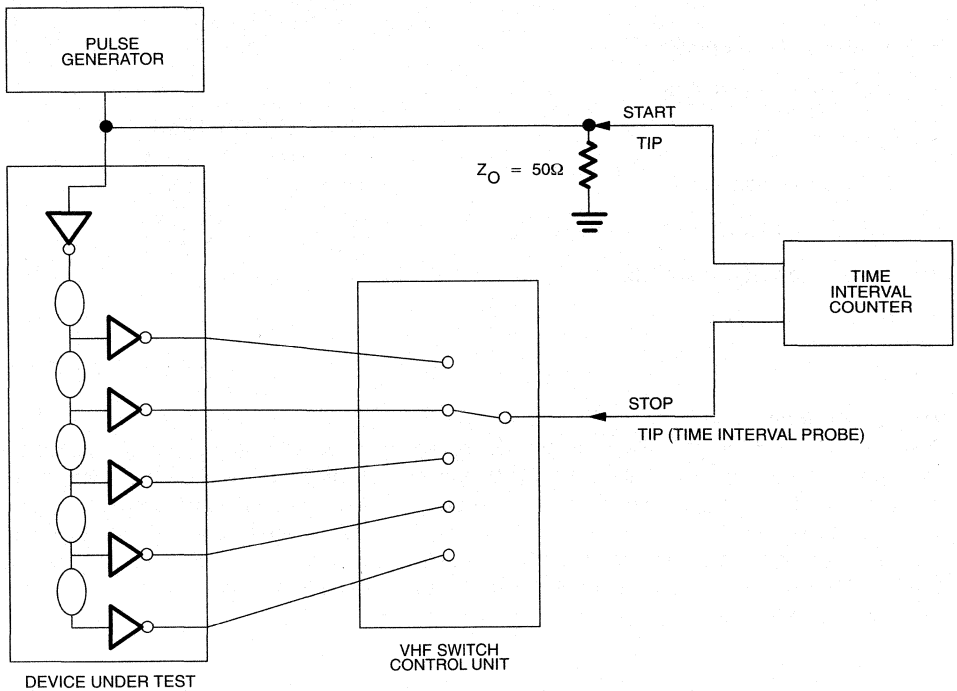
NOTE:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

TIMING DIAGRAM: SILICON DELAY LINE Figure 2



DALLAS SEMICONDUCTOR TEST CIRCUIT Figure 3



7

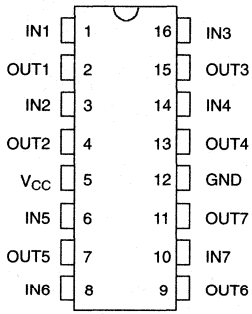
DALLAS SEMICONDUCTOR

DS1007
7-in-1 Silicon Delay Line

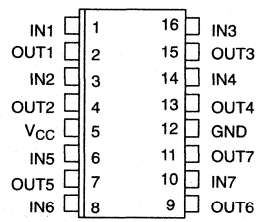
FEATURES

- All-silicon time delay
- 7 independent buffered delays
- Delay tolerance ±2 ns
- Four delays can be custom set between 3 ns and 10 ns
- Three delays can be custom set between 9 ns and 40 ns
- Delays are stable and precise
- Economical
- Auto-insertable, low profile
- Surface mount 16-pin SOIC
- Low-power CMOS
- TTL/CMOS-compatible
- Vapor phase, IR and wave solderable
- Custom specifications available
- Quick turn prototypes

PIN ASSIGNMENT



DS1007 16-PIN DIP (300 MIL)
See Mech. Drawings Section



DS1007S 16-PIN SOIC
(300 MIL)
See Mech. Drawings Section

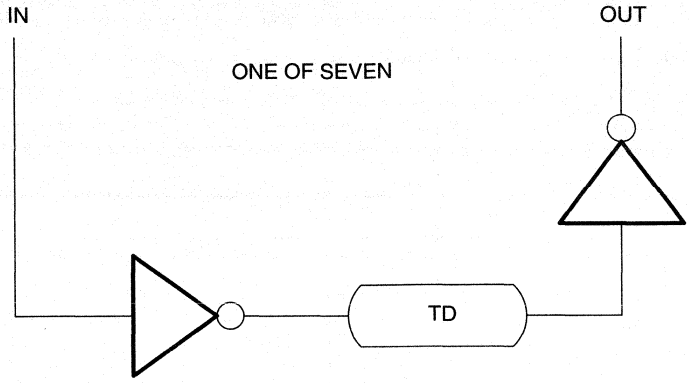
PIN DESCRIPTION

IN1 - IN7	– Inputs
Out1 - Out7	– Outputs
GND	– Ground
V_{CC}	– +5 Volts

DESCRIPTION

The DS1007 7-in-1 Silicon Delay Line provides seven independent delay times which are set by Dallas Semiconductor to the customer's specification. The delay times can be set from 3 ns to 40 ns with an accuracy of ±2 ns at room temperature. The device is offered in both a 16-pin DIP and a 16-pin SOIC. Since the DS1007 is an all-silicon solution, better economy and reliability are achieved when compared to older methods using hybrid technology. The DS1007 reproduces the input logic state at the output after the fixed delay. Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (214) 450-5348.

LOGIC DIAGRAM Figure 1



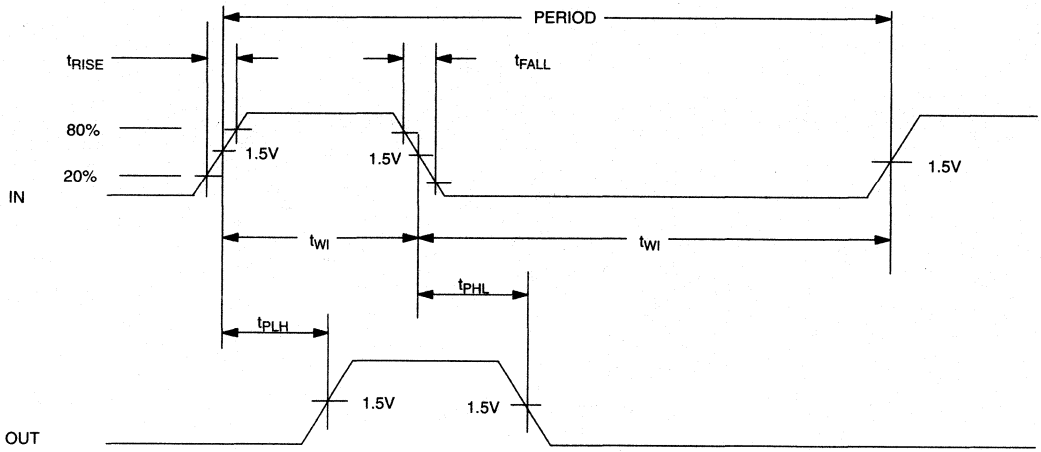
PULSE WIDTH > 100% OF DELAY

PART NUMBER DELAY TABLE (t_{PLH}) Table 1

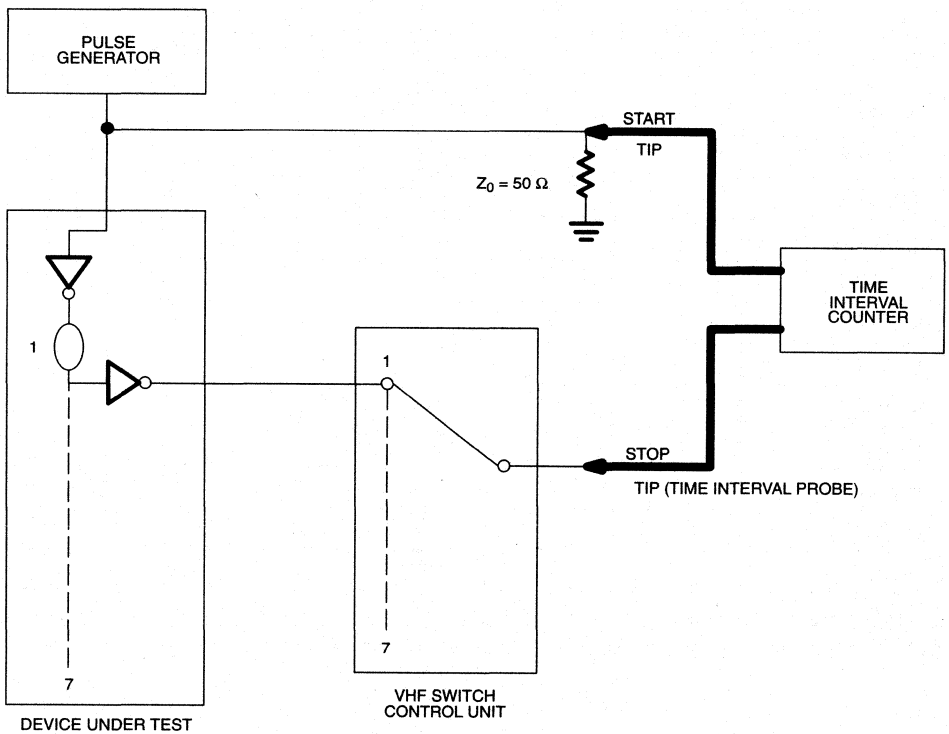
PART #	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	OUT7
DS1007-1	3ns	4ns	5ns	6ns	9ns	13ns	18ns
DS1007-2	4	6	8	10	12	14	16
DS1007-3	3	3	3	3	10	10	10
DS1007-4	4	4	4	4	12	12	12
DS1007-5	5	5	5	5	15	15	15
DS1007-6	6	6	6	6	20	20	20
DS1007-7	7	7	7	7	25	25	25
DS1007-8	8	8	8	8	30	30	30
DS1007-9	9	9	9	9	35	35	35
DS1007-10	10	10	10	10	40	40	40
DS1007-11	3	4	6	8	10	12	14
DS1007-12	3	4	6	8	10	15	20
DS1007-13	3	4	6	8	12	15	20
DS1007-14	7	7	7	7	9	9	9

Custom delays available. Out 1 through Out 4 can be custom set from 3 to 10 ns. (Leading edge only accuracy.) Out 5 through Out 7 can be custom set from 9 to 40 ns. (Both leading and trailing edge accuracy.)

TIMING DIAGRAM: SILICON DELAY LINE Figure 2



TEST CIRCUIT Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5.0V ± 5%)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC}+0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0.0V \le V_I \le V_{CC}$	-1.0		1.0	uA	
Active Current	I_{CC}	V_{CC}= Max; Period= Min.		40.0	70.0	mA	2
High Level Output Current	I_{OH}	V_{CC}= Min. V_{OH}= 2.4V			-1.0	mA	
Low Level Output Current	I_{OL}	V_{CC}= Min. V_{OL}= 0.5V	12.0			mA	

AC ELECTRICAL CHARACTERISTICS

(T_A= 25°C; V_{CC} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}	100% of t_{PLH}			ns	
Input to Output (leading edge)	t_{PLH}		Table 1		ns	3, 4, 5
Power-up Time	t_{PU}			100	ms	7
	Period	3 (t_{WI})			ns	6

CAPACITANCE

(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	

NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open.
3. V_{CC} = 5V @25°C. Delays accurate on rising edges within ±2 ns.
4. See Test Conditions below.
5. All output delays in the same speed output tend to vary unidirectionally with temperature or voltage range (i.e., if OUT 2 slows down, all other outputs also slow down).
6. Period specifications may be exceeded; however, accuracy will be application-sensitive (decoupling, layout, etc.).
7. t_{PU} = 0 ms for OUT 1 through OUT 4.

TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge, and the 1.5V point on the trailing edge or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of the corresponding output pulse.

TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1007. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each output. Each output is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

INPUT:

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V
	Low = 0.0V ± 0.1V
Source Impedance:	50 ohm Max.
Rise and Fall Time:	3.0 ns Max.
Pulse Width:	500 ns
Period:	1 µs

OUTPUT:

Each output is loaded with the equivalent of one 74F04 input gate. Delay is measured at the 1.5V level on the rising edge.

NOTE:

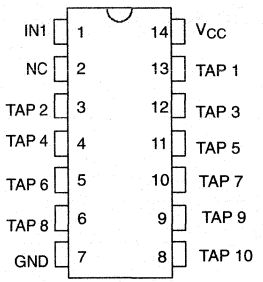
Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

DALLAS SEMICONDUCTOR

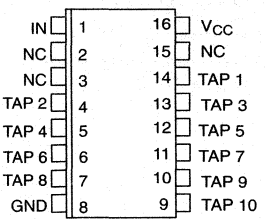
DS1010
10-Tap Silicon Delay Line

FEATURES
- All-silicon time delay
- 10 taps equally spaced
- Delays are stable and precise
- Leading and trailing edge accuracy
- Delay tolerance ±5% or ±2 ns, whichever is greater
- Economical
- Auto-insertable, low profile
- Standard 14-pin DIP or 16-pin SOIC
- Low-power CMOS
- TTL/CMOS-compatible
- Vapor phase, IR and wave solderable
- Custom delays available
- Fast turn prototypes

PIN ASSIGNMENT



DS1010 14-PIN DIP
(300 MIL)
See Mech. Drawings
Section



DS1010S 16-PIN SOIC
(300 MIL)
See Mech. Drawings
Section

PIN DESCRIPTION

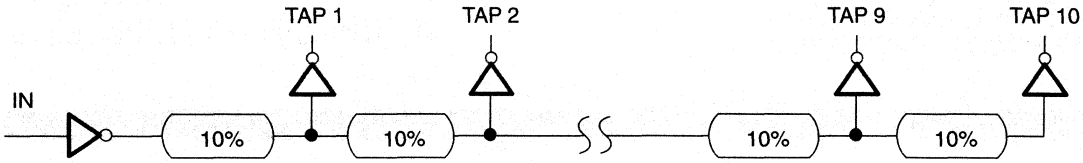
TAP 1-TAP 10	–	TAP Output Number
V_{CC}	–	5 Volts
GND	–	Ground
NC	–	No Connection
IN	–	Input

7

DESCRIPTION

The DS1010 series delay line has ten equally spaced taps providing delays from 5 ns to 500 ns. The devices are offered in a standard 14-pin DIP which is pin-compatible with hybrid delay lines. Alternatively, a 16-pin SOIC is available for surface mount technology which reduces PC board area. Since the DS1010 is an all-silicon solution, better economy is achieved when compared to older methods using hybrid techniques. The DS1010 series delay lines provide a nominal accuracy of ±5% or ±2 ns, whichever is greater. The DS1010 reproduces the input logic state at the TAP 10 output after a fixed delay as specified by the dash number extension of the part number. The DS1010 is designed to produce both leading and trailing edge with equal precision. Each tap is capable of driving up to ten 74LS type loads. Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (214) 450-5348.

LOGIC DIAGRAM Figure 1



PART NUMBER DELAY TABLE (t_{PHL}, t_{PLH}) Table 1

CATALOG P/N	TOTAL DELAY	DELAY/TAP (ns)
DS1010-50	50	5
DS1010-60	60	6
DS1010-75	75	7.5
DS1010-80	80	8
DS1010-100	100	10
DS1010-125	125	12.5
DS1010-150	150	15
DS1010-175	175	17.5
DS1010-200	200	20
DS1010-250	250	25
DS1010-300	300	30
DS1010-350	350	35
DS1010-400	400	40
DS1010-450	450	45
DS1010-500	500	50

Custom delays available.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5.0V ± 5%)

PARAMETER	SYMBOL	TEST COND.	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC}+0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0.0V \le V_I \le V_{CC}$	-1.0		1.0	µA	
Active Current	I_{CC}	V_{CC}=Max: Period=Min.		40	150	mA	2
High Level Output Current	I_{OH}	V_{CC}=Min. V_{OH}=4			-1.0	mA	
Low Level Output Current	I_{OL}	V_{CC}=Min. V_{OL}=0.5	12			mA	

AC ELECTRICAL CHARACTERISTICS

(T_A = 25°C; V_{CC} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}	40% of TAP 10 t_{PLH}			ns	8
Input to Tap Delay (leading edge)	t_{PLH}		Table 1		ns	3,4,5,6,7,9
Input to Tap Delay (trailing edge)	t_{PHL}		Table 1		ns	3,4,5,6,7,9
Power-up Time	t_{PU}			100	ms	
	Period	4(t_{WI})			ns	8

CAPACITANCE

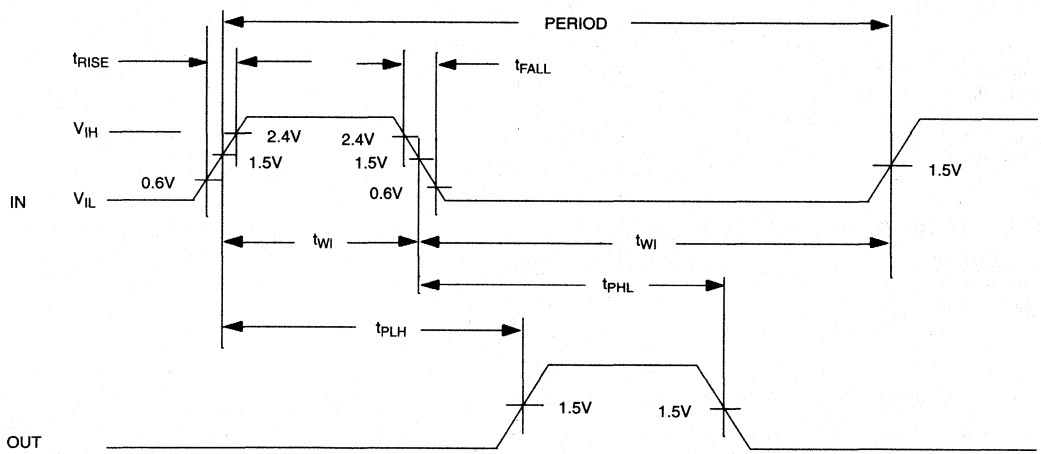
(T_A= 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	

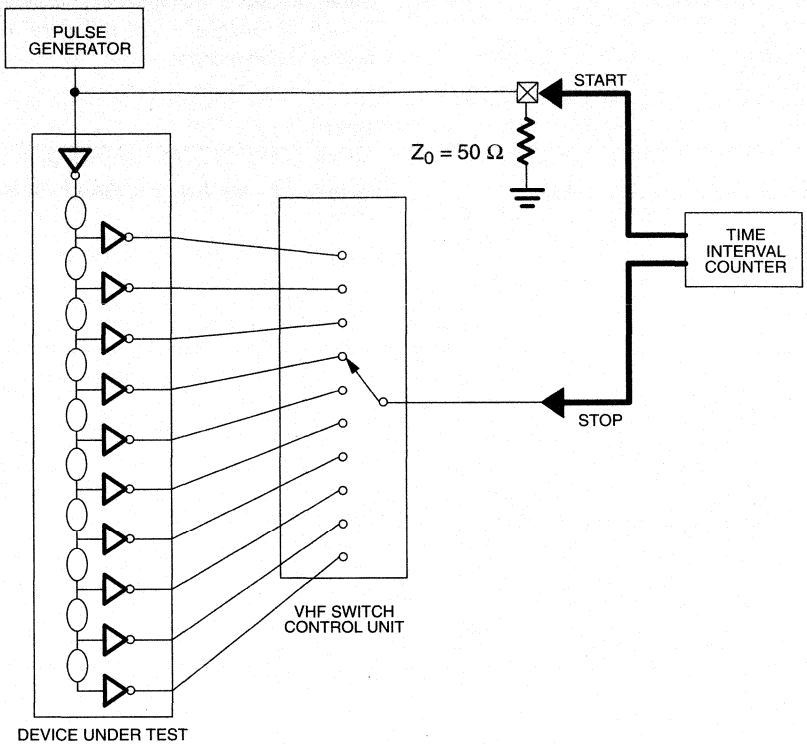
NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open.
3. V_{CC}= 5V @ 25°C. Input-to-tap delays accurate on both rising and falling edges within ±2 ns or ±5% whichever is greater.
4. See "Test Conditions" section.
5. For DS1010 delay lines with a TAP 10 delay of 100 ns or greater, temperature variations from 25°C to 0°C or 70°C may produce an additional input-to-tap delay shift of ±2ns or ±3%, whichever is greater.
6. For DS1010 delay lines with a TAP 10 delay less than 100 ns, temperature variations from 25°C to 0°C or 70°C may produce an additional input-to-tap delay shift of ±1 ns or ±9%, whichever is greater.
7. All tap delays tend to vary unidirectionally with temperature or voltage changes. For example, if TAP 1 slows down, all other taps will also slow dow; TAP 3 can never be faster than TAP 2.
8. Pulse width and period specifications may be exceeded; however, accuracy will be application-sensitive (de-coupling, layout, etc.).
9. Certain high-frequency applications not recommended for -50 in 16-pin package. Consult factory.

TIMING DIAGRAM: SILICON DELAY LINE Figure 2



TEST CIRCUIT Figure 3



TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any tap output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any tap output pulse.

TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1010. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each tap. Each tap is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

INPUT:

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V
	Low = 0.0V ± 0.1V
Source Impedance:	50 ohm Max.
Rise and Fall Time:	3.0 ns Max.
Pulse Width:	500 ns (1 µs for -500)
Period:	1 µs (2 µs for -500)

OUTPUT:

Each output is loaded with the equivalent of one 74FO4 input gate. Delay is measured at the 1.5V level on the rising and falling edge.

NOTE:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

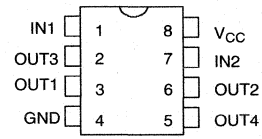
DALLAS SEMICONDUCTOR

DS1012
2-in-1 Sub-Miniature Silicon Delay Line with Logic

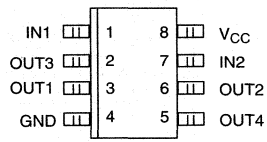
FEATURES

- All-silicon time delay
- 53 µW max. CMOS quiescent mode
- Surface mount 8-pin mini-SOIC and standard 8-pin DIP
- 2 independent buffered delays per input
- Option of complemented output(s)
- Option of timed AND, NAND, OR, NOR, XOR, XNOR, HALF-XOR and HALF-XNOR logic outputs
- Delay tolerance: ±1.5 ns (delays: 3-10 ns), ±2.0 ns (delays: 11-40 ns)
- Vapor phase, IR and wave solderability
- Economical
- TTL/CMOS-compatible
- Quick turn prototypes
- Custom delays and logic options available

PIN ASSIGNMENT



DS1012M 8-PIN DIP (300 MIL)
See Mech. Drawings Section



DS1012Z 8-PIN SOIC (150 MIL)
See Mech. Drawings Section

PIN DESCRIPTION

IN1, IN2	–	Inputs
OUT1, OUT2	–	Outputs (delays)
OUT3, OUT4	–	Outputs (delays, logic)
GND	–	Ground
V_{CC}	–	+5 Volts

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DESCRIPTION

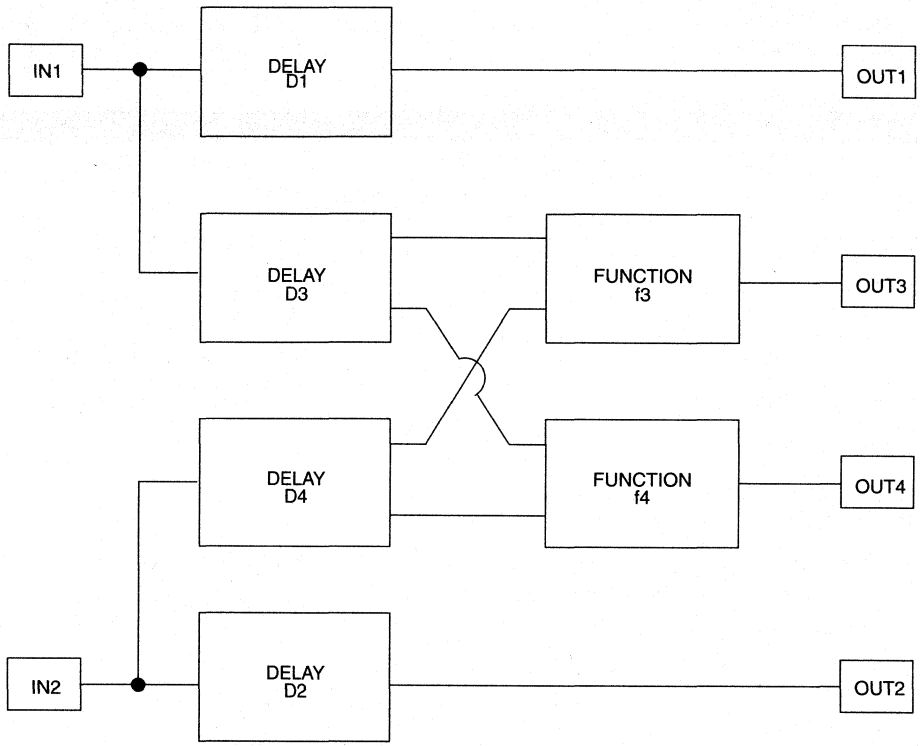
In its most simple configuration, the DS1012 2-in-1 Sub-Miniature Silicon Delay Line Chip provides two inputs, each of which in turn provides independent delays to a pair of outputs. The DS1012-1 and DS1012-3 are examples of catalog parts having this basic configuration. Any of the four outputs can be inverted at the time of manufacture.

For applications requiring two-input timed logic functions, at the time of manufacture the simple delay on OUT4 can be replaced by one of the following: OR, NOR, XOR, or XNOR. Similarly, a timed AND, NAND, HALF-XOR (D3 AND $\overline{D4}$), or NOT HALF-XOR ($\overline{D3}$ OR D4) can be substituted for the simple delay on OUT3. DS1012-2, DS1012-4, and DS1012-5 are examples of catalog parts configured with logic functions on OUT3 and OUT4. Note that DS1012-2 also utilizes an output inversion on OUT2.

In any configuration, delays D1 (t_{D1}) and D2 (t_{D2}) can be specified within the range of ~3 ns to 10 ns. Delays D3 (t_{D3}) and D4 (t_{D4}) can be specified to have values between ~3 ns and 40 ns. The worst case leading edge delay accuracy at nominal voltage and room temperature is ±2 ns. The DS1012 is offered in two packages: an 8-pin DIP and an 8-pin 150 mil wide mini-SOIC.

Dallas Semiconductor offers the DS1012 in a wide variety of custom delay and logic configurations. For special requests and quick turn delivery, call (214) 450-5348.

LOGIC DIAGRAM Figure 1



Function f3 can be one of the following:

D3	$\overline{D3}$
D3 AND D4	D3 NAND D4
D3 HALF-XOR D4	D3 HALF-XNOR D4

Function f4 can be one of the following:

D4	$\overline{D4}$
D3 OR D4	D3 NOR D4
D3 XOR D4	D3 XNOR D4

NOTE: Any output(s) can be inverted at time of manufacture.
If D1 > 10 ns, D1 = D3.
If D2 > 10 ns, D2 = D4.

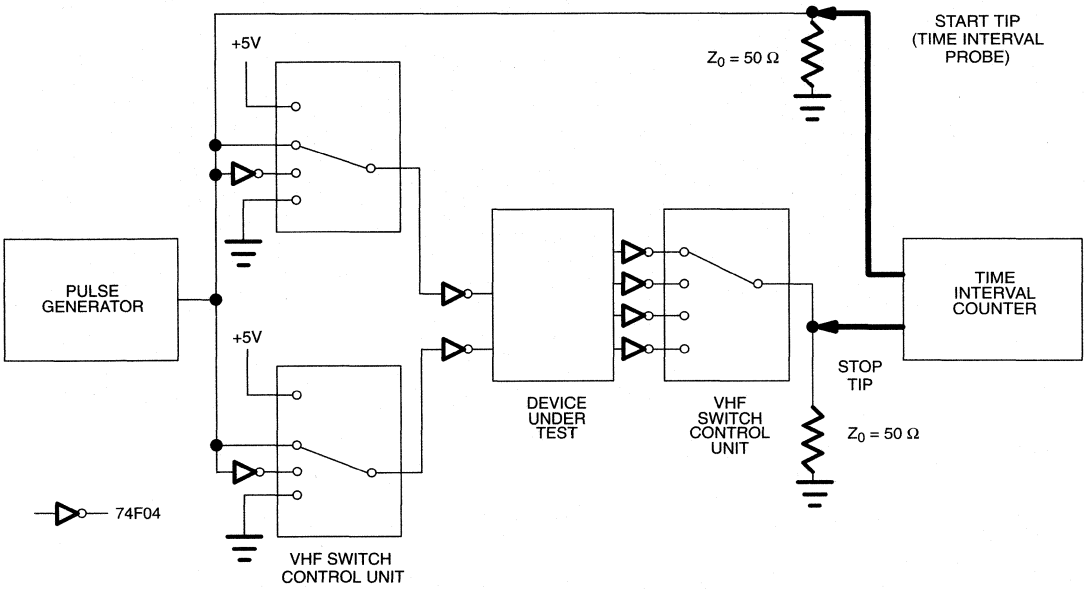
PART NUMBER DELAY AND CONFIGURATION Table 1

CATALOG P/N	t_{D1} (ns)	t_{D2} (ns)	t_{D3} (ns)	t_{D4} (ns)	OUT1	OUT2	OUT3	OUT4
DS1012-1	5	5	10	10	D1	D2	D3	D4
DS1012-2	5	5	10	10	D1	$\overline{D2}$	D3.D4	D3+D4
DS1012-3	3	7	10	40	D1	D2	D3	D4
DS1012-4	5	5	25	25	D1	D2	D3HXD4	D3XD4
DS1012-5	10	10	5	5	D1	D2	D3.D4	D3+D4
DS1012-7	15	4	4	14	D1	$\overline{D2}$	D3	D3XD4
DS1012–9	5	25	5	25	D1	D2	$\overline{D3HXD4}$	D3XD4
DS1012-D16	4	19.6	4	19.6	D1	D2	$\overline{D3.D4}$	D3XD4
DS1012-D20	4	16.5	4	16.5	D1	D2	$\overline{D3.D4}$	D3XD4
DS1012-D25	4	14	4	14	D1	D2	$\overline{D3.D4}$	D3XD4
DS1012-D33	4	11.5	4	11.5	D1	D2	$\overline{D3.D4}$	D3XD4
DS1012-D50	4	9	4	9	D1	D2	$\overline{D3.D4}$	D3XD4
DS1012-V20	25	50	25	50	D1	D2	$\overline{D3.D4}$	$\overline{D3+D4}$
DS1012-V40	12.5	25	12.5	25	D1	D2	$\overline{D3.D4}$	D3XD4
DS1012-V50	10	20	10	20	D1	D2	$\overline{D3.D4}$	D3XD4
DS1012-V60	8.3	8.3	8.3	8.3	D1	D2	$\overline{D3.D4}$	$\overline{D3+D4}$

NOTE: . = AND, + = OR, X = XOR, HX = HALF–XOR

Contact Dallas Semiconductor for information on custom configurations and timing delays.

TEST CIRCUIT Figure 2



7

TEST SETUP DESCRIPTION

Figure 2 illustrates the hardware configuration used for measuring the timing parameters on the DS1012. The input waveform is produced by a precision pulse generator under software control connected to the inputs by VHF switch control units. Time delays are measured by a time interval counter (20 ps resolution) connected between the inputs and the outputs. Outputs are connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

INPUT:

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V
	Low = 0.0V ± 0.1V
Source Impedance:	50 ohms max.
Rise and Fall Time:	3.0 ns max.
Pulse Width:	50 ns
Period:	100 ns

OUTPUT:
Each output is loaded with a 74F04. Delay is measured between the 1.5V level of the rising edge of the input signal and the 1.5V level of the corresponding edge of the output.

NOTE: These conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5.0V ± 5%)

PARAMETER	SYMBOL	TEST	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC}+0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0.0V \le V_I \le V_{CC}$	-1.0		1.0	µA	
Active Current	I_{CC1}	V_{CC} = MAX; PERIOD = MIN		40.0	70.0	mA	2
Quiescent Current	I_{CC2}	V_{CC} = MAX.			10	µA	5
High Level Output Current	I_{OH}	V_{CC} = MIN V_{OH} = 2.4V			-1.0	mA	
Low Level Output Current	I_{OL}	V_{CC} = MIN. V_{OL} = 0.5V	8.0			mA	

AC ELECTRICAL CHARACTERISTICS

(T_A = 25°C; V_{CC} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}				ns	6
Input to Output (leading edge)	t_{D1}, t_{D2}, t_{D3}, t_{D4}				ns	3, 4
Power-up Time	t_{PU}			0	ns	7
	Period	$2(t_{WI})$			ns	

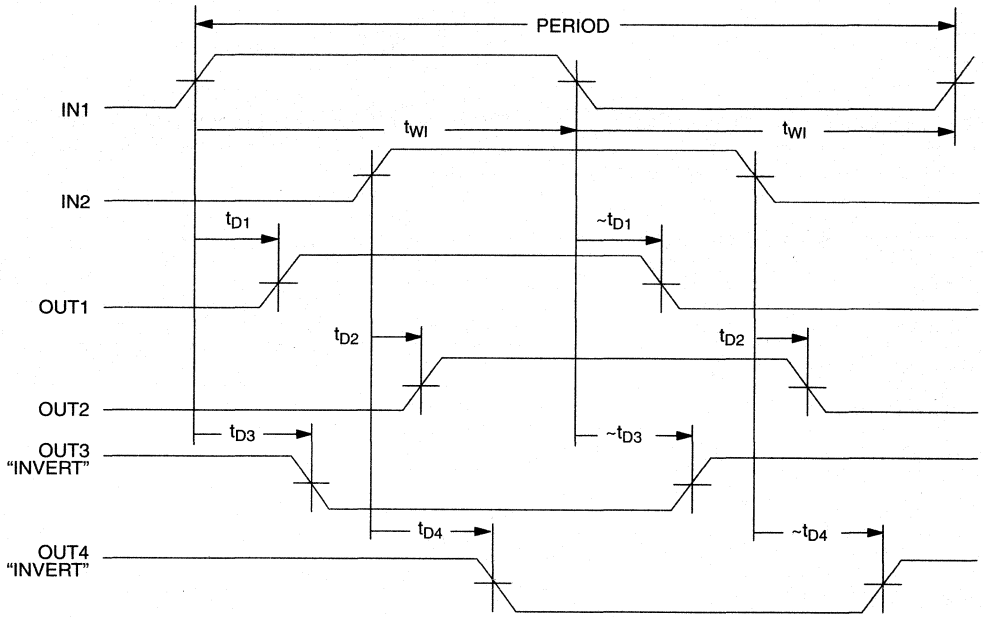
CAPACITANCE

(T_A = 25°C)

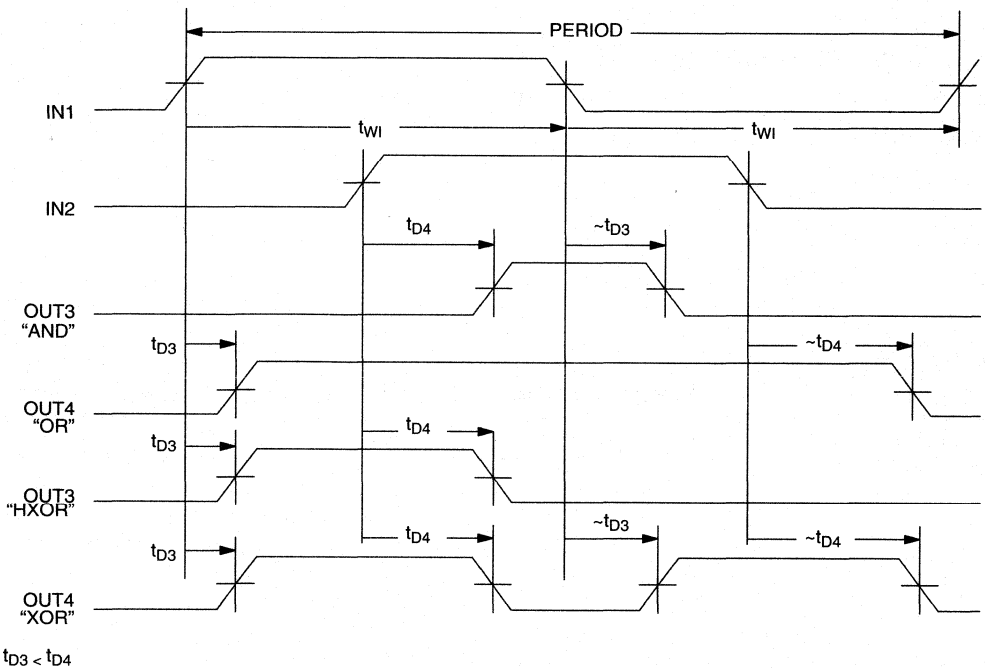
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	

7

DELAY FUNCTION Figure 3



LOGIC FUNCTIONS Figure 4



NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open, minimum period. I_{CC1} (max.) for any value of Period can be calculated using the formula:

   I_{CC1} (max.) = 840/Period + I_{CC2}

   where I_{CC1}, I_{CC2} in mA, Period in ns

   Example: If Period = 50 ns then

   I_{CC1} (Max) = 840/50 + 0.01 = 16.81 mA
3. V_{CC} = 5V @ 25°C. Delays referenced to leading (input rising) edges are accurate within ±1.5 ns for values between 3 to 10 ns and ±2 ns for values between 11 to 40 ns. Delays referenced to trailing (input falling) edges will typically equal the corresponding leading edge delay within ±1 ns.
4. See the section entitled "Test Conditions."
5. For the quiescent mode, both inputs must meet the conditions
   $0.3V > V_I$ or $VI > V_{CC} - 0.3$
6. For specified accuracy, t_{WI} (min) is the longer of $3(t_{D1})$, $3(t_{D2})$, $3(t_{D3})$, or $3(t_{D4})$. Pulse doublers designed for single frequency use will meet specified accuracies at 50% duty cycle; i.e., $2(t_{WI})$ = 1/FREQ = PERIOD. Customs will be adjusted to be accurate at customer input width specifications when t_{WI} is longer than t_{D1}, t_{D2}, t_{D3}, and t_{D4}.
7. On power-up, the DS1012 will supply timing and logic functions with specified accuracy as soon as V_{CC} achieves nominal value.

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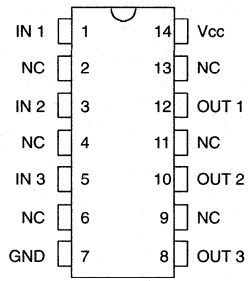
DALLAS SEMICONDUCTOR

DS1013
3-in-1 Silicon Delay Line

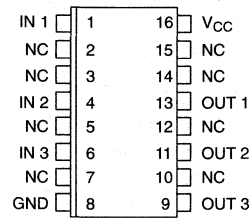
FEATURES

- All-silicon time delay
- 3 independent buffered delays
- Delay tolerance ±2ns for -10 through -60
- Stable and precise over temperature and voltage range
- Leading and trailing edge accuracy
- Economical
- Auto-insertable, low profile
- Standard 14-pin DIP, 8-pin DIP, or 16-pin SOIC
- Low-power CMOS
- TTL/CMOS-compatible
- Vapor phase, IR and wave solderable
- Custom delays available
- Quick turn prototypes
- Extended temperature ranges available

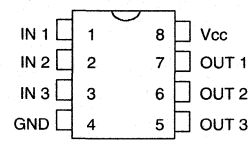
PIN ASSIGNMENT



DS1013 14-PIN DIP (300 MIL)
See Mech. Drawings Section



DS1013S 16-PIN SOIC
(300 MIL)
See Mech. Drawings Section



DS1013M 8-PIN DIP (300 MIL)
See Mech. Drawings Section

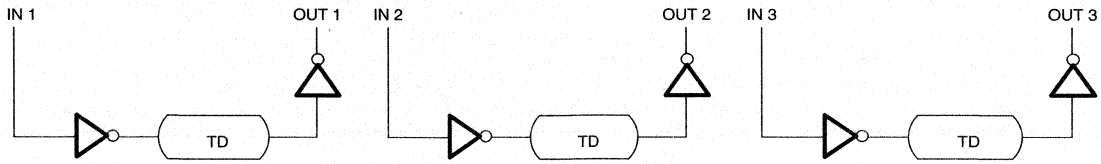
PIN DESCRIPTION

IN 1, IN 2, IN 3	– Inputs
OUT 1, OUT 2, OUT 3	– Outputs
GND	– Ground
V_{CC}	– +5 Volts
NC	– No Connection

DESCRIPTION

The DS1013 series of delay lines has three independent logic buffered delays in a single package. The devices are offered in a standard 14-pin DIP which is pin-compatible with hybrid delay lines. Alternative 8-pin DIP and surface mount packages are available which save PC board area. Since the DS1013 products are an all silicon solution, better economy is achieved when compared to older methods using hybrid techniques. The DS1013 series delay lines provide a nominal accuracy of ±2ns for delay times ranging from 10 ns to 60 ns, increasing to 5% for delays of 150 ns and longer. The DS1013 delay line reproduces the input logic state at the output after a fixed delay as specified by the dash number extension of the part number. The DS1013 is designed to reproduce both leading and trailing edges with equal precision. Each output is capable of driving up to ten 74LS loads. Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (214) 450-5348.

LOGIC DIAGRAM Figure 1



PART NUMBER DELAY TABLE (t_{PHL}, t_{PLH},) Table 1

PART NO.	DELAY PER OUTPUT (ns)
DS1013-10	10/10/10
DS1013-12	12/12/12
DS1013-15	15/15/15
DS1013-20	20/20/20
DS1013-25	25/25/25
DS1013-30	30/30/30
DS1013-35	35/35/35
DS1013-40	40/40/40
DS1013-45	45/45/45
DS1013-50	50/50/50
DS1013-60	60/60/60
DS1013-70*	70/70/70
DS1013-75*	75/75/75
DS1013-80*	80/80/80
DS1013-100*	100/100/100
DS1013-150**	150/150/150
DS1013–200**	200/200/200

Custom delays available.

* ±3% tolerance.

** ±5% tolerance.

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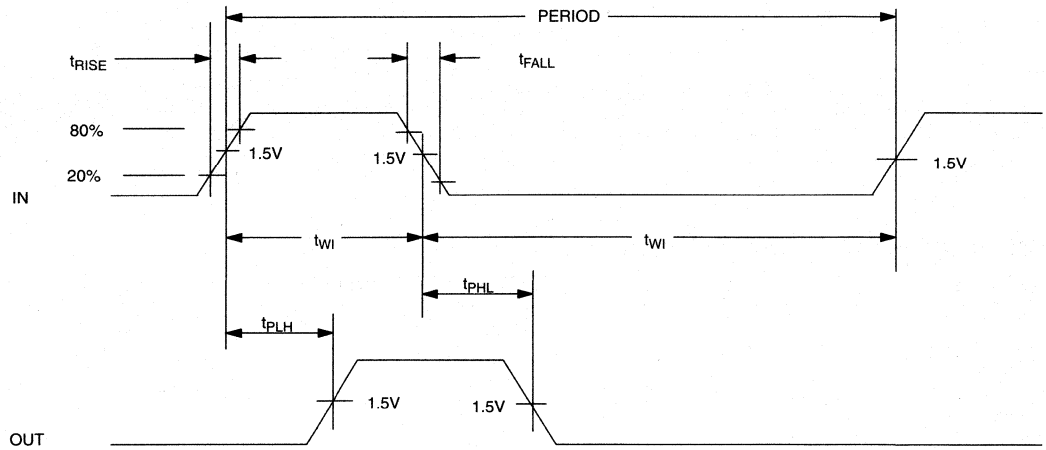
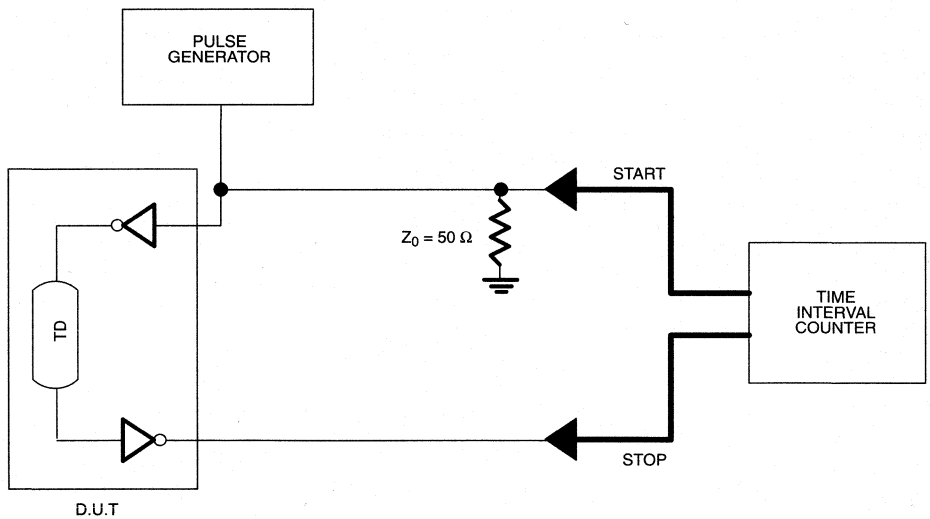
TIMING DIAGRAM: SILICON DELAY LINE Figure 2



TEST CIRCUIT Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}= 5.0V ± 5%)

PARAMETER	SYMBOL	TEST COND.	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC}+0.5		
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	0.0V ≤ VI ≤ V_{CC}	-1.0		1.0	µA	
Active Current	I_{CC}	V_{CC}= Max Period= Min.		40	70	mA	2
High Level Output Current	I_{OH}	V_{CC}= Min. V_{OH}= 4.0V			-1.0	mA	
Low Level Output Current	I_{OL}	V_{CC}=Min V_{OL}=0.5V	12.0			mA	

AC ELECTRICAL CHARACTERISTICS

(T_A= 25°C; V_{CC} = 5.0V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}	100% of t_{PLH}			ns	
Input to Output Delay (leading edge)	t_{PLH}		Table 1		ns	3,4,5,6
Input to Output Delay (trailing edge)	t_{PHL}		Table 1		ns	3,4,5,6
Power-up Time	t_{PU}			100	ms	
	Period	3(t_{WI})			ns	7

CAPACITANCE

(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	

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NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open.
3. V_{CC}= 5V @ 25°C. Delays accurate on both rising and falling edges within ±2 ns for -10 to -60, ±3% for -70 to -100 and ±5% for -150 and longer delays.
4. See "Test Conditions" section.
5. The combination of temperature variations from 25°C to 0°C or 25°C to 70°C and voltage variations from 5.0V to 4.75V or 5.0V to 5.25V may produce an additional delay shift of ±1.5 ns or ±3%, whichever is greater.
6. All output delays tend to vary unidirectionally over temperature or voltage ranges (i.e., if OUT 1 slows down, all other outputs also slow down).
7. Period specifications may be exceeded; however, accuracy will be application-sensitive (decoupling, layout, etc.).

TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of the corresponding output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of the corresponding output pulse.

TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1013. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between each input and corresponding output. Each output is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

INPUT:

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V
	Low = 0.0V ± 0.1V
Source Impedance:	50 ohms Max.
Rise and Fall Time:	3.0 ns Max.
Pulse Width:	500 ns
Period:	1 µs

OUTPUT:

Each output is loaded with the equivalent of one 74F04 input gate. Delay is measured at the 1.5V level on the rising and falling edge.

NOTE:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

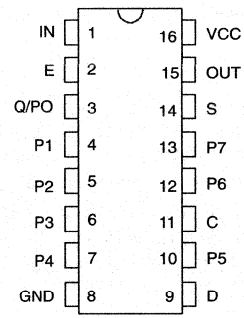
DALLAS SEMICONDUCTOR

DS1020
Programmable 8-Bit Silicon Delay Line

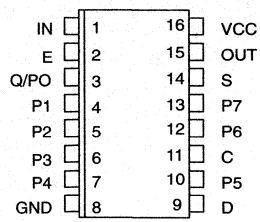
FEATURES

- All-silicon time delay
- Models with 0.15 ns, 0.25 ns, 0.5 ns, 1 ns, and 2 ns steps
- Programmable using 3-wire serial port or 8-bit parallel port
- Leading and trailing edge accuracy
- Standard 16-pin DIP or 16-pin SOIC
- Economical
- Auto-insertable, low profile
- Low-power CMOS
- TTL/CMOS-compatible
- Vapor phase, IR and wave solderable

PIN ASSIGNMENT



DS1020 16-PIN DIP
(300 MIL)
See Mech. Drawings Section



DS1020S 16-PIN SOIC
(300 MIL)
See Mech. Drawings Section

PIN DESCRIPTION

IN	–	Delay Input
P0-P7	–	Parallel Program Pins
GND	–	Ground
OUT	–	Delay Output
VCC	–	+5 Volts
S	–	Mode Select
E	–	Enable
C	–	Serial Port Clock
Q	–	Serial Data Output
D	–	Serial Data Input

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DESCRIPTION

The DS1020 Programmable 8-Bit Silicon Delay Line consists of an 8-bit, user-programmable CMOS silicon integrated circuit. Delay values, programmed using either the 3-wire serial port or the 8-bit parallel port, can be varied over 256 equal steps. The fastest model (-15) offers a maximum delay of 48.25 ns with an incremental delay of 0.15 ns, while the slowest model (-200) has a maximum delay of 520 ns with an incremental delay of 2 ns. All models have an inherent (step zero) delay of 10 ns. After the user-determined delay, the input logic state is reproduced at the output without inversion. The DS1020 is TTL- and CMOS-compatible, capable of driving 10 74LS-type loads, and features both rising and falling edge accuracy.

The all-CMOS DS1020 integrated circuit has been designed as a reliable, economic alternative to hybrid programmable delay lines. It is offered in a standard 16-pin auto-insertable DIP and a space-saving surface mount 16-pin SOIC.

PARALLEL MODE (S = 1)

In the PARALLEL programming mode, the output of the DS1020 will reproduce the logic state of the input after a delay determined by the state of the eight program input pins P0 - P7. The parallel inputs can be programmed using DC levels or computer-generated data. For infrequent modification of the delay value, jumpers may be used to connect the input pins to V_{CC} and ground. For applications requiring frequent timing adjustment, DIP switches should be used. The enable pin (E) must be at a logic 1 in hardwired implementations.

Maximum flexibility is obtained when the eight parallel programming bits are set using computer-generated data. When the data setup (t_{DSE}) and data hold (t_{DHE}) requirements are observed, the enable pin can be used to latch data supplied on an 8-bit bus. Enable must be held at a logic 1 if it is not used to latch the data. After each change in delay value, a settling time (t_{EDV} or t_{PDV}) is required before input logic levels are accurately delayed.

Since the DS1020 is a CMOS design, unused input pins (D and C) must be connected to well-defined logic levels; they must not be allowed to float.

SERIAL MODE (S = 0)

In the SERIAL programming mode, the output of the DS1020 will reproduce the logic state of the input after a delay time determined by an 8-bit value clocked into serial port D. While observing data setup (t_{DSC}) and data hold (t_{DHC}) requirements, timing data is loaded in MSB-to-LSB order by the rising edge of the serial clock (C). The enable pin (E) must be at a logic 1 to load or read the internal 8-bit input register, during which time the delay is determined by the last value activated. Data transfer ends and the new delay value is activated when enable (E) returns to a logic 0. After each change, a settling time (t_{EDV}) is required before the delay is accurate.

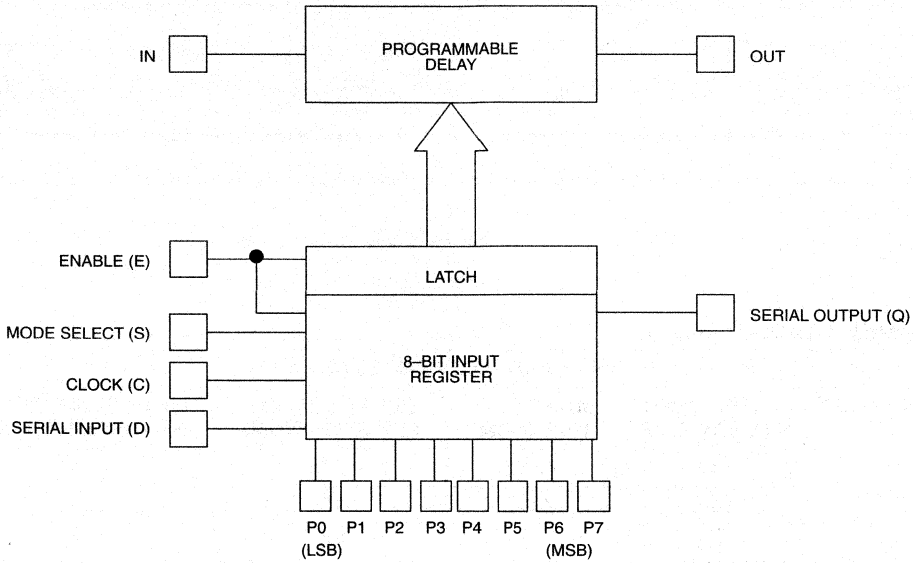
As timing values are shifted into the serial data input (D), the previous contents of the 8-bit input register are shifted out of the serial output pin (Q) in MSB-to-LSB order. By connecting the serial output of one DS1020 to the serial input of a second DS1020, multiple devices can be daisy-chained (cascaded) for programming purposes (Figure 3). The total number of serial bits must be eight times the number of units daisy-chained and each group of 8 bits must be sent in MSB-to-LSB order.

Applications can read the setting of the DS1020 delay line by connecting the serial output pin (Q) to the serial input (D) through a resistor with a value of 1K to 10K ohms (Figure 2). Since the read process is destructive, the resistor restores the value read and provides isolation when writing to the device. The resistor must connect the serial output (Q) of the last device to the serial input (D) of the first device of a daisy-chain (Figure 3). For serial readout with automatic restoration through a resistor, the device used to write serial data must go to a high impedance state.

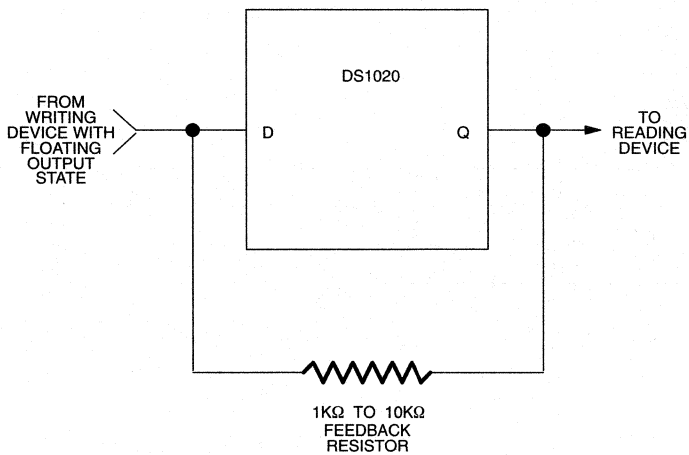
To initiate a serial read, enable (E) is taken to a logic 1 while serial clock (C) is at a logic 0. After a waiting time (t_{EQV}), bit 7 (MSB) appears on the serial output (Q). On the first rising (0 --> 1) transition of the serial clock (C), bit 7 (MSB) is rewritten and bit 6 appears on the output after a time t_{CQV}. To restore the input register to its original state, this clocking process must be repeated 8 times. In the case of a daisy-chain, the process must be repeated 8 times per package. If the value read is restored before enable (E) is returned to logic 0, no settling time (t_{EDV}) is required and the programmed delay remains unchanged.

Since the DS1020 is a CMOS design, unused input pins (P1 - P7) must be connected to well-defined logic levels; they must not be allowed to float. Serial output Q/P0 should be allowed to float if unused.

FUNCTION BLOCK DIAGRAM Figure 1



SERIAL READOUT Figure 2



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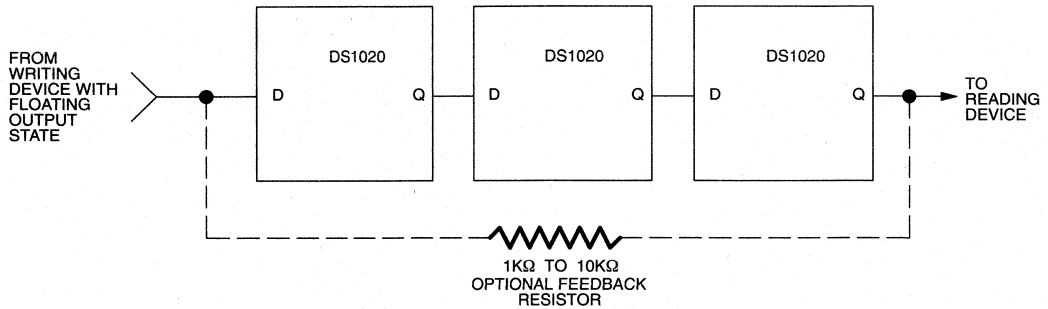
CASCADING MULTIPLE DEVICES (DAISY CHAIN) Figure 3



PART NUMBER TABLE Table 1

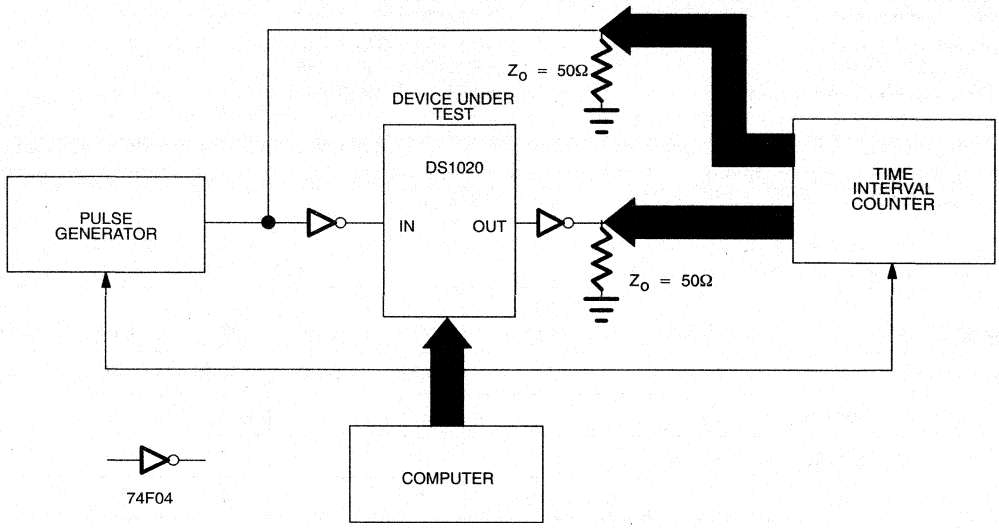
DELAYS AND TOLERANCES (IN ns)				
PART NUMBER	**STEP ZERO DELAY TIME**	**MAX DELAY TIME (NOM)**	**DELAY CHANGE PER STEP (NOM)**	**MAX DEVIATION FROM PROGRAMMED DELAY**
DS1020–15	10 ± 2	48.25	0.15	±4
DS1020–25	10 ± 2	73.75	0.25	±6
DS1020–50	10 ± 2	137.5	0.5	±8
DS1020–100	10 ± 2	265	1	±20
DS1020–200	10 ± 3	520	2	±40

DELAY VS. PROGRAMMED VALUE Table 2

	MIN DELAY (STEP ZERO)								**MAX DELAY**	**PARALLEL PORT**	**SERIAL PORT**
BINARY PROGRAMMED VALUE	0	0	0	0	0	0	1	1	1	P7	MSB
	0	0	0	0	0	0	1	1	1	P6	
	0	0	0	0	0	0	1	1	1	P5	
	0	0	0	0	0	0	1	1	1	P4	
	0	0	0	0	0	0	1	1	1	P3	
	0	0	0	0	1	1	1	1	1	P2	
	0	0	1	1	0	0	0	1	1	P1	
PART NUMBER	0	1	0	1	0	1	1	0	1	P0	LSB
DS1020–15	10.00	10.15	10.30	10.45	10.60	10.75	47.95	48.10	48.25		
DS1020–25	10.00	10.25	10.50	10.75	11.00	11.25	73.25	73.50	73.75		
DS1020–50	10.0	10.5	11.0	11.5	12.0	12.5	136.5	137.0	137.5		
DS1020–100	10	11	12	13	14	15	263	264	265		
DS1020–200	10	12	14	16	18	20	516	518	520		

All delays in nanoseconds, referenced to input pin.

DALLAS SEMICONDUCTOR TEST CIRCUIT Figure 4



TEST SETUP DESCRIPTION

Figure 4 illustrates the hardware configuration used for measuring the timing parameters of the DS1020. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected to the output. The DS1020 serial and parallel ports are controlled by interfaces to a central computer. All measurements are fully automated with each instrument controlled by the computer over an IEEE 488 bus.

TEST CONDITIONS

INPUT:

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V
	Low = 0.0V ± 0.1V
Source Impedance:	50 ohms max.
Rise and Fall Time:	3.0 ns max. (measured between 0.6V and 2.4V)
Pulse Width:	500 ns (DS1020–15)
	500 ns (DS1020–25)
	2 µs (DS1020–50)
	4 µs (DS1020–100)
	4 µs (DS1020–200)
Period:	1 µs (DS1020–15)
	1 µs (DS1020–25)
	4 µs (DS1020–50)
	8 µs (DS1020–100)
	8 µs (DS1020–200)

NOTE: Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

OUTPUT:

Output is loaded with a 74F04. Delay is measured between the 1.5V level of the rising edge of the input signal and the 1.5V level of the corresponding edge of the output.

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5.0V ± 5%)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC}+0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0 \le V_I \le V_{CC}$	-1.0		1.0	µA	
Active Current	I_{CC}	V_{CC} = MAX; PERIOD = 1 µs			30.0	mA	3
High Level Output Current	I_{OH}	V_{CC} = MIN V_{OH} = 2.7V			-1.0	mA	
Low Level Output Current	I_{OL}	V_{CC} = MIN. V_{OL} = 0.5V	8			mA	4

AC ELECTRICAL CHARACATERISTICS

(0°C to 70°C; V_{CC} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock Frequency	f_C			10	MHz	
Enable Width	t_{EW}	50			ns	
Clock Width	t_{CW}	50			ns	
Data Setup to Clock	t_{DSC}	30			ns	
Data Hold from Clock	t_{DHC}	10			ns	
Data Setup to Enable	t_{DSE}	30			ns	
Data Hold from Enable	t_{DHE}	20			ns	
Enable to Serial Output Valid	t_{EQV}			50	ns	
Enable to Serial Output High Z	t_{EQZ}	0		50	ns	
Clock to Serial Output Valid	t_{CQV}			50	ns	
Clock to Serial Output Invalid	t_{CQX}	10			ns	
Enable Setup to Clock	t_{ES}	50			ns	
Enable Hold from Clock	t_{EH}	50			ns	

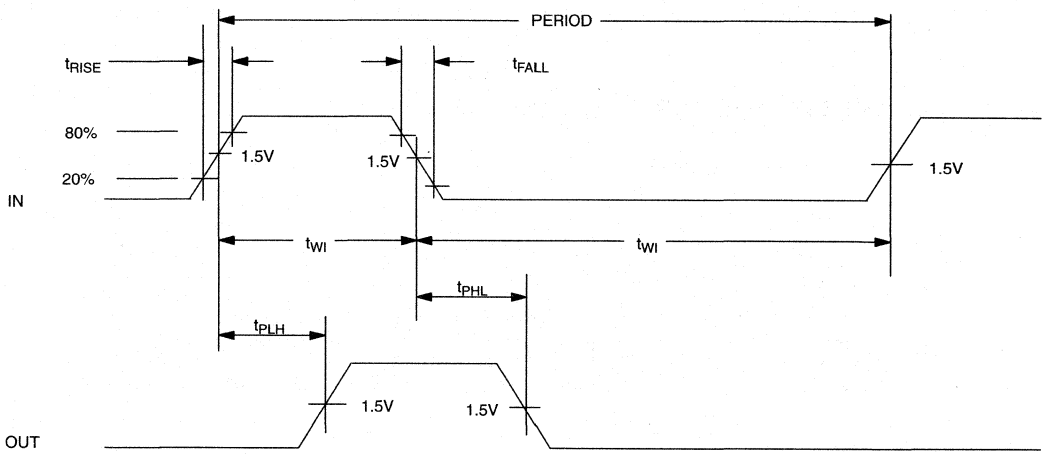
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Parallel Input Valid to Delay Valid	t_{PDV}			50	µs	
Parallel Input Change to Delay Invalid	t_{PDX}	0			ns	
Enable to Delay Valid	t_{EDV}			50	µs	
Enable to Delay Invalid	t_{EDX}	0			ns	
V_{CC} Valid to Device Functional	t_{PU}			100	ms	
Input Pulse Width	t_{WI}	100% of Output Delay			ns	
Input to Output Delay	t_{PLH}, t_{PHL}		Table 2		ns	2
Input Period	Period	$2(t_{WI})$			ns	

CAPACITANCE

(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			10	pF	

TIMING DIAGRAM: SILICON DELAY LINE Figure 5



TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

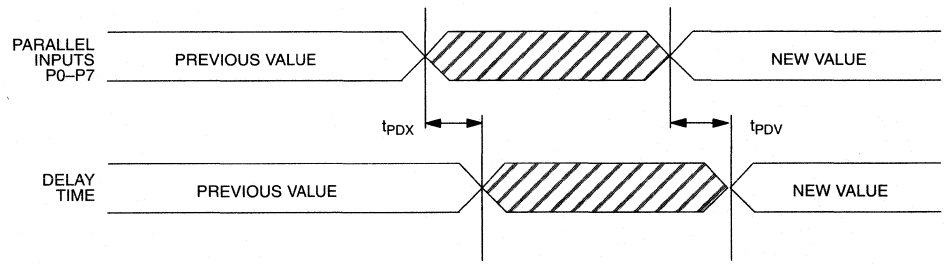
t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

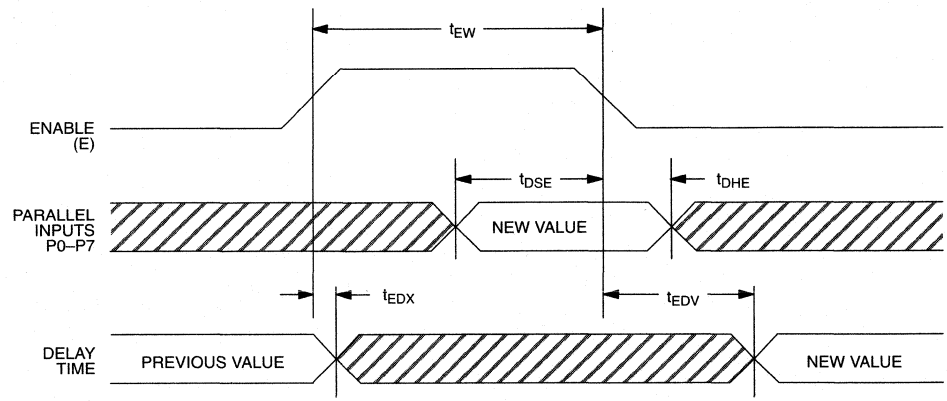
t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of the output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of the output pulse.

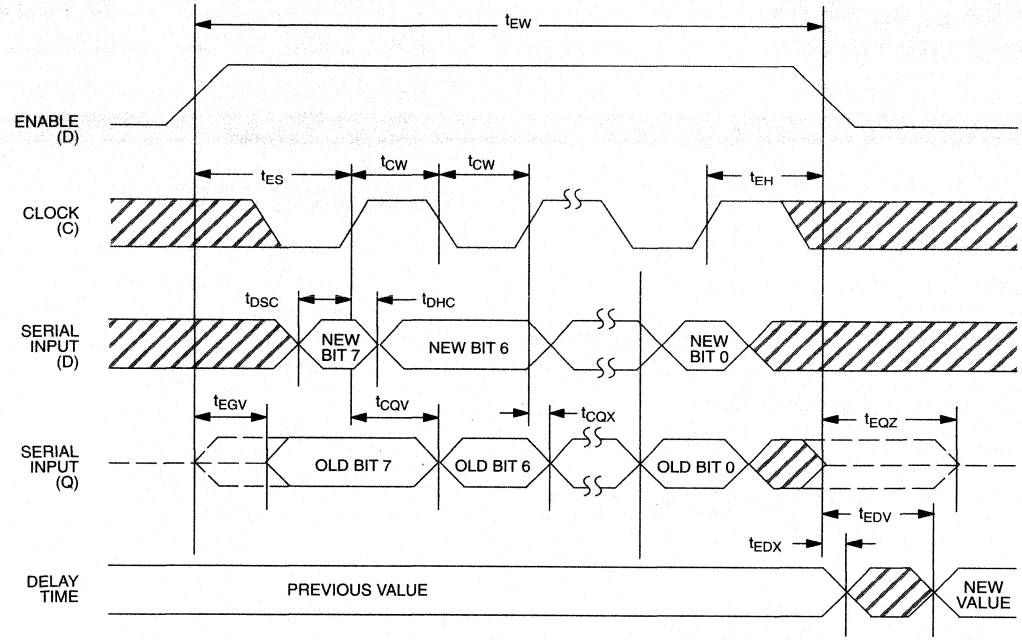
TIMING DIAGRAM: NON-LATCHED PARALLEL MODE (S = 1, E = 1) Figure 6



TIMING DIAGRAM: LATCHED PARALLEL MODE (S=1) Figure 7



TIMING DIAGRAM: SERIAL MODE (S = 0) Figure 8



NOTES:

1. All voltages are referenced to ground.
2. @V_{CC} = 5V and 25°C. Delay accurate on both rising and falling edges within tolerances given in Table 1.
3. Measured with output open.
4. The "Q" output will only source 4 mA. This pin is only intended to drive other DS1020s.

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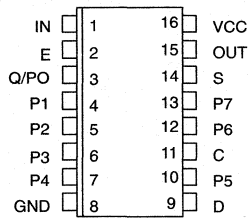
DALLAS SEMICONDUCTOR

DS1021
Programmable 8-Bit Silicon Delay Line

FEATURES

- All-silicon time delay
- Models with 0.25 ns and 0.5 ns steps
- Programmable using 3-wire serial port or 8-bit parallel port
- Leading and trailing edge accuracy
- Economical
- Auto-insertable, low profile, 16–pin SOIC package
- Low-power CMOS
- TTL/CMOS-compatible
- Vapor phase, IR and wave solderable

PIN ASSIGNMENT



DS1021S 16-PIN SOIC (300 MIL)
See Mech. Drawings Section

PIN DESCRIPTION

IN	–	Delay Input
P0-P7	–	Parallel Program Pins
GND	–	Ground
OUT	–	Delay Output
VCC	–	+5 Volts
S	–	Mode Select
E	–	Enable
C	–	Serial Port Clock
Q	–	Serial Data Output
D	–	Serial Data Input

DESCRIPTION

The DS1021 Programmable 8-Bit Silicon Delay Line consists of an 8-bit, user-programmable CMOS silicon integrated circuit. Delay values, programmed using either the 3-wire serial port or the 8-bit parallel port, can be varied over 256 equal steps. The faster model (-25) offers a maximum delay of 73.75 ns with an incremental delay of 0.25 ns, while the slower model (-50) has a maximum delay of 137.5 ns with an incremental delay of 0.5 ns. Both models have an inherent (step zero) delay of 10 ns. After the user-determined delay, the input logic state is reproduced at the output without inversion. The DS1021 is TTL- and CMOS-compatible, capable of driving 10 74LS-type loads, and features both rising and falling edge accuracy.

The all-CMOS DS1021 integrated circuit has been designed as a reliable, economic alternative to hybrid programmable delay lines. It is offered in a space-saving surface mount 16-pin SOIC.

PARALLEL MODE (S = 1)

In the PARALLEL programming mode, the output of the DS1021 will reproduce the logic state of the input after a delay determined by the state of the eight program input pins P0 - P7. The parallel inputs can be programmed using DC levels or computer-generated data. For infrequent modification of the delay value, jumpers may be used to connect the input pins to V_{CC} and ground. For applications requiring frequent timing adjustment, DIP switches should be used. The enable pin (E) must be at a logic 1 in hardwired implementations.

Maximum flexibility is obtained when the eight parallel programming bits are set using computer-generated data. When the data setup (t_{DSE}) and data hold (t_{DHE}) requirements are observed, the enable pin can be used to latch data supplied on an 8-bit bus. Enable must be held at a logic 1 if it is not used to latch the data. After each change in delay value, a settling time (t_{EDV} or t_{PDV}) is required before input logic levels are accurately delayed.

Since the DS1021 is a CMOS design, unused input pins (D and C) must be connected to well-defined logic levels; they must not be allowed to float.

SERIAL MODE (S = 0)

In the SERIAL programming mode, the output of the DS1021 will reproduce the logic state of the input after a delay time determined by an 8-bit value clocked into serial port D. While observing data setup (t_{DSC}) and data hold (t_{DHC}) requirements, timing data is loaded in MSB-to-LSB order by the rising edge of the serial clock (C). The enable pin (E) must be at a logic 1 to load or read the internal 8-bit input register, during which time the delay is determined by the last value activated. Data transfer ends and the new delay value is activated when enable (E) returns to a logic 0. After each change, a settling time (t_{EDV}) is required before the delay is accurate.

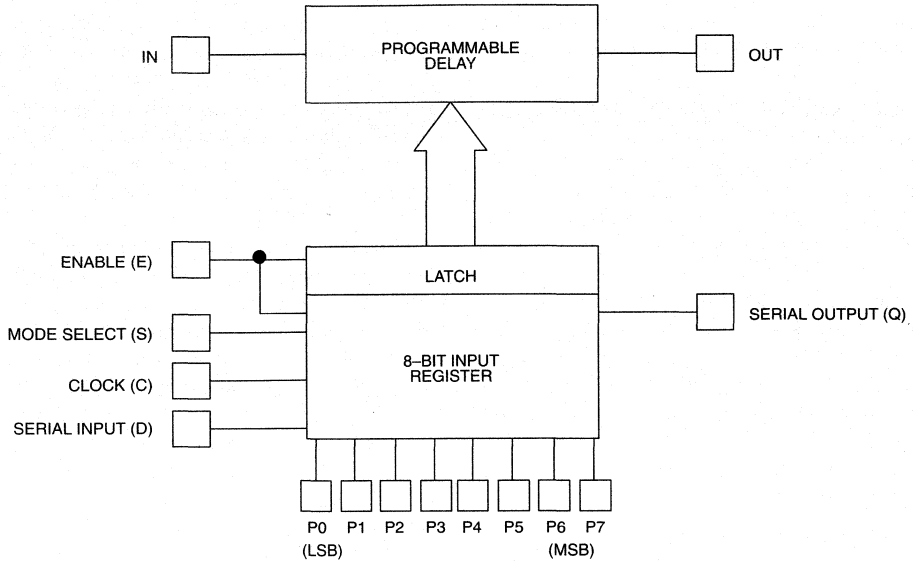
As timing values are shifted into the serial data input (D), the previous contents of the 8-bit input register are shifted out of the serial output pin (Q) in MSB-to-LSB order. By connecting the serial output of one DS1021 to the serial input of a second DS1021, multiple devices can be daisy-chained (cascaded) for programming purposes (Figure 3). The total number of serial bits must be eight times the number of units daisy-chained and each group of 8 bits must be sent in MSB-to-LSB order.

Applications can read the setting of the DS1021 delay line by connecting the serial output pin (Q) to the serial input (D) through a resistor with a value of 1K to 10K ohms (Figure 2). Since the read process is destructive, the resistor restores the value read and provides isolation when writing to the device. The resistor must connect the serial output (Q) of the last device to the serial input (D) of the first device of a daisy-chain (Figure 3). For serial readout with automatic restoration through a resistor, the device used to write serial data must go to a high impedance state.

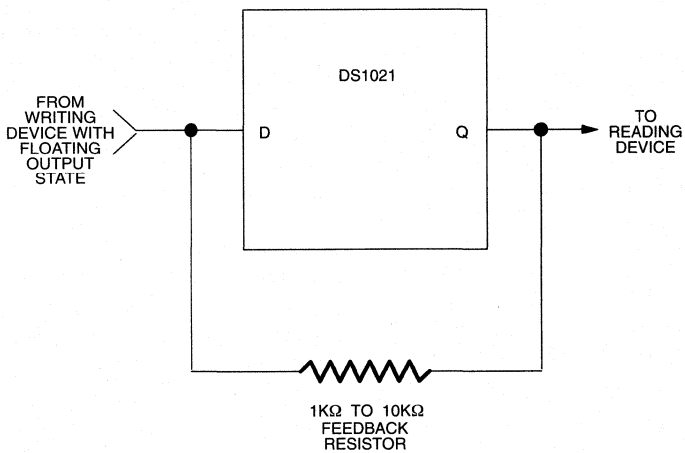
To initiate a serial read, enable (E) is taken to a logic 1 while serial clock (C) is at a logic 0. After a waiting time (t_{EQV}), bit 7 (MSB) appears on the serial output (Q). On the first rising (0 --> 1) transition of the serial clock (C), bit 7 (MSB) is rewritten and bit 6 appears on the output after a time t_{CQV}. To restore the input register to its original state, this clocking process must be repeated 8 times. In the case of a daisy-chain, the process must be repeated 8 times per package. If the value read is restored before enable (E) is returned to logic 0, no settling time (t_{EDV}) is required and the programmed delay remains unchanged.

Since the DS1021 is a CMOS design, unused input pins (P1 - P7) must be connected to well-defined logic levels; they must not be allowed to float. Serial output Q/P0 should be allowed to float if unused.

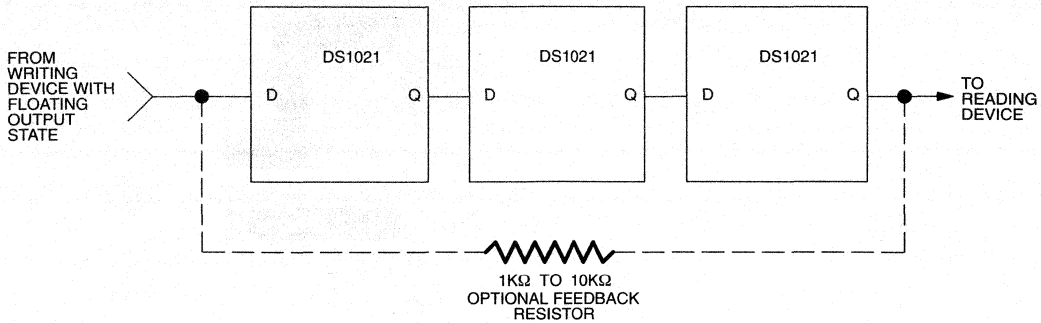
FUNCTION BLOCK DIAGRAM Figure 1



SERIAL READOUT Figure 2



CASCADING MULTIPLE DEVICES (DAISY CHAIN) Figure 3



PART NUMBER TABLE Table 1

DELAYS AND TOLERANCES (IN ns)				
PART NUMBER	**STEP ZERO DELAY TIME**	**MAX DELAY TIME (NOM)**	**DELAY CHANGE PER STEP (NOM)**	**MAX DEVIATION FROM PROGRAMMED DELAY**
DS1021–25	10 ± 2	73.75	0.25	±6
DS1021–50	10 ± 2	137.5	0.5	±8

DELAY VS. PROGRAMMED VALUE Table 2

	MIN DELAY (STEP ZERO)									**MAX DELAY**	**PARALLEL PORT**	**SERIAL PORT**
BINARY PROGRAMMED VALUE	0	0	0	0	0	0		1	1	1	P7	MSB
	0	0	0	0	0	0		1	1	1	P6	
	0	0	0	0	0	0		1	1	1	P5	
	0	0	0	0	0	0		1	1	1	P4	
	0	0	0	0	0	0		1	1	1	P3	
	0	0	0	0	1	1		1	1	1	P2	
	0	0	1	1	0	0		0	1	1	P1	
PART NUMBER	0	1	0	1	0	1		1	0	1	P0	LSB
DS1021–25	10.00	10.25	10.50	10.75	11.00	11.25		73.25	73.50	73.75		
DS1021–50	10.0	10.5	11.0	11.5	12.0	12.5		136.5	137.0	137.5		

All delays in nanoseconds, referenced to input pin.

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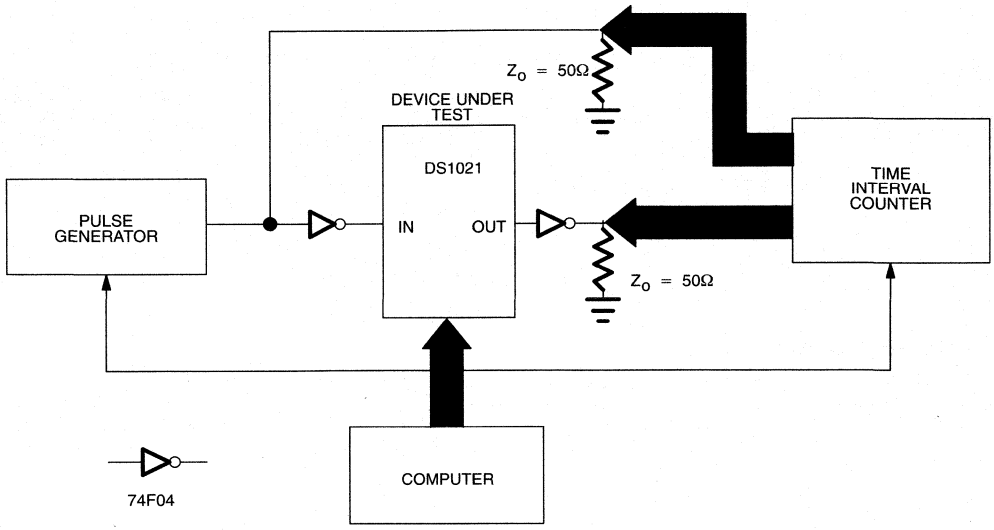
DALLAS SEMICONDUCTOR TEST CIRCUIT Figure 4



TEST SETUP DESCRIPTION

Figure 4 illustrates the hardware configuration used for measuring the timing parameters of the DS1021. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected to the output. The DS1021 serial and parallel ports are controlled by interfaces to a central computer. All measurements are fully automated with each instrument controlled by the computer over an IEEE 488 bus.

TEST CONDITIONS

INPUT:

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V
	Low = 0.0V ± 0.1V
Source Impedance:	50 ohms max.
Rise and Fall Time:	3.0 ns max. (measured between 0.6V and 2.4V)
Pulse Width:	500 ns (DS1021–25)
	2 µs (DS1021–50)
Period:	1 µs (DS1021–25)
	4 µs (DS1021–50)

NOTE: Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

OUTPUT:
Output is loaded with a 74F04. Delay is measured between the 1.5V level of the rising edge of the input signal and the 1.5V level of the corresponding edge of the output.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5.0V ± 5%)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC}+0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0 \le V_I \le V_{CC}$	-1.0		1.0	µA	
Active Current	I_{CC}	V_{CC} = MAX; PERIOD = 1 µs			30.0	mA	3
High Level Output Current	I_{OH}	V_{CC} = MIN V_{OH} = 2.7V			-1.0	mA	
Low Level Output Current	I_{OL}	V_{CC} = MIN. V_{OL} = 0.5V	8			mA	4

AC ELECTRICAL CHARACATERISTICS

(0°C to 70°C; V_{CC} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock Frequency	f_C			10	MHz	
Enable Width	t_{EW}	50			ns	Fig. 7, 8
Clock Width	t_{CW}	50			ns	Fig. 8
Data Setup to Clock	t_{DSC}	30			ns	Fig. 8
Data Hold from Clock	t_{DHC}	10			ns	Fig. 8
Data Setup to Enable	t_{DSE}	30			ns	Fig. 7
Data Hold from Enable	t_{DHE}	20			ns	Fig. 7
Enable to Serial Output Valid	t_{EQV}			50	ns	Fig. 8
Enable to Serial Output High Z	t_{EQZ}	0		50	ns	Fig. 8
Clock to Serial Output Valid	t_{CQV}			50	ns	Fig. 8
Clock to Serial Output Invalid	t_{CQX}	10			ns	Fig. 8
Enable Setup to Clock	t_{ES}	50			ns	Fig. 8
Enable Hold from Clock	t_{EH}	50			ns	Fig. 8

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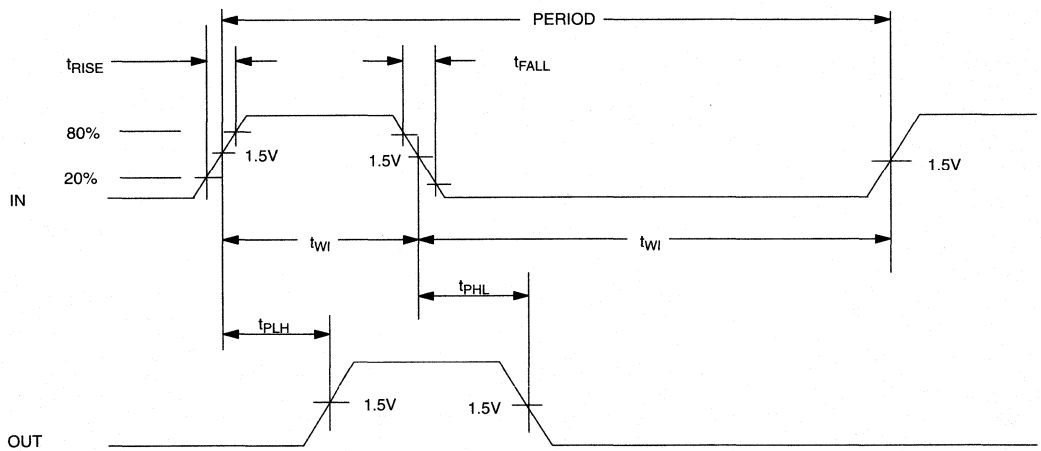
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Parallel Input Valid to Delay Valid	t_{PDV}			50	µs	Fig. 6
Parallel Input Change to Delay Invalid	t_{PDX}	0			ns	Fig. 6
Enable to Delay Valid	t_{EDV}			50	µs	Fig. 7
Enable to Delay Invalid	t_{EDX}	0			ns	Fig. 7
V_{CC} Valid to Device Functional	t_{PU}			100	ms	Fig. 9
V_{CC} Rise Time	t_{VR}	20			ms	Fig. 9
Input Pulse Width	t_{WI}	100% of Output Delay			ns	Fig. 5
Input to Output Delay	t_{PLH}, t_{PHL}		Table 2		ns	2
Input Period	Period	$2(t_{WI})$			ns	

CAPACITANCE

(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			10	pF	

TIMING DIAGRAM: SILICON DELAY LINE Figure 5



TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

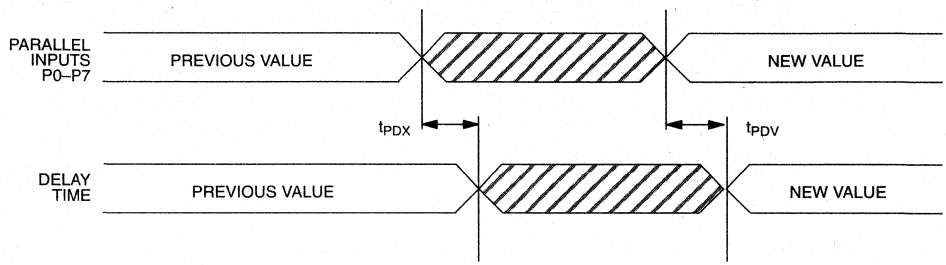
t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

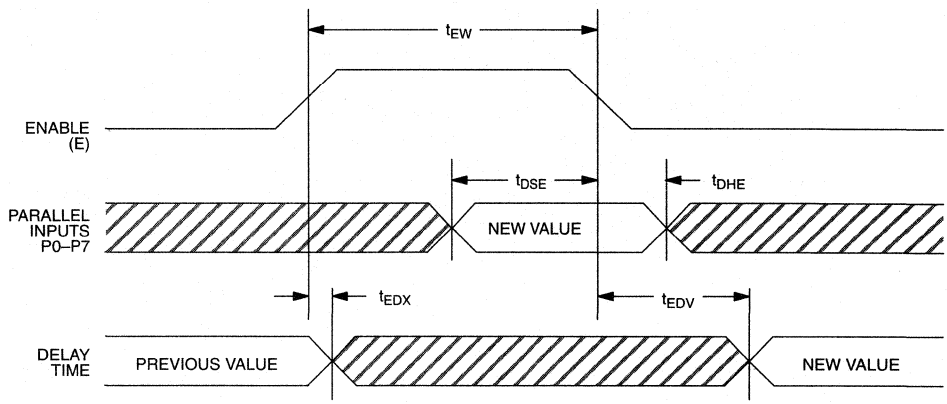
t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of the output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of the output pulse.

TIMING DIAGRAM: NON-LATCHED PARALLEL MODE (S = 1, E = 1) Figure 6



TIMING DIAGRAM: LATCHED PARALLEL MODE (S=1) Figure 7



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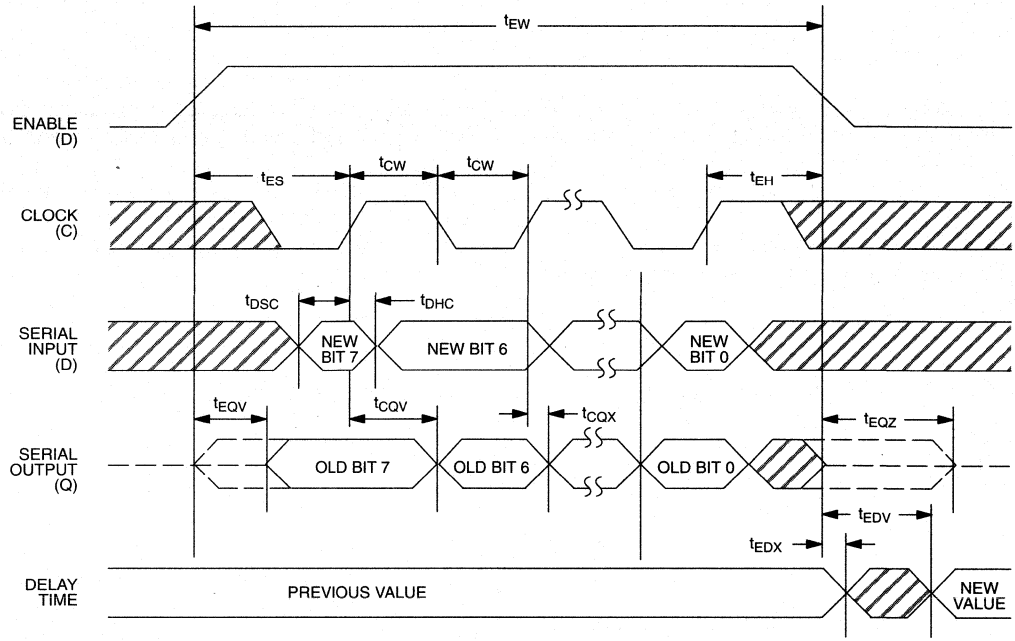
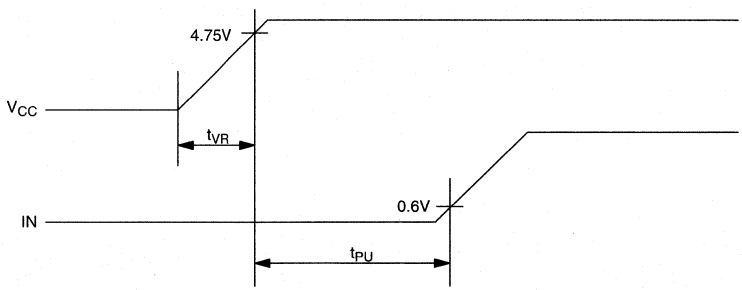
TIMING DIAGRAM: SERIAL MODE (S = 0) Figure 8



TIMING DIAGRAM: POWER UP Figure 9



NOTES:

1. All voltages are referenced to ground.
2. @V_{CC} = 5V and 25°C. Delay accurate on both rising and falling edges within tolerances given in Table 1.
3. Measured with output open.
4. The "Q" output will only source 4 mA. This pin is only intended to drive other DS1021s.

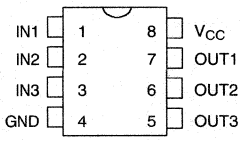
DALLAS SEMICONDUCTOR

DS1033
3–in–1 Low Voltage Silicon Delay Line

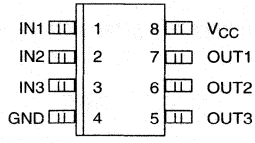
FEATURES

- All–silicon timing circuit
- Three independent buffered delays
- Initial delay tolerance ±1.5 ns
- Stable and precise over temperature and voltage
- Leading and trailing edge precision preserves the input symmetry
- Standard 8–pin DIP, 8–pin SOIC (150 mil) and 20–pin TSSOP
- Vapor phasing, IR and wave solderable
- Available in Tape and Reel

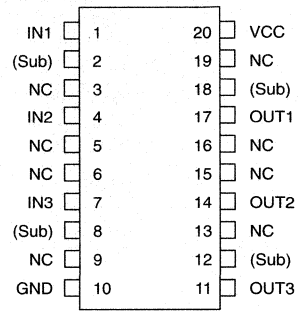
PIN ASSIGNMENT



DS1033M 8–PIN DIP
See Mech. Drawings Section



DS1033Z 8–PIN SOIC (150 MIL)
See Mech. Drawings Section



DS1033E 20–PIN TSSOP
(CONTACT FACTORY FOR AVAILABILITY)
See Mech. Drawings Section

PIN DESCRIPTION

IN1–IN3	–	Input Signals
OUT1–OUT3	–	Output Signals
NC	–	No Connection
V_{CC}	–	Supply Voltage
GND	–	Ground
(Sub)	–	Internal substrate connection, do not make any external connections to these pins

DESCRIPTION

The DS1033 series is a low–power +3.3 Volt version of the DS1035. It is characterized for operation over the range of 2.7V to 3.6V.

The DS1033 series of delay lines have three independent logic buffered delays in a single package. It is available in a standard 8–pin DIP, 150 Mil 8–pin Mini–SOIC and 20–pin TSSOP.

The device features precise leading and trailing edge accuracies. It has the inherent reliability of an all–silicon delay line solution. The DS1033's nominal tolerance is ±1.5 ns and an additional tolerance over temperature and voltage of ±1.0 ns for the faster delays. Detailed specifications are shown in Table 1.

Standard delay values are indicated in Table 1. Customers may contact Dallas Semiconductor at 214–450–5348 for further information.

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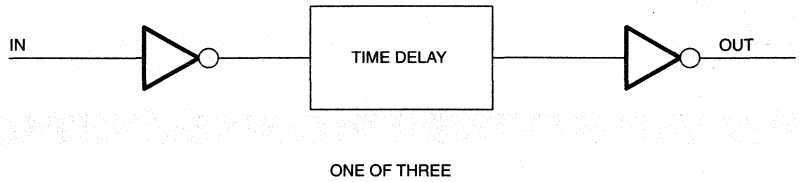
LOGIC DIAGRAM Figure 1



PART NUMBER DELAY TABLE (t_{PLH}, t_{PHL}) Table 1

PART NUMBER	DELAY PER OUTPUT (ns) (note 1)	INITIAL TOLERANCE (note 1)	TOLERANCE OVER TEMPERATURE AND VOLTAGE (note 2)	
			V_{CC}=3.3V ± 0.3V	V_{CC}=2.7V
DS1033–8	8/8/8	±1.5 ns	±1.0 ns	±1.5 ns
DS1033–10	10/10/10	±1.5 ns	±1.0 ns	±1.5 ns
DS1033–12	12/12/12	±1.5 ns	±1.0 ns	±1.5 ns
DS1033–15	15/15/15	±1.5 ns	±1.5 ns	±2.0 ns
DS1033–20	20/20/20	±1.5 ns	±1.5 ns	±2.5 ns
DS1033–25	25/25/25	±2.0 ns	±2.0 ns	±3.5 ns
DS1033–30	30/30/30	±2.0 ns	±2.0 ns	±5.0 ns

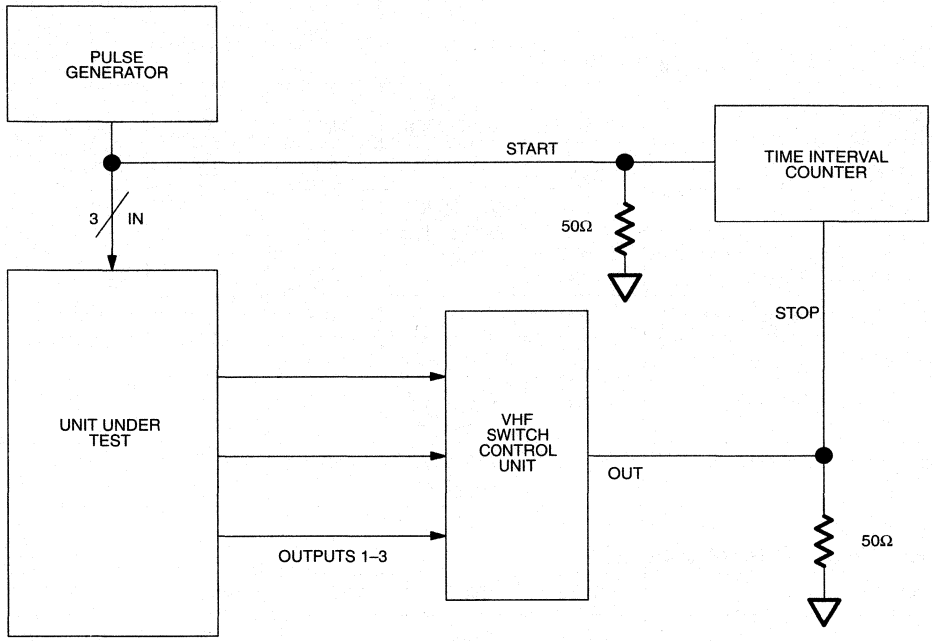
NOTES:

1. Nominal conditions are +25°C and V_{CC}=+3.3 volts.
2. Temperature range of 0°C to 70°C.
3. Delay accuracy is for both leading and trailing edges.

TEST SETUP DESCRIPTION

Figure 2 illustrates the hardware configuration used for measuring the timing parameters of the DS1033. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected to the output. The DS1033 output taps are selected and connected to the interval counter by a VHF switch control unit. All measurements are fully automated with each instrument controlled by the computer over an IEEE 488 bus.

DS1033 TEST CIRCUIT Figure 2



7

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–1.0V to +6.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(T_A=0°C to 70°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		2.7	3.3	3.6	V
Active Current	I_{CC}	V_{CC}=3.6V Period=1µs			25	mA
High Level Input Voltage	V_{IH}		2.0		V_{CC}+0.5	V
Low Level Input Voltage	V_{IL}		–0.5		0.8	V
Input Leakage	I_L	$0V \le V_I \le V_{CC}$	–1.0		1.0	µA
High Level Output Current	I_{OH}	V_{CC}=2.7V V_{OH}=2V			–1.0	mA
Low Level Output Current	I_{OL}	V_{CC}=2.7V V_{OL}=0.4V	8			mA

AC ELECTRICAL CHARACTERISTICS

(T_A=+25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Period	t_{PERIOD}	2 (t_{WI})			ns	2
Input Pulse Width	t_{WI}	100% of Tap Delay			ns	2
Input–to–Tap Output Delay	t_{PLH}, t_{PHL}		Table 1		ns	
Output Rise or Fall Time	t_{OR}, t_{OF}		2.0 3.0	2.5 3.5	ns ns	3 4
Power–up Time	t_{PU}			100	ms	

CAPACITANCE

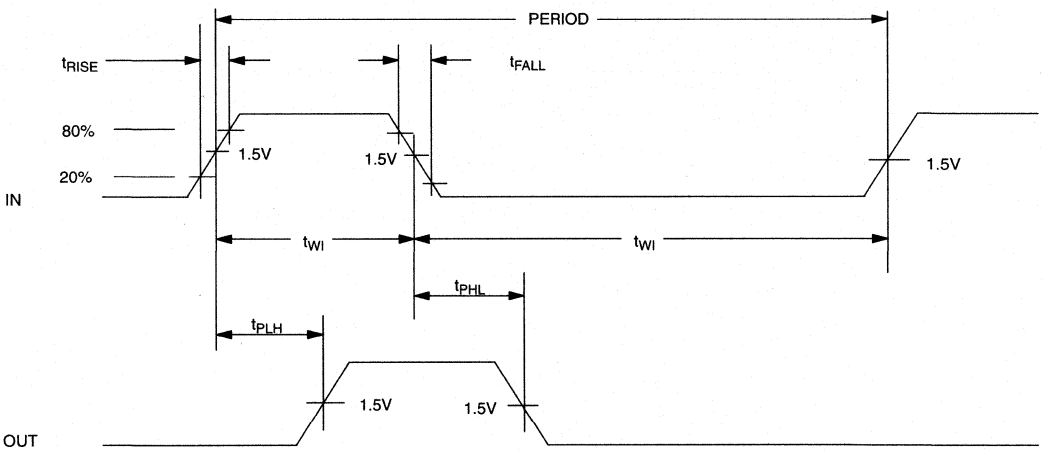
(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			10	pF	

TEST CONDITIONS

Ambient Temperature: 25°C ± 3°C
Supply Voltage (V_{CC}): 3.3V ± 0.1V
Input Pulse:
High: 3.0V ± 0.1V
Low: 0.0V ± 0.1V
Source Impedance: 50Ω Max.
Rise and Fall Time: 3.0 ns Max. – Measured between 0.6V and 2.4V.
Pulse Width: 500 ns
Pulse Period: 1 µs
Output Load Capacitance: 15 pF
Output: Each output is loaded with the equivalent of one 74F04 input gate.
Data is measured at the 1.5V level on the rising and falling edges.
Note: The above conditions are for test only and do not restrict the devices under other data sheet conditions.

TIMING DIAGRAM



NOTES:

1. All voltages are referenced to ground.
2. Pulse width and duty cycle specifications may be exceeded, however, accuracy will be application sensitive with respect to de–coupling, layout, etc.
3. V_{CC}=3.3V ± 10%
4. V_{CC}=2.7V

TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5 volt point on the leading edge and the 1.5 volt point on the trailing edge or the 1.5 volt point on the trailing edge and the 1.5 volt point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge on the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5 volt point on the leading edge of the input pulse and the 1.5 volt point on the leading edge of the output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5 volt point on the falling edge of the input pulse and the 1.5 volt point on the falling edge of the output pulse.

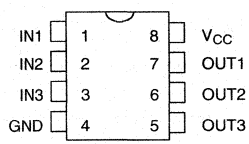
DALLAS SEMICONDUCTOR

DS1035
3–in–1 High–Speed Silicon Delay Line

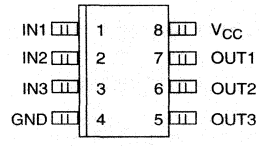
FEATURES

- All–silicon timing circuit
- Three independent buffered delays
- Initial delay tolerance ±2 ns
- Stable and precise over temperature and voltage
- Leading and trailing edge precision preserves the input symmetry
- Standard 8–pin DIP, 8–pin SOIC (150 mil) and 20–pin TSSOP
- Vapor phasing, IR and wave solderable
- Available in Tape and Reel

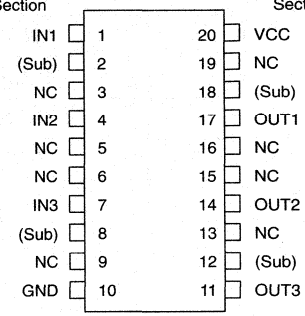
PIN ASSIGNMENT



DS1035M 8–PIN DIP
See Mech. Drawings Section



DS1035Z 8–PIN SOIC (150 MIL)
See Mech. Drawings Section



DS1035E 20–PIN TSSOP
(CONTACT FACTORY FOR AVAILABILITY)
See Mech. Drawings Section

PIN DESCRIPTION

IN1–IN3	–	Input Signals
OUT1–OUT3	–	Output Signals
NC	–	No Connection
V_{CC}	–	+5 Volt Supply
GND	–	Ground
(Sub)	–	Internal substrate connection, do not make any external connections to these pins

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DESCRIPTION

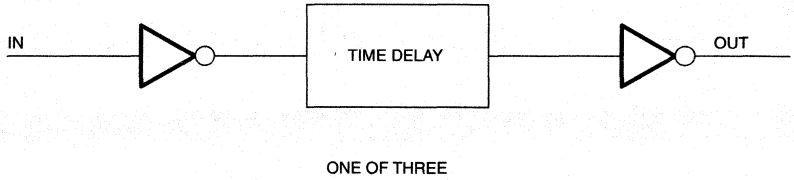
The DS1035 series is a low–power +5 Volt high speed version of the popular DS1013 and compliments the DS1033 +3.3 Volt version.

The DS1035 series of delay lines have three independent logic buffered delays in a single package. The device is Dallas Semiconductor's fastest 3–in–1 delay line. It is available in a standard 8–pin DIP, 150 Mil 8–pin Mini–SOIC and 20–pin TSSOP.

The device features precise leading and trailing edge accuracies. It has the inherent reliability of an all–silicon delay line solution. The DS1035's initial tolerance is ±2 ns with an additional tolerance over temperature and voltage of ±1.0 ns or ±1.5 ns, depending on the delay value. Each output is capable of driving up to 10 LS loads.

Standard delay values are indicated in Table 1. Customers may contact Dallas Semiconductor at 214–450–5348 for further information.

LOGIC DIAGRAM Figure 1



PART NUMBER DELAY TABLE (t_{PLH}, t_{PHL}) Table 1

PART NUMBER	DELAY PER OUTPUT (ns)	INITIAL TOLERANCE	TOLERANCE OVER (temp and voltage)
DS1035–6	6/6/6	±2.0 ns	±1.0 ns
DS1035–8	8/8/8	±2.0 ns	±1.0 ns
DS1035–10	10/10/10	±2.0 ns	±1.0 ns
DS1035–12	12/12/12	±2.0 ns	±1.0 ns
DS1035–15	15/15/15	±2.0 ns	±1.5 ns
DS1035–20	20/20/20	±2.0 ns	±1.5 ns
DS1035–25	25/25/25	±2.0 ns	±1.5 ns
DS1035–30	30/30/30	±2.0 ns	±1.5 ns

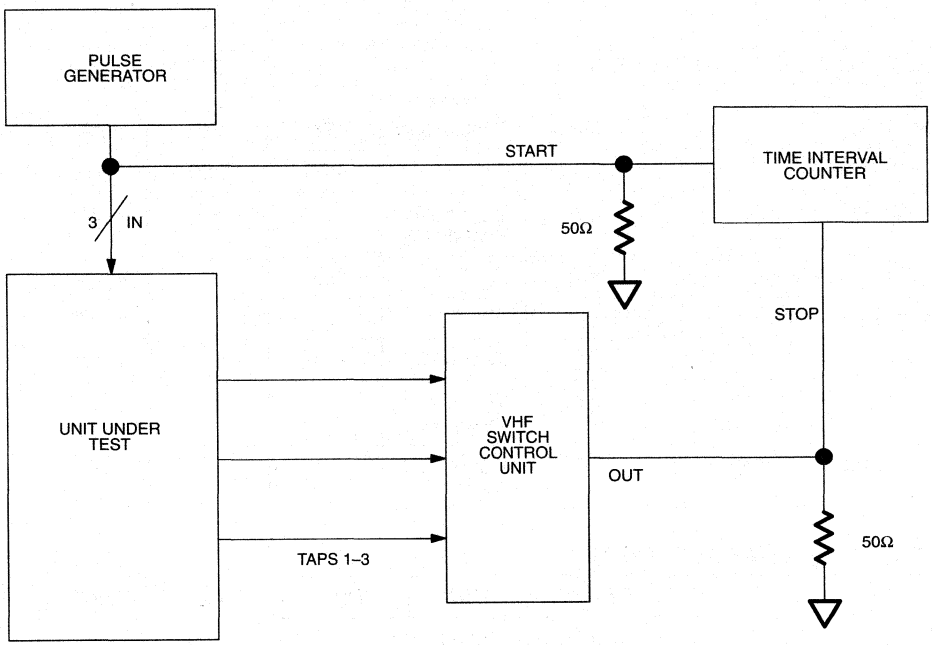
NOTES:

1. Nominal conditions are +25°C and V_{CC}=+5.0 volts.
2. Temperature range of 0°C to 70°C and voltage range of 4.75 volts to 5.25 volts.
3. Delay accuracy are for both leading and trailing edges.

TEST SETUP DESCRIPTION

Figure 2 illustrates the hardware configuration used for measuring the timing parameters of the DS1035. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected to the output. The DS1035 output taps are selected and connected to the interval counter by a VHF switch control unit. All measurements are fully automated with each instrument controlled by the computer over an IEEE 488 bus.

DS1035 TEST CIRCUIT Figure 2



7

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=+5V ± 5%)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.75	5.00	5.25	V
Active Current	I_{CC}	V_{CC}=5.25V Period=1µs			35	mA
High Level Input Voltage	V_{IH}		2.2		V_{CC}+0.5	V
Low Level Input Voltage	V_{IL}		–0.5		0.8	V
Input Leakage	I_L	$0V \le V_I \le V_{CC}$	–1.0		1.0	µA
High Level Output Current	I_{OH}	V_{CC}=4.75V V_{OH}=4V			–1.0	mA
Low Level Output Current	I_{OL}	V_{CC}=4.75V V_{OL}=0.5V	12			mA

AC ELECTRICAL CHARACTERISTICS

(+25°C; V_{CC}=5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Period	t_{PERIOD}	2 (t_{WI})			ns	3
Input Pulse Width	t_{WI}	100% of Tap Delay			ns	3
Input–to–Tap Output Delay	t_{PLH}, t_{PHL}		Table 1		ns	
Output Rise or Fall Time	t_{OR}, t_{OF}		2.0	2.5	ns	
Power–up Time	t_{PU}			100	ms	

CAPACITANCE

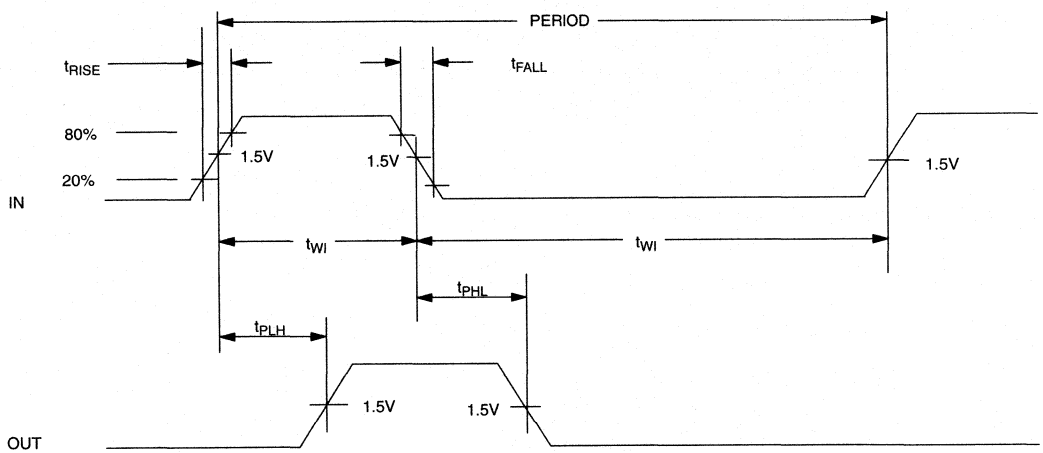
(T_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			10	pF	

TEST CONDITIONS

Ambient Temperature: 25°C ± 3°C
Supply Voltage (V_{CC}): 5.0V ± 0.1V
Input Pulse:
High: 3.0V ± 0.1V
Low: 0.0V ± 0.1V
Source Impedance: 50Ω Max.
Rise and Fall Time: 3.0 ns Max. – Measured between 0.6V and 2.4V.
Pulse Width: 500 ns
Pulse Period: 1 µs
Output Load Capacitance: 15 pF
Output: Each output is loaded with the equivalent of one 74F04 input gate.
Data is measured at the 1.5V level on the rising and falling edges.
Note: The above conditions are for test only and do not restrict the devices under other data sheet conditions.

TIMING DIAGRAM



NOTES:

1. All voltages are referenced to ground.
2. @ V_{CC}=5 volts and 25°C, delay accuracy on both the rising and falling edges within tolerances given in Table 1.
3. Pulse width and duty cycle specifications may be exceeded, however, accuracy will be application sensitive with respect to de–coupling, layout, etc.

TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5 volt point on the leading edge and the 1.5 volt point on the trailing edge or the 1.5 volt point on the trailing edge and the 1.5 volt point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge on the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5 volt point on the leading edge of the input pulse and the 1.5 volt point on the leading edge of the output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5 volt point on the falling edge of the input pulse and the 1.5 volt point on the falling edge of the output pulse.

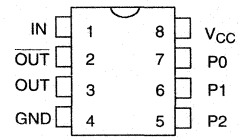
DALLAS SEMICONDUCTOR

DS1040
Programmable One-Shot Pulse Generator

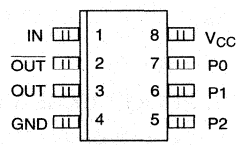
FEATURES

- All-silicon pulse width generator
- Five programmable widths
- Equal and unequal increments available
- Pulse widths from 5 ns to 500 ns
- Widths are stable and precise
- Rising edge-triggered
- Inverted and non-inverted outputs
- Width tolerance ±5% or ±2 ns, whichever is greater
- Economical
- Auto-insertable, low profile
- Low-power CMOS
- TTL/CMOS-compatible
- Vapor phase, IR and wave solderable
- Custom widths available
- Fast turn prototypes
- Extended temperature range available

PIN ASSIGNMENT



DS1040M 8-PIN DIP (300 MIL)
See Mech. Drawings Section



DS1040Z 8-PIN SOIC (150 MIL)
See Mech. Drawings Section

PIN DESCRIPTION

IN	–	Trigger Input
P0-P2	–	Programming Pins
GND	–	Ground
OUT	–	Pulse Output
$\overline{OUT}$	–	Inverted Pulse Output
V_{CC}	–	+5V

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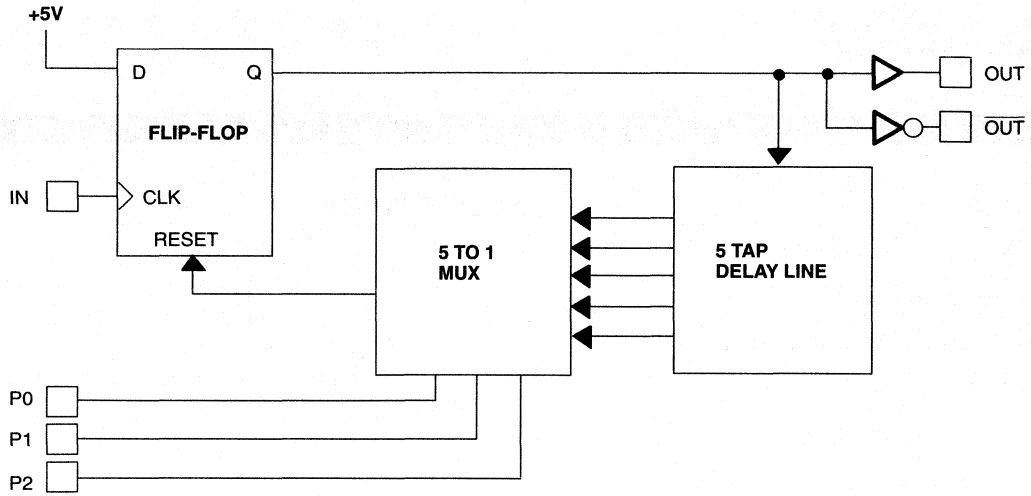
DESCRIPTION

The DS1040 Pulse Generator is a user-programmable one-shot with a choice of five precise pulse widths. Maximum widths range from 50 ns to 500 ns; increments range from 2.5 ns to 100 ns. For maximum flexibility in applications such as magneto-optical read/write disk laser power control, varieties are offered with equal and unequal increments. The DS1040 is offered in standard 8-pin DIPs and 8-pin mini-SOICs. Low cost and superior reliability over hybrid technology are achieved by the combination of a 100% CMOS silicon design and industry standard packaging. The DS1040 series of pulse generators provide a nominal width accuracy of ±5% or ±2 ns, whichever is greater. In response to the rising edge of the input (trigger) pulse, the DS1040 produces an output pulse with a width determined by the logic states of the three parallel programming pins. For convenience, both inverting and non-inverting outputs are supplied. The intrinsic delay between the trigger pulse and the output pulse is no more than 10 ns. Each output is capable of driving up to five 74LS loads.

Dallas Semiconductor can customize standard products to meet special needs. For special request and rapid delivery, call (214) 450-5348.

LOGIC DIAGRAM Figure 1



PULSE WIDTH VS. PROGRAMMED VALUE Table 1

	PROGRAMMING PINS	MAX WIDTH	MIN WIDTH →				MAX WIDTH	MAX WIDTH	MAX WIDTH
	MSB P2	0	0	0	0	1	1	1	1
	P1	0	0	1	1	0	0	1	1
	LSB P0	0	1	0	1	0	1	0	1
PART NUMBER									
DS1040-75		75	15	30	45	60	75	75	75
DS1040-100		100	20	40	60	80	100	100	100
DS1040-150		150	30	60	90	120	150	150	150
DS1040-200		200	40	80	120	160	200	200	200
DS1040-250		250	50	100	150	200	250	250	250
DS1040-500		500	100	200	300	400	500	500	500
DS1040-B50		50	30	35	40	45	50	50	50
DS1040-D60		60	20	30	40	50	60	60	60
DS1040-A15		15	5	7.5	10	12.5	15	15	15
DS1040-A20		20	10	12.5	15	17.5	20	20	20
DS1040-A32		32.5	22.5	25	27.5	30	32.5	32.5	32.5
DS1040-B40		40	20	25	30	35	40	40	40
DS1040-D70		70	30	40	50	60	70	70	70

All times in nanoseconds.
Custom pulse widths available.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5.0V ± 5%)

PARAMETER	SYMBOL	TEST	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC} + 0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0.0 \le V_I \le V_{CC}$	-1.0		1.0	mA	
Active Current	I_{CC}	V_{CC} = Max; Period = Min		35	75	mA	2,6
High Level Output Current	I_{OH}	V_{CC} = Min V_{OH} = 4			-1	mA	
Low Level Output Current	I_{OL}	V_{CC} = Min V_{OL} = 0.5	8			mA	

AC ELECTRICAL CHARACTERISTICS

(T_A = 25°C; V_{CC} = 5.0V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Programming Setup	t_{PS}	5			ns	
Programming Hold	t_{PH}	0			ns	
Input Pulse Width at Logic 1	t_{WIH}	5			ns	
Input Pulse Width at Logic 0	t_{WIL}	5			ns	
Intrinsic Delay	t_D	0	5	10	ns	
Output Pulse Width	t_{WO}		Table 1		ns	3,4,5,7
Power-up Time	t_{PU}			100	ms	
Period	Period	t_{WO} + 50			ns	

CAPACITANCE

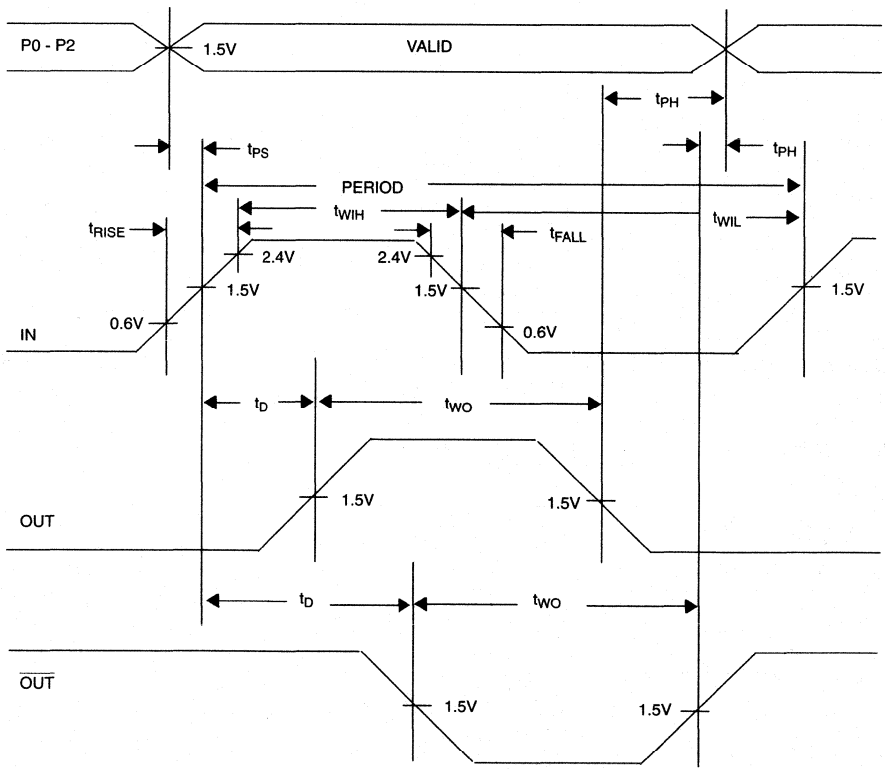
(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	

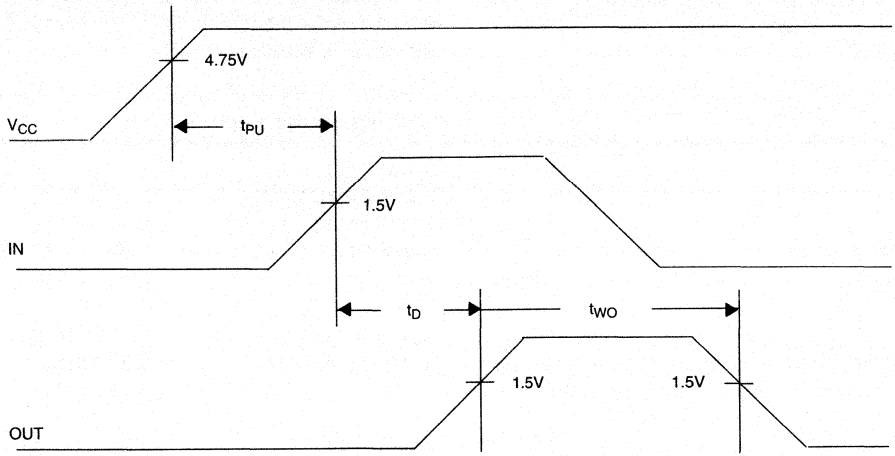
NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open, minimum period.
3. V_{CC} = 5V @ 25°C. Width accurate to within ±2 ns or 5%.
4. Temperature variations between 0°C and 70°C may increase or decrease width by an additional ±1 ns or ±3%, whichever is greater.
5. For DS1040 pulse generators with maximum widths less than 50ns, temperature variations between 0°C and 70°C may increase or decrease width by ±1 ns or ±9%, whichever is greater.
6. I_{CC} is a function of frequency and maximum width. Only a pulse generator operating with 40 ns period and V_{CC}=5.25V will have an I_{CC}=75 mA. For example, a -100 will never exceed 30 mA, etc.
7. See "Test Conditions" sections at the end of this data sheet.

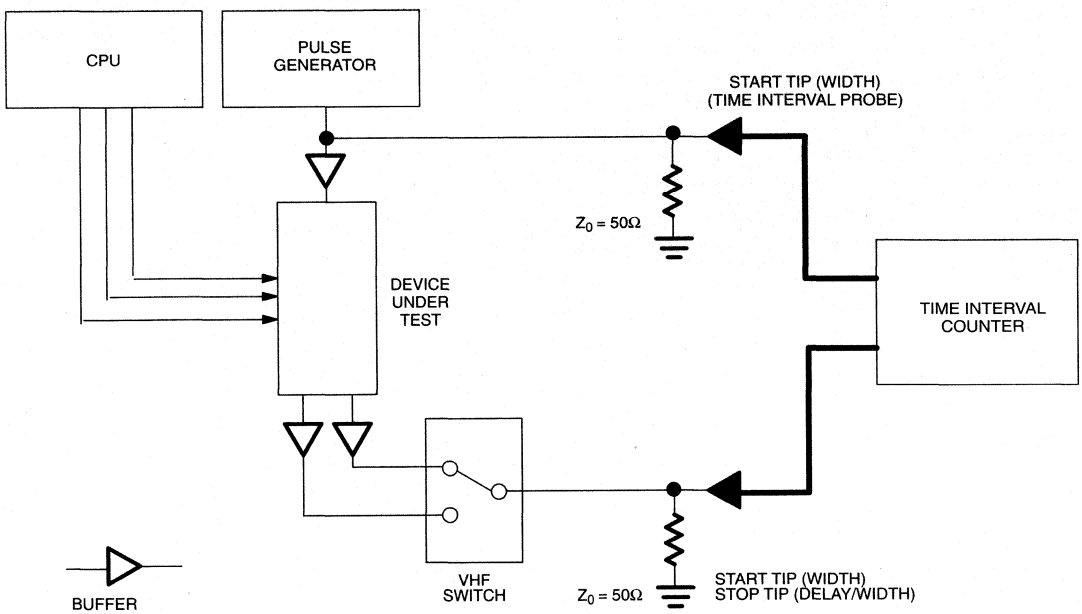
TIMING DIAGRAM Figure 2



POWER–UP TIMING DIAGRAM Figure 3



TEST CIRCUIT Figure 4



7

TERMINOLOGY

Period: The time elapsed between the leading edge of the first trigger pulse and the leading edge of the following trigger pulse.

$t_{WIH, WIL, WO}$ (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_D (Intrinsic Delay): The elapsed time between the 1.5 point on the leading edge of the input trigger pulse and the 1.5V point on the leading edge of output pulse.

t_{PU} (Power-up Time): After V_{CC} is valid, the time required before timing specifications is within tolerance.

TEST SETUP DESCRIPTION

Figure 4 illustrates the hardware configuration used for measuring the timing parameters on the DS1040. The input waveform is produced by a precision pulse generator under software control. The intrinsic delay is measured by a time interval counter (20 ps resolution) connected between the input and each output. Outputs are selected and connected to the counter by a VHF switch control unit. Width measurements are made by directing both the start and stop functions of the counter to the same output. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

Input:

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V Low = 0.0V ± 0.1
Source Impedance:	50 ohm max.
Rise and Fall Time:	3.0 ns max. (measured between 0.6V and 2.4)
Pulse Width:	500 ns (1 µs for -500)
Period:	1 µs (2 µs for -500)

Output:

The output is loaded with a 74F04. Delay is measured at the 1.5V level on the rising and falling edge.

Note:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

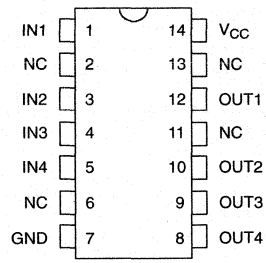
DALLAS SEMICONDUCTOR

DS1044
4–in–1 High–Speed Silicon Delay Line

FEATURES

- All–silicon timing circuit
- Four independent buffered delays
- Initial delay tolerance ±1.5 ns
- Stable and precise over temperature and voltage
- Leading and trailing edge precision preserves the input symmetry
- Standard 14–pin DIP, 14–pin SOIC (150 mil)
- Vapor phasing, IR and wave solderable
- Available in Tape and Reel

PIN ASSIGNMENT



DS1044 14–PIN DIP
DS1044R 14–PIN SOIC (150 MIL)
See Mech. Drawings Section

PIN DESCRIPTION

IN1–IN4	– Input Signals
OUT1–OUT4	– Output Signals
NC	– No Connection
V_{CC}	– +5 Volt Supply
GND	– Ground

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DESCRIPTION

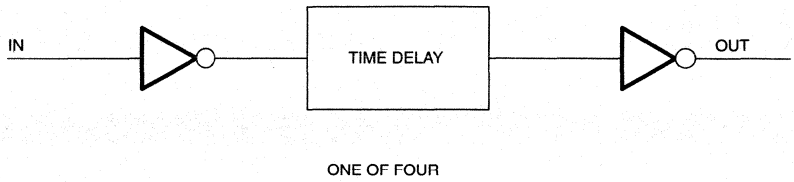
The DS1044 series is a 4–in–1 version of the low–power, +5 Volt, high speed, DS1035.

The DS1044 series of delay lines have four independent logic buffered delays in a single package. The device is Dallas Semiconductor's fastest 4–in–1 delay line. It is available in a standard 14–pin DIP and 14–pin SOIC.

The device features precise leading and trailing edge accuracies. It has the inherent reliability of an all–silicon delay line solution. The DS1044's nominal tolerance is ±1.5 ns and an additional tolerance over temperature and voltage of ±1.0 ns for the faster delays. Each output is capable of driving up to 10 LS loads.

Standard delay values are indicated in Table 1. Customers may contact Dallas Semiconductor at 214–450–5348 for further information.

LOGIC DIAGRAM Figure 1



PART NUMBER DELAY TABLE (t_{PLH}, t_{PHL}) Table 1

PART NUMBER	DELAY PER OUTPUT (ns)	INITIAL TOLERANCE	TOLERANCE OVER (temp and voltage)
DS1044–5	5	±1.5 ns	±1.0 ns
DS1044–6	6	±1.5 ns	±1.0 ns
DS1044–7	7	±1.5 ns	±1.0 ns
DS1044–8	8	±1.5 ns	±1.0 ns
DS1044–10	10	±1.5 ns	±1.0 ns
DS1044–12	12	±1.5 ns	±1.0 ns
DS1044–14	14	±1.5 ns	±1.5 ns
DS1044–18	18	±1.5 ns	±1.5 ns
DS1044–20	20	±1.5 ns	±1.5 ns
DS1044–25	25	±2.0 ns	±1.5 ns

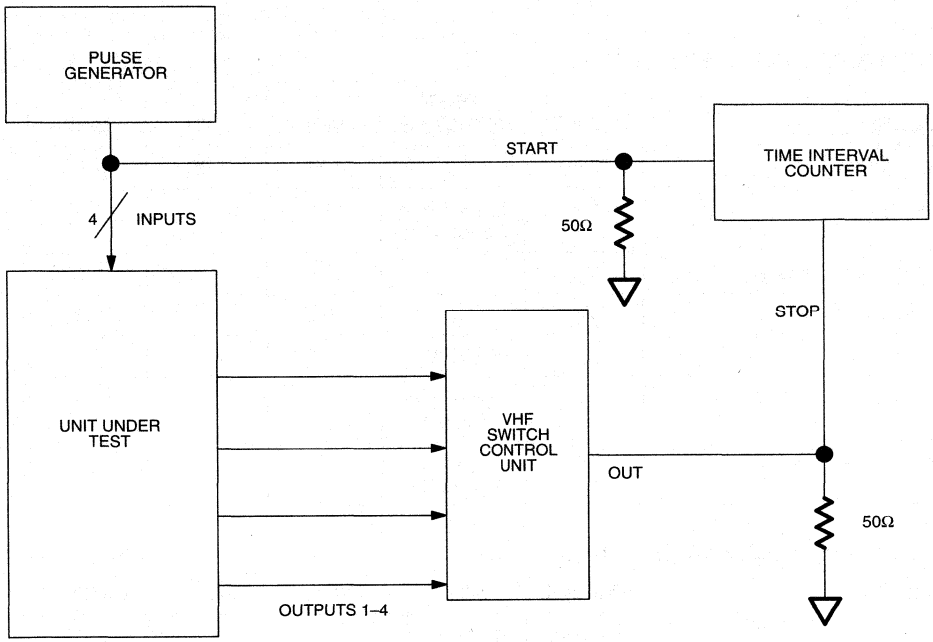
NOTES:

1. Nominal conditions are +25°C and V_{CC}=+5.0 volts.
2. Temperature range of 0°C to 70°C and voltage range of 4.75 volts to 5.25 volts.
3. Delay accuracy are for both leading and trailing edges.

TEST SETUP DESCRIPTION

Figure 2 illustrates the hardware configuration used for measuring the timing parameters of the DS1044. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected to the output. The DS1044 output taps are selected and connected to the interval counter by a VHF switch control unit. All measurements are fully automated with each instrument controlled by the computer over an IEEE 488 bus.

DS1044 TEST CIRCUIT Figure 2



7

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=+5V ± 5%)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.75	5.00	5.25	V
Active Current	I_{CC}	V_{CC}=5.25V Period=1µs			45	mA
High Level Input Voltage	V_{IH}		2.2		V_{CC}+0.5	V
Low Level Input Voltage	V_{IL}		–0.5		0.8	V
Input Leakage	I_L	$0V \le V_I \le V_{CC}$	–1.0		1.0	µA
High Level Output Current	I_{OH}	V_{CC}=4.75V V_{OH}=4V			–1.0	mA
Low Level Output Current	I_{OL}	V_{CC}=4.75V V_{OL}=0.5V	12			mA

AC ELECTRICAL CHARACTERISTICS

(+25°C; V_{CC}=5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Period	t_{PERIOD}	2 (t_{WI})			ns	3
Input Pulse Width	t_{WI}	100% of Tap Delay			ns	3
Input–to–Tap Output Delay	t_{PLH}, t_{PHL}		Table 1		ns	
Output Rise or Fall Time	t_{OR}, t_{OF}		2.0	2.5	ns	
Power–up Time	t_{PU}			100	ms	

CAPACITANCE

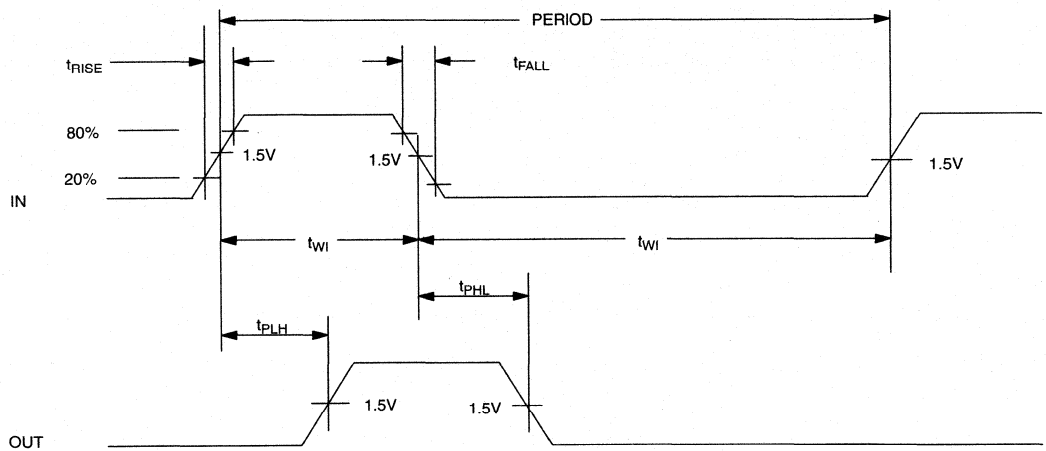
(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			10	pF	

TEST CONDITIONS

Ambient Temperature: 25°C ± 3°C
Supply Voltage (V_{CC}): 5.0V ± 0.1V
Input Pulse:
High: 3.0V ± 0.1V
Low: 0.0V ± 0.1V
Source Impedance: 50Ω Max.
Rise and Fall Time: 3.0 ns Max. – Measured between 0.6V and 2.4V.
Pulse Width: 500 ns
Pulse Period: 1 µs
Output Load Capacitance: 15 pF
Output: Each output is loaded with the equivalent of one 74F04 input gate.
Data is measured at the 1.5V level on the rising and falling edges.
Note: The above conditions are for test only and do not restrict the devices under other data sheet conditions.

TIMING DIAGRAM



NOTES:

1. All voltages are referenced to ground.
2. @ V_{CC}=5 volts and 25°C, delay accuracy on both the rising and falling edges within tolerances given in Table 1.
3. Pulse width and duty cycle specifications may be exceeded, however, accuracy will be application sensitive with respect to de–coupling, layout, etc.

TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5 volt point on the leading edge and the 1.5 volt point on the trailing edge or the 1.5 volt point on the trailing edge and the 1.5 volt point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge on the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5 volt point on the leading edge of the input pulse and the 1.5 volt point on the leading edge of the output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5 volt point on the falling edge of the input pulse and the 1.5 volt point on the falling edge of the output pulse.

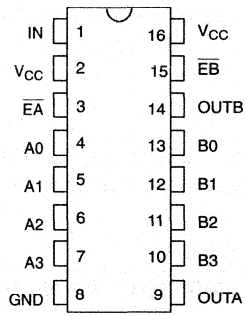
DALLAS SEMICONDUCTOR

DS1045
4-Bit Dual Programmable Delay Line

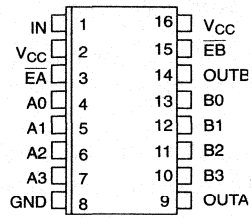
FEATURES

- All–silicon time delay
- Two programmable outputs from a single input produce output–to–output delays between 9 and 84 ns depending on device type
- Programmable via four input pins
- Programmable increments of 2 to 5 ns with a minimum of 9 ns and a maximum of 84 ns
- Output pulse is a reproduction of input pulse after delay with both leading and trailing edge accuracy
- Standard 16–pin DIP or surface mount 16–pin SOIC
- Auto-insertable
- Low–power CMOS design is TTL–compatible

PIN ASSIGNMENT



DS1045 16-PIN DIP
See Mech. Drawings Section



DS1045S 16-PIN SOIC (300 MIL)
See Mech. Drawings Section

PIN DESCRIPTION

IN	-	Delay Line Input
OUTA, OUTB	-	Delay Line Outputs
A0-A3	-	Parallel Program Inputs for OUT1
B0-B3	-	Parallel Program Inputs for OUT2
$\overline{EA}$, $\overline{EB}$	-	Enable A and B Inputs
V_{CC}	-	+5 Volt Input
GND	-	Ground

7

DESCRIPTION

The DS1045 is a programmable silicon delay line having one input and two 4-bit programmable delay outputs. Each 4-bit programmable output offers the user 16 possible delay values to select from, starting with a minimum inherent DS1045 delay of 9 ns and a maximum achievable delay in the standard DS1045 family of 84 ns. The standard DS1045 product line provides the user with four devices having uniform delay increments of 2, 3, 4, and 5 ns depending on the device. Table 1 presents standard device family and delay capability. Additionally, custom delay increments are available for special order through Dallas Semiconductor.

The DS1045 is TTL and CMOS-compatible and capable of driving ten 74LS-type loads. The output produced by the DS1045 is both rising and falling edge precise. The DS1045 programmable silicon delay line has been designed as a reliable, economic alternative to hybrid programmable delay lines. It is offered in a standard 16-pin auto-insertable DIP and a space-saving surface mount 16-pin SOIC package.

PARALLEL PROGRAMMING

Parallel programming of the DS1045 is accomplished via the set of parallel inputs A0–A3 and B0–B3 as shown in Figure 1. Parallel input A0–A3 and B0–B3 accept TTL levels and are used to set the delay values of outputs OUTA and OUTB, respectively. Sixteen possible delay values between the minimum 9 ns delay and the maximum delay of the DS1045-x device version can be selected using the parallel programming inputs A0–A3 or B0–B3 (see Table 2, "Delay vs. Programmed Input"). For example, the DS1045-3 outputs OUTA or OUTB and can be programmed to produce 16 possible delays between the 9 ns (minimum) and the 54 ns (maximum) in 3 ns increment levels.

For applications that do not require frequent reprogramming, the parallel inputs can be set using fixed logic levels, as would be produced by jumpers, DIP switches, or TTL levels as produced by computer systems. Maximum flexibility in parallel programming can be achieved when inputs are set by computer-generated data. By using the enable input pins for each respective programmed output and observing the input setup (t_{DSE}) and hold time (t_{DHE}) requirements, data can be latched on an 8-bit bus. If the enable pins, $\overline{EA}$ and $\overline{EB}$, are not used to latch data, they should be set to a logic level 1. After each change in the programmed delay value, a settling time (t_{EDV}) or (t_{PDV}) is required before the delayed output signal is reliably produced. Since the DS1045 is a CMOS design, undefined input pins should be connected to well defined logic levels and not left floating.

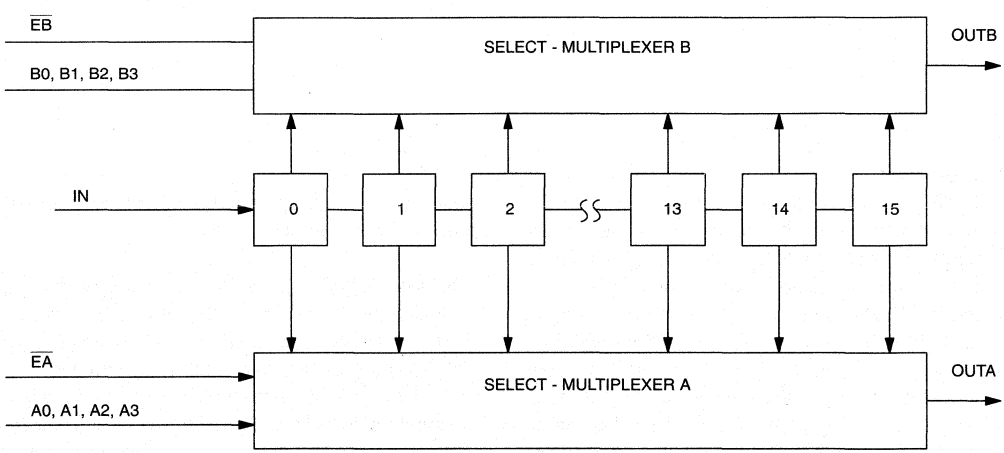
PART NUMBER TABLE Table 1

PART NUMBER	STEP ZERO DELAY	MAX DELAY TIME	MAX DELAY TOLERANCE
DS1045-2	9 ± 1 ns	39 ns	±1.8 ns
DS1045-3	9 ± 1 ns	54 ns	±2.5 ns
DS1045-4	9 ± 1 ns	69 ns	±3.3 ns
DS1045-5	9 ± 1 ns	84 ns	±4.1 ns

NOTE:

Additional delay step times are available from Dallas Semiconductor by special order. Consult factory for availability.

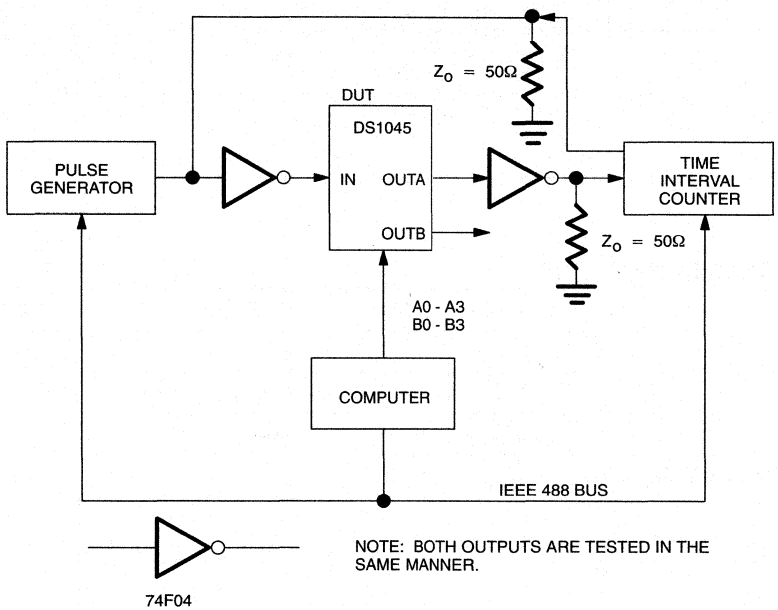
BLOCK DIAGRAM Figure 1



DELAY VS. PROGRAMMED VALUE Table 2

PART NUMBER	OUTPUT DELAY VALUE															
DS1045–2	9	11	13	15	17	19	21	23	25	27	29	31	33	35	37	39
DS1045–3	9	12	15	18	21	24	27	30	33	36	39	42	45	48	51	54
DS1045–4	9	13	17	21	25	29	33	37	41	45	49	53	57	61	65	69
DS1045–5	9	14	19	24	29	34	39	44	49	54	59	64	69	74	79	84
	PROGRAM VALUES FOR EACH DELAY VALUE															
A0 OR B0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
A1 OR B1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
A2 OR B2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
A3 OR B3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

DS1045 TEST CIRCUIT Figure 2



TEST SETUP DESCRIPTION

Figure 2 illustrates the hardware configuration used for measuring the timing parameters of the DS1045. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected to the output. The DS1045 parallel inputs are controlled by an interface to a central computer. All measurements are fully automated with each instrument controlled by the computer over an IEEE 488 bus.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	250°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.0	5.25	V	1
Input Logic 1	V_{IH}		2.2		V_{CC} + 0.5	V	1
Input Logic 0	V_{IL}		-0.5		0.8	µA	1
Input Leakage	I_I	$0 \le V_I \le V_{CC}$	-1.0		1.0	mA	
Active Current	I_{CC}	V_{CC}=5.25V PERIOD=1 µs			35.0	mA	
Logic 1 Output Current	I_{OH}	V_{CC} = 4.75V V_{OH} = 4.0V			-1.0	mA	
Logic 0 Output Current	I_{OL}	V_{CC} = 4.75V V_{OL} = 0.5V	8			mA	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Period	t_{PERIOD}	4 x t_{WI}			ns	
Pulse Width	t_{WI}	100% of output delay size				
Input to Output Delay	t_{PLH}, t_{PHL}	Table 1				2
Parallel Input Change to Delay Invalid	t_{PDX}	0			ns	
Parallel Input Valid to Delay Valid	t_{PDV}		10		ns	
Enable Width	t_{EW}	15			ns	
Data Setup to Enable	t_{DSE}	10			ns	
Data Hold from Enable	t_{DHE}	0			ns	
Enable to Delay Invalid	t_{EDX}		5		ns	
Enable to Delay Valid	t_{EDV}		15		ns	

CAPACITANCE

(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			10	pF	

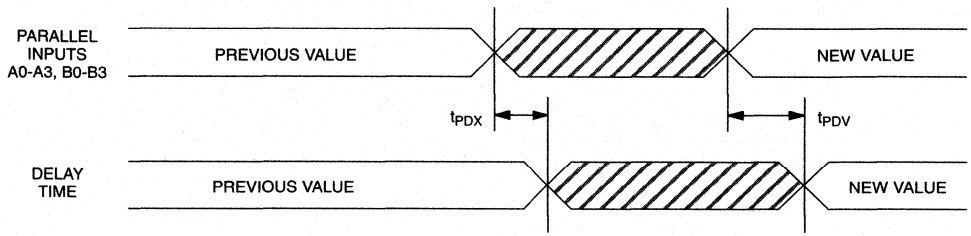
TEST CONDITIONS

T_A = 25°C ± 3°C
V_{CC} = 5.0V ± 0.1V
Input Pulse = 3.0V high to 0.0V low ± 0.1V
Input Source Impedance = 50 ohms maximum
Rise and fall times = 3.0 ns max. between 0.6V and 2.4V
Pulse Width = 250 ns
Period = 500 ns
Output Load = 74F04
Measurement Point = 1.5V on inputs and outputs
Output Load Capacitance = 15 pF

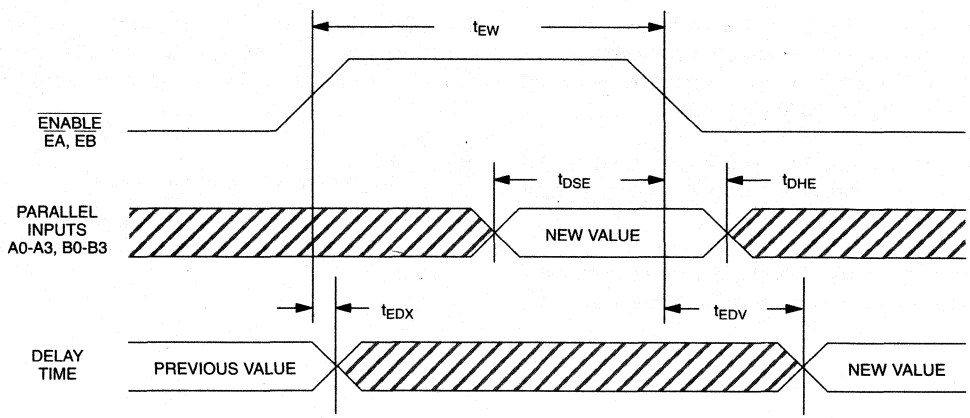
NOTE:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

TIMING DIAGRAM: NON-LATCHED PARALLEL MODE, $\overline{EA}$, $\overline{EB}$ = V_{IH}



TIMING DIAGRAM: LATCHED PARALLEL MODE



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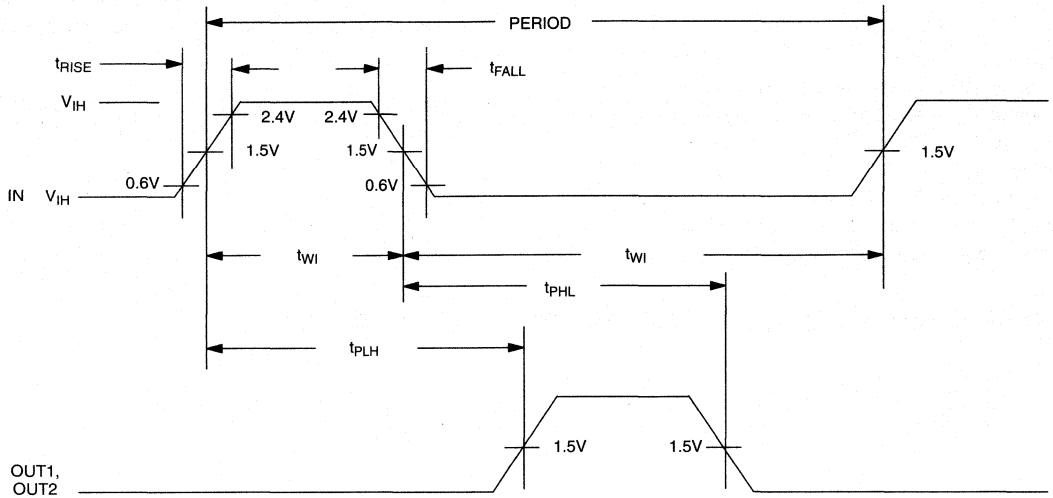
TIMING DIAGRAM: DS1045 INPUTS TO OUTPUTS



TERMINOLOGY

PERIOD: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of the output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of the output pulse.

NOTES:

1. All voltages are referenced to ground.
2. @ V_{CC} = 5V and 25°C. Delay accurate on both rising and falling edges within tolerances given in Table 1.

SYSTEM EXTENSION

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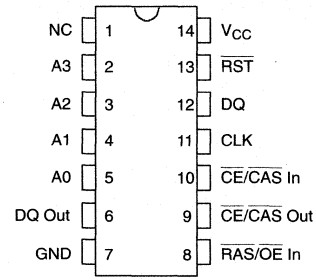
DALLAS SEMICONDUCTOR

DS1206
Phantom Serial Interface Chip

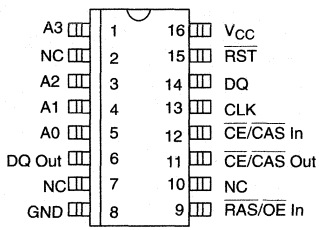
FEATURES

- Minimum expense add-on serial port
- Converts standard bytewide or DRAM memory waveforms into a 3-wire serial port
- Operation is transparent to memory
- Software-generated memory cycles activate serial port and transfer data
- High bandwidth – 1-bit data transfer per two memory cycles
- Intercepts memory signals so that pass-through connections to memory can be maintained
- Controls communications for as many as ten DS1201 Electronic Tags, DS1204U Electronic Keys, DS1207 TimeKeys or DS1290 Eliminators
- Low-power CMOS circuitry
- Optional 16-pin SOIC surface mount package

PIN ASSIGNMENT



14-Pin DIP (300 MIL)
See Mech. Drawings Section



16-Pin SOIC (300 MIL)
See Mech. Drawings Section

PIN DESCRIPTION

NC	–	No Connection
A0–A3	–	Memory Address Bus
DQ Out	–	Data Out To Memory Bus
GND	–	Ground
$\overline{RAS}/\overline{OE}$ In	–	Output Enable or $\overline{RAS}$ input from memory bus
$\overline{CE}/\overline{CAS}$ In	–	Chip enable or $\overline{CAS}$ from memory bus
$\overline{CE}/\overline{CAS}$ Out	–	Chip enable or $\overline{CAS}$ to memory circuit
CLK	–	Clock for Serial Port
DQ	–	Data I/O for Serial Port
$\overline{RST}$	–	Reset for Serial Port
V_{CC}	–	+5 Volts

DESCRIPTION

The DS1206 Phantom Serial Interface Chip is a CMOS circuit which intercepts the standardized memory bus found in computer systems and adapts the bus to a 3-wire serial port. Multiple memory cycles are used as a basis for generating the appropriate signals to control the serial port. A sequence of software-generated memory cycles encodes commands and transfers data with low pin count. The serial port signaling is derived from the memory address bus lines A0 through A3, the $\overline{CE}/\overline{CAS}$ signal and $\overline{RAS}/\overline{OE}$ signal without affecting

address space, thereby maintaining transparency to the memory bus. Communications are established under software control by an address pattern recognition sequence (serial port protocol) which disables a bytewide or DRAM memory via $\overline{CE}/\overline{CAS}$ output. An additional address sequence is required to generate the 3-wire port signals: $\overline{RESET}$ ($\overline{RST}$), Data (DQ), and Clock (CLK). The add-on serial port provides a minimum cost interface to the DS1201, DS1204U, DS1207, DS1223, and DS1290.

OPERATION

The main parts of the DS1206 are shown in the block diagram of Figure 1. Information presented on address inputs is latched into the DS1206 on the falling edge of a strobe signal derived from the logical combination of $\overline{CE}/\overline{CAS}$ In and $\overline{RAS}/\overline{OE}$ In. When redirecting information from a DRAM memory bus, both $\overline{RAS}$ and $\overline{CAS}$ inputs are required and the column addresses are used for signaling.

For a bytewide memory bus, only a $\overline{CE}$ input is required and the $\overline{RAS}/\overline{OE}$ input can be tied low or connected to the memory $\overline{OE}$ input signal. The rising edge of the strobe will cause the address information to be presented for comparison to the 4-bit serial interface protocol and to logic which will generate signals for the serial port. The serial interface protocol is derived from address inputs A0, A1, and A2.

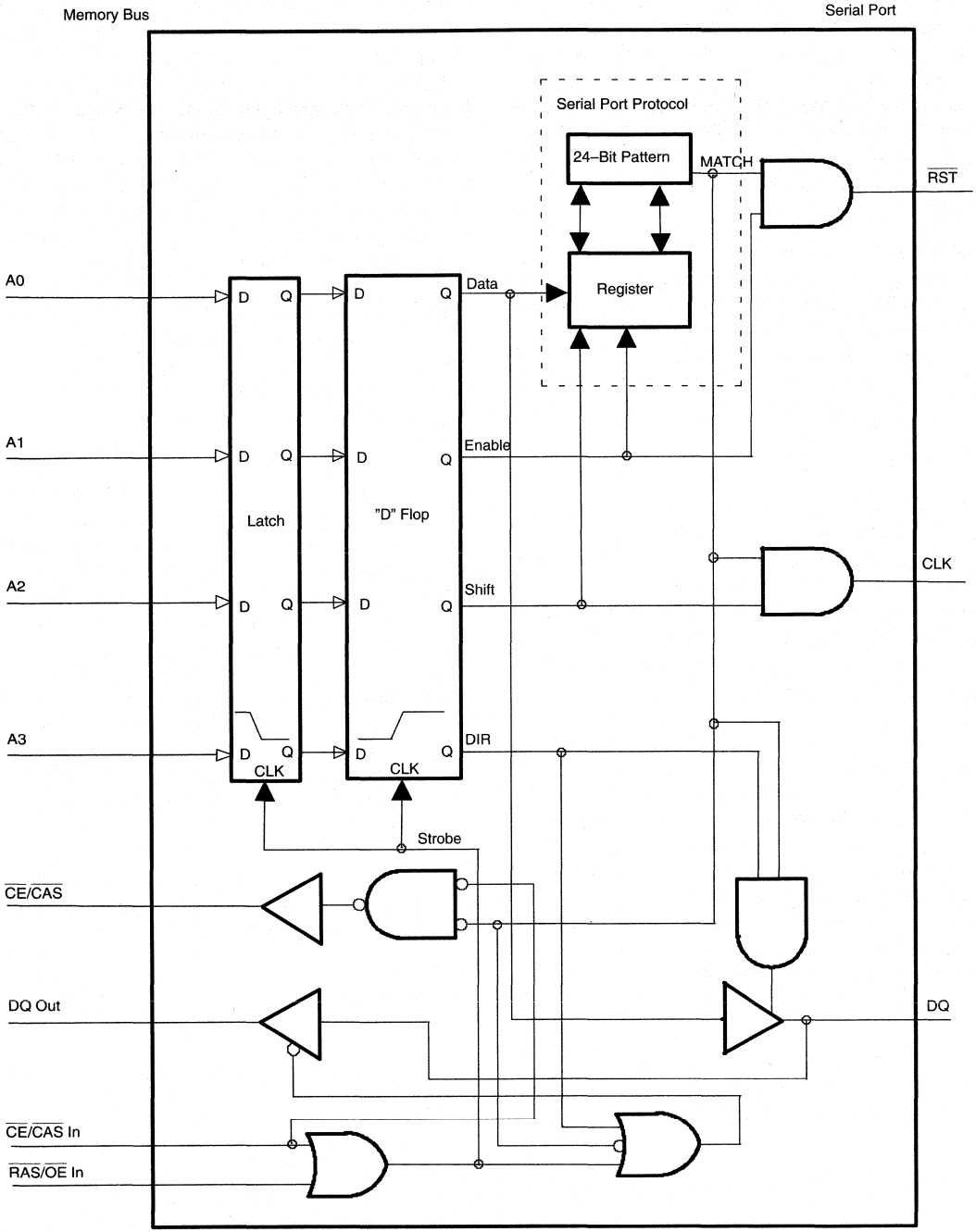
A1 is an enable signal which activates the communications sequence. A0 defines the data which is compared for recognition. A2 is used to clock in information defined by A0. Initially the A1 input must be set high to enable serial interface communications. A1 must remain high during the pattern recognition sequence and subsequent communications with the serial port after the protocol pattern match is established. If the A1 input is set low, all communications are terminated and future access to the serial port is denied.

Data transfer through the serial interface occurs by matching a 24-bit pattern as shown in Figure 2. This pattern is presented to a register on each rising edge of strobe. Data is input for comparison to the serial interface protocol at the end of each memory cycle (see Figure 3). The proper information must be presented on A0 to match the 24-bit pattern while keeping A1 high. Address input A2 is used to generate the shift signal which causes data to enter the 24-bit register for comparison to the 24-bit pattern. Information is loaded one bit at a time on the rising edge of shift. Each shift cycle must be generated from two memory cycles.

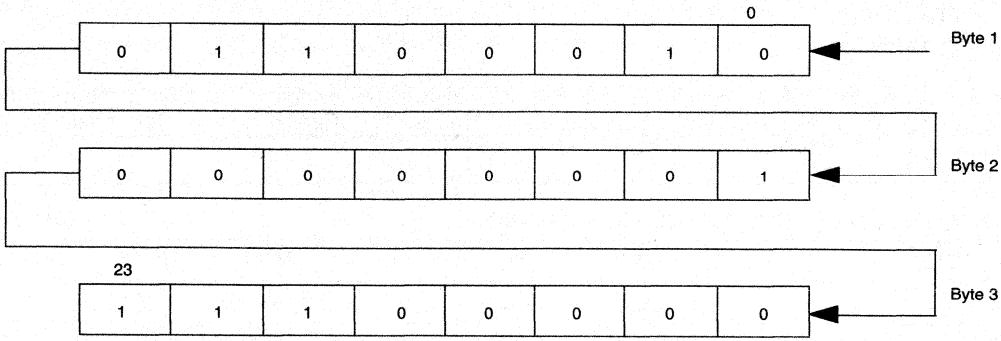
The first memory cycle sets A2 low and establishes the shift clock low. The second memory cycle sets A2 high and causes the transition necessary to shift a bit of data into the 24-bit register. Data on A0 is kept at the correct level for both memory cycles. Address input A3 is used to control the direction of data going to and from the serial port. This input is not used during pattern recognition of the protocol. After the 24-bit pattern has been correctly entered , a match signal is generated. The match signal is logically combined with the enable signal to generate the $\overline{RST}$ signal for the serial port. The match signal is also used to disable Chip Enable to the memory bus and to enable a gate which allows the serial port DQ to drive the DQ out line to the memory bus.

When $\overline{RST}$ is driven high, devices attached to the serial port become active. Subsequent shift signals derived from A2 will now be recognized as the serial port clock. The data signal for the serial bus is derived from A0 conditioned on the level of the direction signal derived from A3. When A3 is set high, data as defined by A0 will be sent out on the serial port DQ. When A3 is set low, devices attached to the serial port can drive the memory bus DQ out line. The data direction bit must be set low when reading data from the serial port DQ.

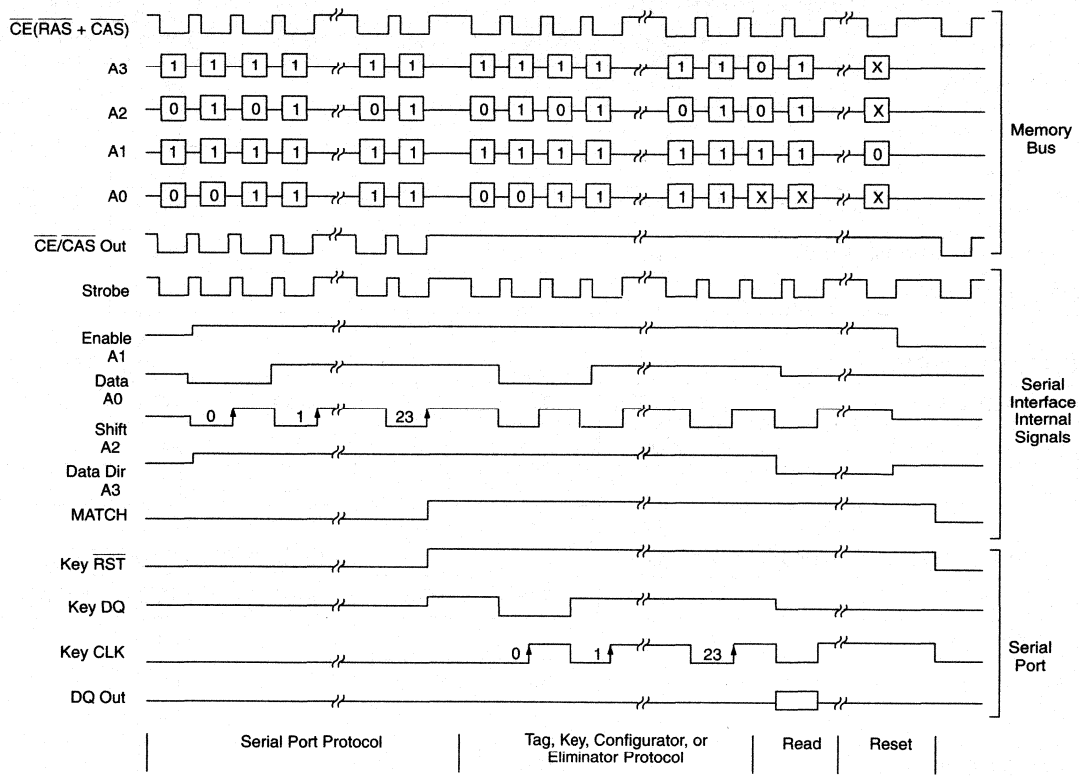
PHANTOM SERIAL INTERFACE BLOCK DIAGRAM Figure 1



SERIAL INTERFACE 24-BIT PROTOCOL Figure 2



PHANTOM SERIAL INTERFACE SIGNALS Figure 3



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ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		V_{CC} + 0.3	V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1
Supply	V_{CC}	4.5	5.0	5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-1		1	µA	
Output Leakage	I_{LO}			1	µA	
Output Current @ 2.4V	I_{OH}	-1			mA	
Output Current @ .4V	I_{OL}	+4			mA	
$\overline{RST}$ Output Current @ 3.8V	I_{OHR}	16			mA	
Supply Current	I_{CC}			6	mA	2

CAPACITANCE

(t_A=25°C)

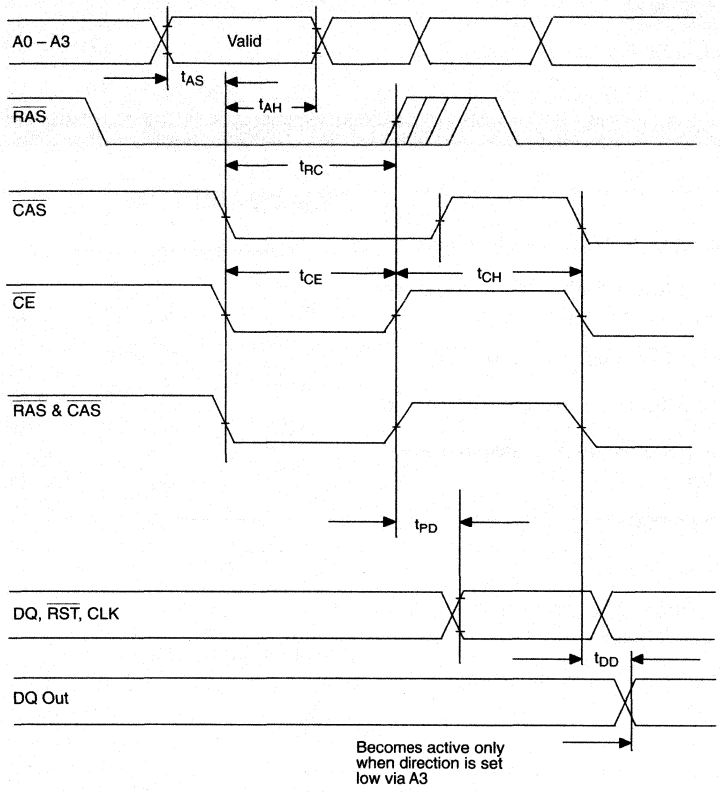
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
$\overline{RAS}$ to $\overline{CAS}$ Overlap	t_{RC}	60			ns	
$\overline{CE}$ Pulse Width	t_{CE}	60			ns	
Key Signals Valid	t_{PD}			60	ns	3
Key Data Out	t_{DD}	10			ns	3
$\overline{CE}$ Inactive	t_{CH}	30			ns	

MEMORY BUS INPUTS



NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open.
3. Measured with a load as shown in Figure 4.

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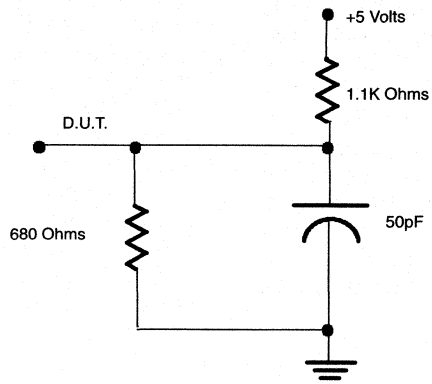
OUTPUT LOAD Figure 4



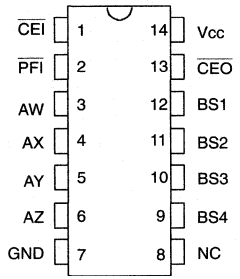
DALLAS SEMICONDUCTOR

DS1222
BankSwitch Chip

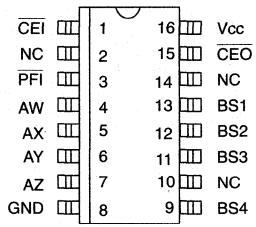
FEATURES

- Provides bank switching for 16 banks of memory
- Bank switching is software-controlled by a pattern recognition sequence on four address inputs
- Automatically sets all 16 banks off on power-up
- Bank switching logic allows only one bank on at a time
- Custom recognition patterns are available to prevent unauthorized access
- Full ±10% operating range
- Low-power CMOS circuitry
- Can be used to expand the address range of microprocessors and decoders
- Optional 16-pin SOIC surface mount package

PIN ASSIGNMENT



DS1222 14-Pin DIP
(300 Mil.)
See Mech. Drawings
Section



DS1222S16-Pin SOIC
(300 Mil.)
See Mech. Drawings
Section

PIN DESCRIPTION

A_W-A_Z	–	Address Inputs
$\overline{CEI}$	–	Chip Enable Input
$\overline{CEO}$	–	Chip Enable Output
NC	–	No Connection
BS1,BS2,	–	Bank Select Outputs
BS3,BS4	–	Bank Select Outputs
$\overline{PFI}$	–	Power Fail Input
V_{CC}	–	+5 Volts
GND	–	Ground

DESCRIPTION

The DS1222 BankSwitch Chip is a CMOS circuit designed to select one of sixteen memory banks under software control. Memory bank switching allows for an increase in memory capacity without additional address lines. Continuous blocks of memory are enabled by selecting the proper memory bank through a pattern recognition sequence on four address inputs. Custom patterns available from Dallas Semiconductor can provide security through uniqueness and prevent unauthorized access. By combining the DS1222 with the DS1212 Nonvolatile Controller x16 Chip, up to 16 banks of static RAMs can be selected.

OPERATION – BANK SWITCHING

Initially, on power-up all four bank select outputs are low and the chip enable output ($\overline{CEO}$) is held high. (Note: the power fail input [$\overline{PFI}$] must be low prior to power-up to assure proper initialization.) Bank switching is achieved by matching a predefined pattern stored within the DS1222 with a 16-bit sequence received on four address inputs. Prior to entering the 16-bit pattern, which sets the bank switch, a read cycle of 1111 on address inputs AW through AZ should be executed to guarantee that pattern entry starts with bit 0. Each set of address inputs is clocked into the DS1222 when $\overline{CEI}$ is driven low. All 16 inputs must be consecutive read cycles. The first eleven cycles must match the exact bit pattern as

shown in Table 1. The last five cycles must match the exact bit pattern as shown for addresses AX, AY, and AZ. However, address line AW defines the bank number to be enabled as per Table 2.

Switching to a selected bank of memory occurs on the rising edge of $\overline{CEI}$ when the last set of bits is input and a match has been established. After bank selection $\overline{CEO}$ always follows $\overline{CEI}$ with a maximum propagation delay of 15 ns. The bank selected is determined by the levels set on Bank Select 1 through Bank Select 4 as per Table 2. These levels are held constant for all memory cycles until a new memory bank is selected.

ADDRESS BIT SEQUENCE Table 1

	BIT SEQUENCE															
ADDRESS INPUTS	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
A_W	1	0	1	0	0	0	1	1	0	1	0	x	x	x	x	x
A_X	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1
A_Y	1	0	1	0	0	0	1	1	0	1	0	1	1	1	0	0
A_Z	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1

X See Table 2

BANK SELECT CONTROL Table 2

Bank	**A_W Bit Sequence**					**Outputs**			
Selected	**11**	**12**	**13**	**14**	**15**	**BS1**	**BS2**	**BS3**	**BS4**
*Banks Off	0	X	X	X	X	Low	Low	Low	Low
Bank 0	1	0	0	0	0	Low	Low	Low	Low
Bank 1	1	0	0	0	1	High	Low	Low	Low
Bank 2	1	0	0	1	0	Low	High	Low	Low
Bank 3	1	0	0	1	1	High	High	Low	Low
Bank 4	1	0	1	0	0	Low	Low	High	Low
Bank 5	1	0	1	0	1	High	Low	High	Low
Bank 6	1	0	1	1	0	Low	High	High	Low
Bank 7	1	0	1	1	1	High	High	High	Low
Bank 8	1	1	0	0	0	Low	Low	Low	High
Bank 9	1	1	0	0	1	High	Low	Low	High
Bank 10	1	1	0	1	0	Low	High	Low	High
Bank 11	1	1	0	1	1	High	High	Low	High
Bank 12	1	1	1	0	0	Low	Low	High	High
Bank 13	1	1	1	0	1	High	Low	High	High
Bank 14	1	1	1	1	0	Low	High	High	High
Bank 15	1	1	1	1	1	High	High	High	High

*$\overline{CEO}$ = V_{IH} independent of $\overline{CEI}$

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ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current	I_{LO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	2
Output Current @ 0.4V	I_{OL}			+4.0	mA	2
Operating Current	I_{CC}			15	mA	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS

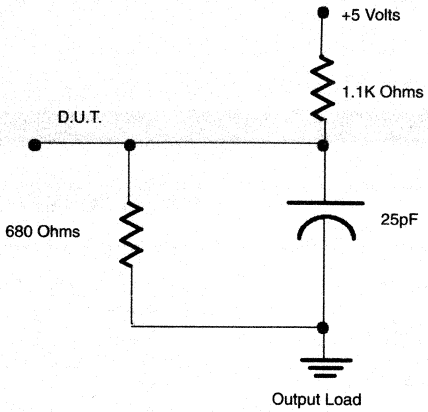
(0°C to 70°C; V_{CC} = 5V± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t_{AS}	5			ns	
Address Hold	t_{AH}	50			ns	
Read Recovery	t_{RR}	40			ns	
Propagation Delay	t_{PD}			15	ns	2
Power Fail Input to First $\overline{CE}$	t_{PF}	50			ns	
Chip Enable Low	t_{CW}	110			ns	

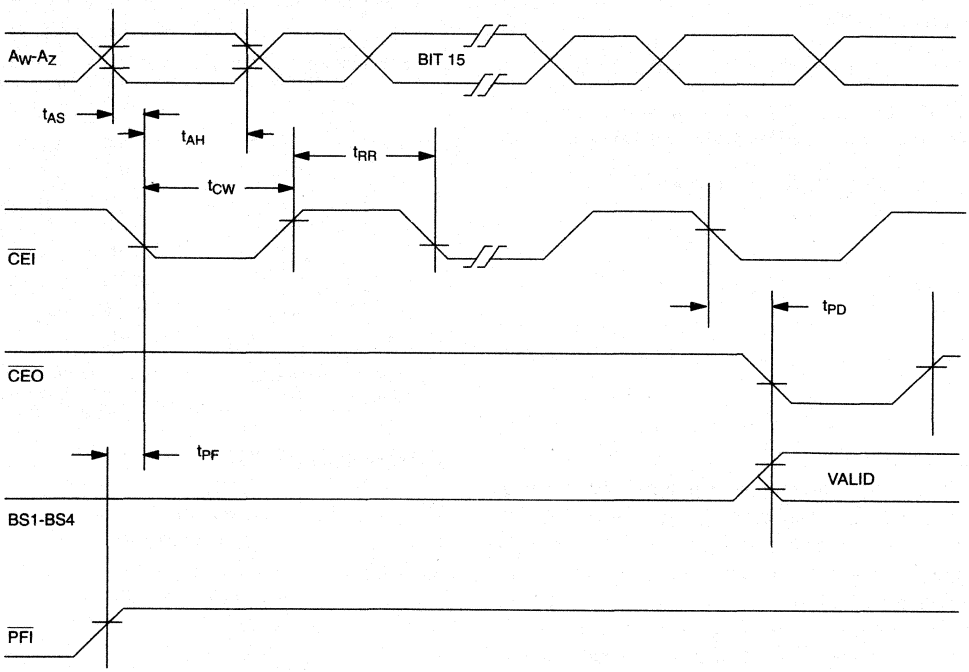
NOTES:

1. All voltages are referenced to ground.
2. Measured with a load as shown in Figure 1.

OUTPUT LOAD Figure 1



TIMING DIAGRAM-ACCESS TO BANK SWITCH



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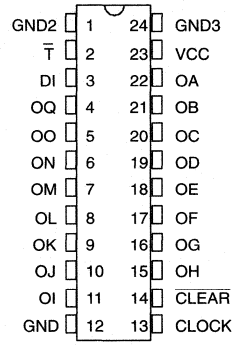
DALLAS SEMICONDUCTOR

DS129x Eliminator

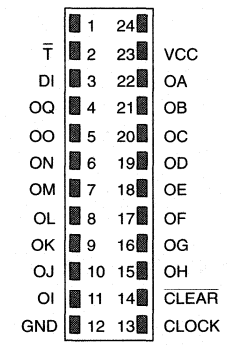
FEATURES

- Replaces 8 or 16 hard-to-get-at manual switches
- Options printed circuit board via software
- Modular expansion by cascading packages
- Set or interrogate with only three signals
- Requires no pull-up resistors
- Links to system bus with the DS1206 Phantom Serial Interface Chip
- Low-power CMOS
- Switch setting changes occur simultaneously
- DS1290 and DS1292 maintain settings in the absence of power; DS1291 and DS1293 are volatile
- Over 10 years of data retention for DS1290 and DS1292

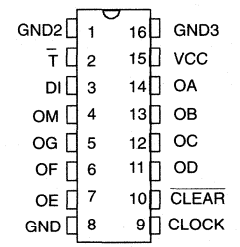
PIN ASSIGNMENT



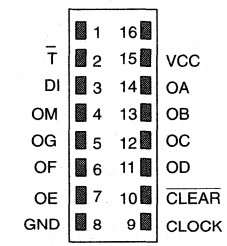
DS1293 24-Pin DIP (300 Mil) See Mech. Drawings Section



DS1292 24-Pin Encapsulated Package (450 Mil) See Mech. Drawings Section



DS1291 16-Pin DIP (300 Mil) See Mech. Drawings Section



DS1290 16-Pin Encapsulated Package (450 Mil) See Mech. Drawings Section

DESCRIPTION

The DS129x Eliminator replaces manual switches used to option printed circuit boards. Up to sixteen output pins can be set to a logic level or interrogated by three signals: clock, data and transfer. The Eliminator can be controlled with software using the DS1206 Phantom Interface to synthesize the clock, data and transfer signals from a system bus. Multiple packages can be strung together for modular expansion. Once programmed, the DS1290 and DS1292 will maintain high or low level outputs, duplicating the effects of a mechanical switch and pull-up resistor. The technical support needed to configure a system is minimized with the Eliminator, Phantom Interface and menu-driven software.

PIN DESCRIPTION

$\overline{T}$	–	Transfer
DI	–	Data Input
O_A–O_Q	–	Switch Outputs
CLOCK	–	Clock Input
$\overline{CLEAR}$	–	All Outputs Set Low
V_{CC}	–	+5 Volts
GND	–	Ground
GND2	–	Missing on DS1292. Must be grounded on DS1293.
GND3	–	Missing on DS1292. Must be grounded on DS1293.

OPERATION

The DS1292/DS1293 Eliminator is a 16-bit shift register that has a clocked serial input, an asynchronous clear, and an output transfer control (see "Block Diagram" in Figure 1). The DS1290/DS1291 Eliminator is an 8-bit shift register that has a clocked serial input, an asynchronous clear, and an output transfer control. Data can be entered into the registers only when the transfer input ($\overline{T}$) is at a high level. While at a high level, the transfer function allows serial entry of data via the data input pin (DI). The outputs 0_Q through 0_B remain in the state that was set prior to $\overline{T}$ being driven to a high level. Output 0_A will change state as new data is entered. This output provides a method of feeding back actual output settings prior to setting the $\overline{T}$ input low (Figure 2). When the $\overline{T}$ input is driven low, new data that has been input into the 16-bit shift register is now locked at outputs 0_Q through 0_A. When the $\overline{T}$ input is low, all clock and data inputs are ignored. Valid data is clocked into the eliminator while $\overline{T}$ is high on the low-to-high transition of the CLOCK input. Data can be changed while the CLOCK input is high or low, but only data meeting the setup requirements will enter the shift register. The $\overline{CLEAR}$ input will always set all outputs to low level regardless of the level of the CLOCK or $\overline{T}$ input.

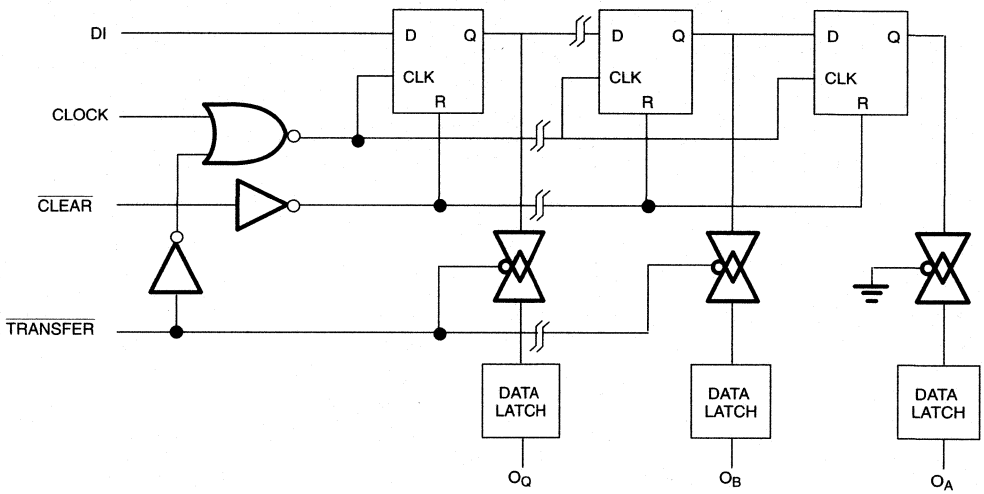
DATA RETENTION MODE

The DS129x Eliminator provides full functional capability when V_{CC} is greater than 4.5 volts and will ignore all inputs when V_{CC} reaches 4.25 volts typical. In this manner, the settings of each register remain intact during power transients. As V_{CC} falls below approximately 3 volts, an internal power switching circuit connects a lithium energy source to the shift register to maintain data. During power-up when V_{CC} rises above approximately 3 volts, the power switching circuit connects external V_{CC} to the shift register and disconnects the lithium energy source. Normal operation can resume after V_{CC} exceeds 4.5 volts for 10 ms minimum. During power transients the 16 outputs will track the level of V_{CC} if set to logic 1 and will remain at ground level if set to Logic 0.

TYPICAL APPLICATION – ELIMINATOR

The DS129x and DS1206 combine to make a programmable nonvolatile DIP switch that can be transparently set in systems without disturbing other operations. Because the switches are nonvolatile, they need only be set once; they will remain in the programmed state indefinitely. The block diagram of Figure 2 shows the Eliminator implemented with the DS1206 Phantom Serial Interface Chip. The DS1206 samples four address lines and the chip enable signal looking for a special pattern for 24 consecutive cycles (see the DS1206 data sheet). When a proper match is found, the address lines and one data line become control and data signals that are used to program and verify the settings of the DS129x. All of the signaling sent to the DS1206 and subsequently to the DS1292 is generated by software-controlled read cycles that have no effect on the rest of system operation. The clear signal can be used to restore a system back to an unconfigured state.

BLOCK DIAGRAM - DS129x Figure 1



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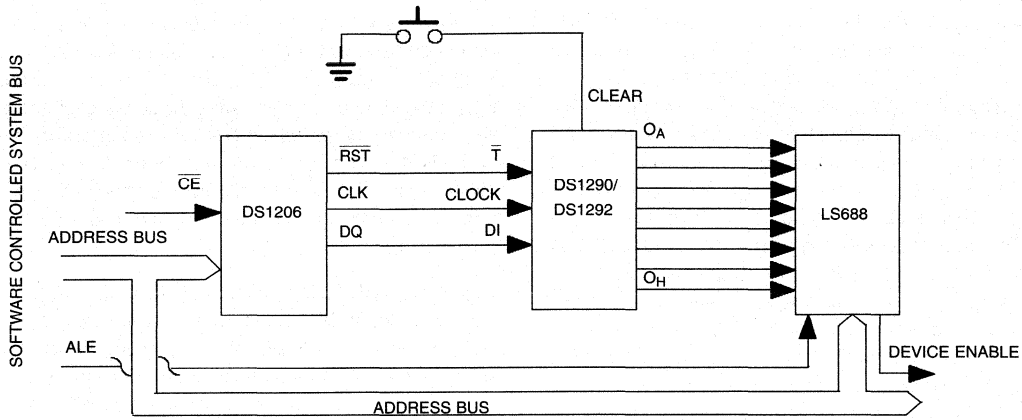
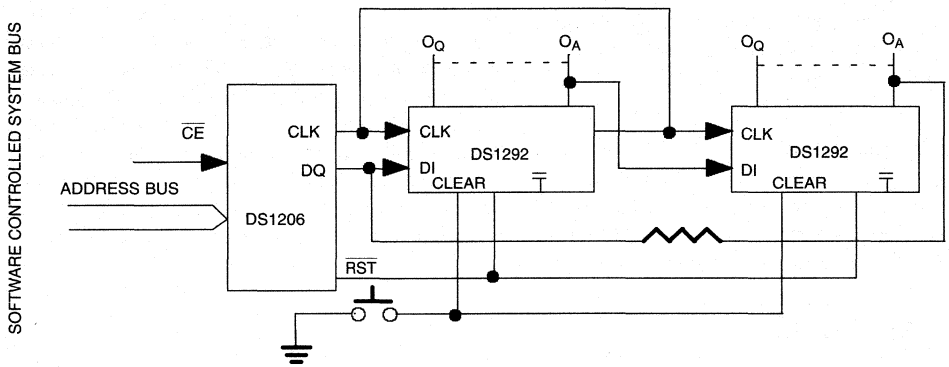
PHANTOM INTERFACE AND ELIMINATOR TYPICAL APPLICATION Figure 2



MODULAR EXPANSION OF THE ELIMINATOR Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}		3	5	mA	
Input Leakage	I_{IL}	-1.0		+1.0	µA	4
Output Leakage	I_{LO}	-1.0		+1.0	µA	
Logic 1 Output @ 2.4V	I_{OH}	-1.0			mA	2
Logic 0 Output @ 0.4V	I_{OL}			4.0	mA	2

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock Frequency	f_{CLOCK}			10	MHz	
Width of Clock Pulse	tw_{CLOCK}	50			ns	3
Width of Clear Pulse	tw_{CLEAR}	50			ns	3
Data Setup Time	t_{SU}	30			ns	3
Data Hold Time	t_H	10			ns	3
Propagation Delay Time High to Low Level Clear to Output	t_{PHLC}			70	ns	3
Propagation Delay Time Low to High Level Clock to Output	t_{PLH}			50	ns	3

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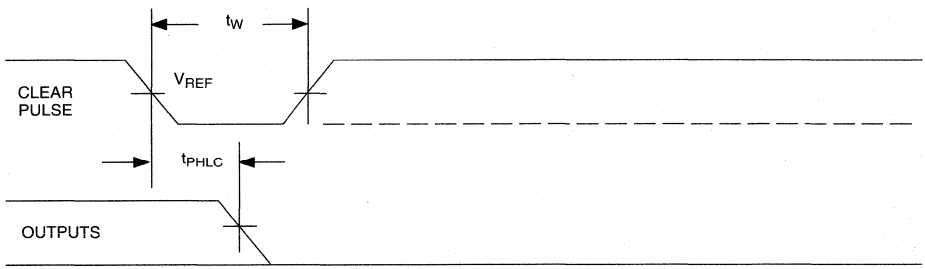
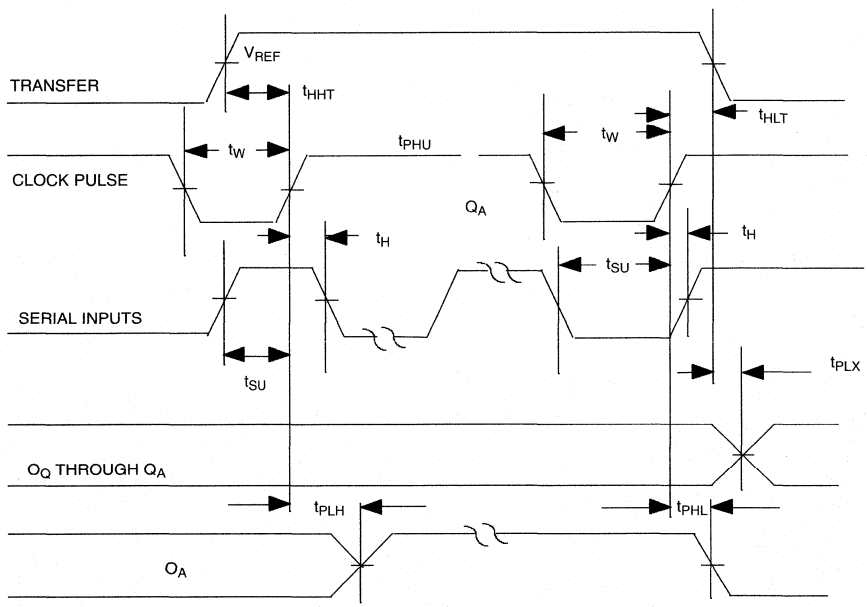
AC ELECTRICAL CHARACTERISTICS (cont'd)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Propagation Delay Time High to Low Level Clock to Output	t_{PHL}			50	ns	3
Recovering on Power-Up	t_{REC}	10			ms	
Propagation Delay Time High to Low Level Transfer to O Out	t_{PLX}			50	ns	3
Transfer High to Clock Input High	t_{HHT}	50			ns	3
Transfer Low from Clock Input High	t_{HLT}	50			ns	3

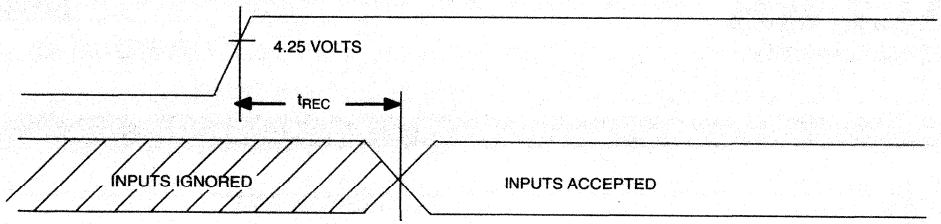
TIMING DIAGRAM: CLEAR CONTROL (3)



TIMING DIAGRAM: TRANSFER DATA (3)



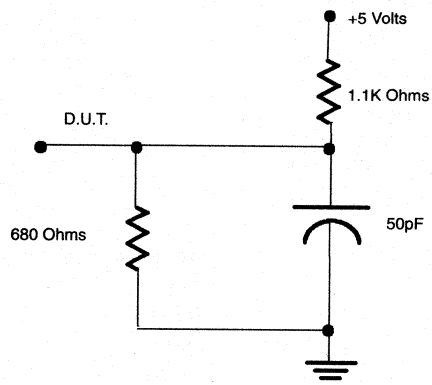
TIMING DIAGRAM: POWER-UP (3)



NOTES:

1. All voltages are referenced to ground.
2. Measured with a load as shown in Figure 4.
3. V_{REF} = 1.5 volts.
4. Clock and transfer inputs have internal pull-down resistors of 20K ohms typical. Clear has an internal pull-up resistor of 20K ohms typical.

OUTPUT LOAD Figure 4



8

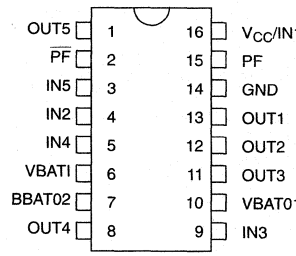
DALLAS SEMICONDUCTOR

DS1336
Afterburner Chip

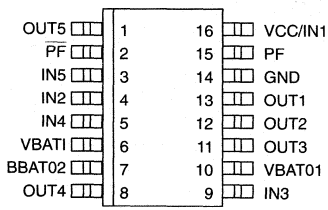
FEATURES

- Provides power switching of up to 1.5 amps at voltages between 3 and 5 volts
- Five separate power switches
- Selectable battery switches for use with battery-backed systems
- Very low on impedance of 0.7Ω
- Battery backup current of 4 mA
- Diode-isolated battery path
- Available in 16-pin DIP or 16-pin SOIC surface mount package
- Low voltage drop battery path
- Connects directly to a variety of Dallas Semiconductor devices adding increased switching capability for large battery backup current applications

PIN ASSIGNMENT



16-Pin DIP (300 mil)
See Mech. Drawings Section



16-Pin SOIC (300 mil)
See Mech. Drawings Section

PIN DESCRIPTION

V_{CC}/IN1	-	+5V Input and Input 1
IN2 - IN5	-	Inputs 2 - 5
OUT1 - 5	-	Outputs 1 - 5
V_{BATIN}	-	External Battery Input
V_{BAT01}	-	Diode Protected Battery Output
V_{BAT02}	-	Low Voltage Drop Battery Output
PF, $\overline{PF}$	-	Power Fail Inputs
GND	-	Ground

DESCRIPTION

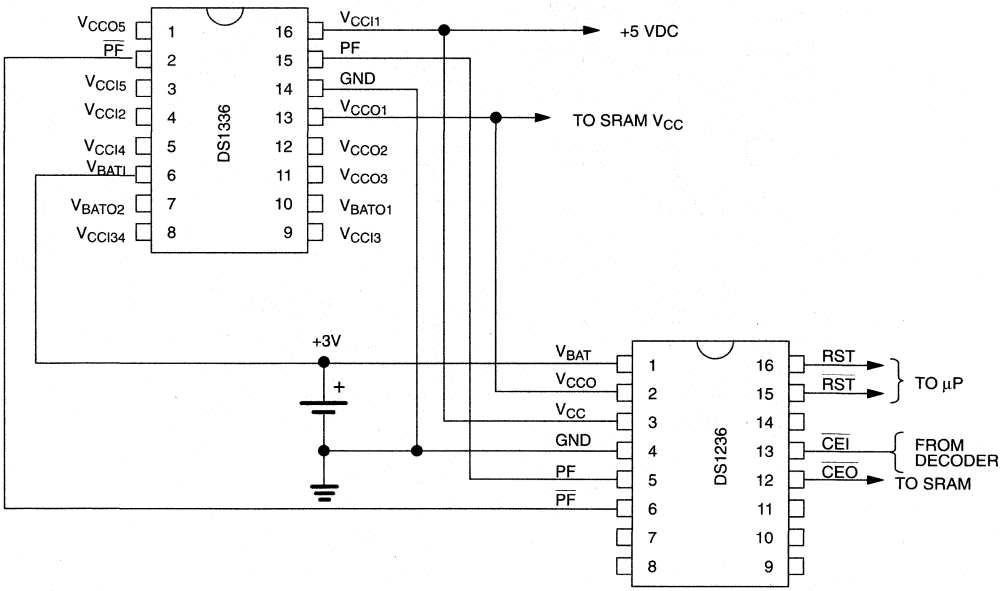
The DS1336 Afterburner Chip is designed to provide power switching between a primary power supply (V_{CC}) and a backup battery power supply (V_{BAT}). Five V_{CC} and two battery paths are provided which can be used individually or in parallel to supply uninterrupted power in applications such as SRAM networks. When used with one of the Dallas power monitoring devices listed in Section 10, Page 119, Table 1, the DS1336 allows a load to be switched from its main power supply V_{CC} to a battery backup supply when V_{CC} falls out of tolerance. A user may selectively tie together any combination of the output pins to provide the desired high current supply, providing up to 300mA per OUT pin or a maximum of 1.5A. Depending upon the user's backup supply load requirements, either of the V_{BAT} outputs may be tied to the OUT pins to supply current when V_{CC} is out of tolerance. The DS1336 switches back to the higher current V_{CC} from battery current when PF and $\overline{PF}$ become inactive.

OPERATION

The required PF or $\overline{PF}$ input which controls the switching between the main V_{CC} and backup battery can be supplied by any of the devices listed in Table 1. All of the devices provide the DS1336 with a PF or $\overline{PF}$ signal, switching between a main supply V_{CC} and backup supply V_{BAT} when V_{CC} falls out of tolerance. For applications requiring switching from the V_{CC} supply inputs to V_{BAT}, the required PF or $\overline{PF}$ input to the DS1336 can be provided by the DS1236, DS1239, DS5001, or DS5340. For applications requiring switching from the V_{CC} inputs to the V_{BAT} input when V_{CC} begins falling out of tolerance, any of the Dallas Semiconductor devices listed in Table 1 can provide the DS1336 with the required switching input. A typical application is shown in Figure 1. For applications where switching between V_{CC} and V_{BAT} must occur at a voltage level such that V_{CC} is still greater than V_{BAT}, the OUT5 pin is recommended as it provides a diode path which will provide for a gradual transition between V_{CC} and V_{BAT}. OUT5 can be tied to the other OUTPUT pins to provide a gradual transition for all five current paths. In applications where tri-state switching is desired, OUT5 should be omitted. Only the $\overline{PF}$/PF pin is required for switching. In cases where the PF input will not be used, it should be connected to GND.

When either PF or $\overline{PF}$ is active, either of the V_{BAT0X} outputs is available, although they should not be tied together (Figure 2, "DS1336 Block Diagram"). V_{BAT01} is recommended for sensitive applications such as providing backup current to timekeepers, because its diode isolated path provides for increased protection. V_{BAT02} is not recommended for applications where it would be tied to an OUTPUT pin supplying a voltage greater than that of the backup battery because V_{BAT02} is not a diode isolated current path.

TYPICAL APPLICATION Figure 1



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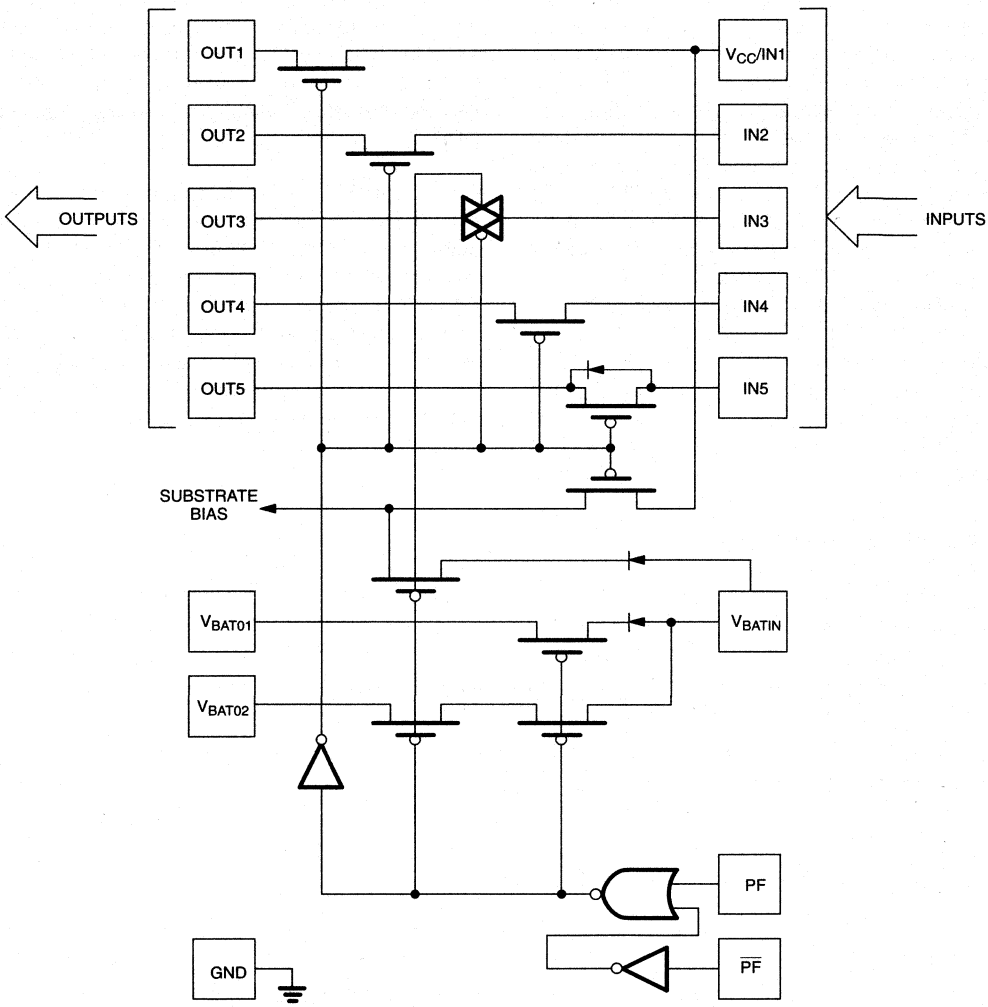
DS1336 BLOCK DIAGRAM Figure 2



DALLAS SEMICONDUCTOR DEVICES WHICH PROVIDE PF OR $\overline{PF}$ INPUT TO DS1336 Table 1

DEVICE	SWITCH > V_{BAT}	SWITCH AT V_{BAT}	DEVICE	SWITCH > V_{BAT}	SWITCH AT V_{BAT}
DS1211	X		DS1238	X	X
DS1212	X		DS1239	X	X
DS1231	X		DS1259	X	
DS1232	X		DS1260	X	
DS1233	X		DS1610	X	
DS1233A		X	DS1632	X	
DS1233D	X		DS1833	X	
DS1234	X		DS5001	X	X
DS1236	X	X	DS5340	X	X
DS1237	X				

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC CHARACTERISTICS

(t_A = 0°C to 70°C; V_{CC} = +5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC1}	3.0	5.0	5.5	V	1
Supply Current	I_{CC1}		0.25	1	mA	
Supply Current	I_{CC2}		50	100	nA	3
Input Low Voltage	V_{IL}			0.8	V	1
Input High Voltage	V_{IH}	2.0		V_{CC}	V	1
Current Output V_{CC}=V_{CC1}, PF=0, $\overline{PF}$=1	I_{CCO}			300	mA	2
Current Output V_{CC}=0, PF=1, $\overline{PF}$=0	I_{BATO2}			4	mA	4
Current, Forward Bias of V_{CC5} Diode	I_{FB}			20	mA	
Off Impedance	R_{OFF1}	5			MΩ	5
Off Impedance	R_{OFF2}	10			MΩ	6
On Impedance	R_{ON1}			0.7	Ω	7
On Impedance	R_{ON2}			50	Ω	8

AC CHARACTERISTICS

(t_A = 0°C to 70°C; V_{CC} = +5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Propagation Delay	t_{PD}		10		ns	9
Switch Delay Power Fail	t_{PF}		100		ns	
Switch Delay Power On	t_{PON}			100	ns	
Capacitance PF, $\overline{PF}$	C_I			7	pF	

NOTES:

1. All voltages referenced to ground.
2. I_{CCO} with a voltage drop of 0.2V from any V_{CCO} output.
3. V_{CC}=0, V_{BATIN}=3.0V.
4. V_{BATO2} with a voltage drop of 1.0V.
5. R_{OFF1} applies to $V_{CCO1,2,3,4}$.
6. R_{OFF2} applies to $V_{BATO1,2}$.
7. Applies to V_{CCO1-5}, 300 mA.
8. Applies to $V_{BATO1-2}$, 4 mA.
9. V_{CCI3} to V_{CCO3} delay when used as chip enable control for write protection of a memory device. In this application a current 8 mA source current on V_{CCI3} with 50 pF load on V_{CCO3} can be accommodated.

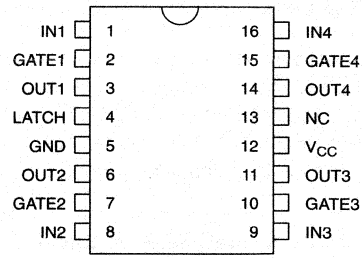
DALLAS SEMICONDUCTOR

DS1640/DS1640C
Personal Computer Power FET

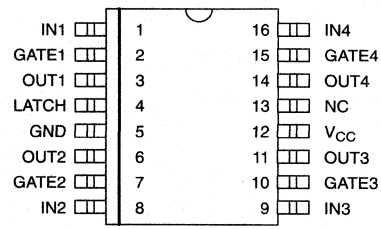
FEATURES

- Contains four P channel power FET switches that can each supply over 300 mA @ 0.2 volts drop
- Controlled directly from CMOS or TTL level signals
- Fast switching time of less than 10 µs at rated supply current
- 16-pin DIP or 16-pin SOIC surface mount package
- Positive logic signal turns each FET on and ground or low level signal turns each FET off
- Off condition allows less than 50 nA of current flow
- Low control gate capacitance of less than 5 pF
- FET gates can either follow inputs or be latched
- Designed for use with power supplies ranging from +3 to +5 volts

PIN ASSIGNMENT



16-Pin DIP (300 Mil)
See Mech. Drawings Section



16-Pin SOIC (300 Mil)
See Mech. Drawings Section

PIN DESCRIPTION

V_{CC}	-	+3 to +5 Volt Input
GND	-	Ground
IN1-IN4	-	FET Sources
OUT1-OUT4	-	FET Drains
GATE1-GATE4	-	FET Control Gates
NC	-	No Connection
LATCH	-	Gate Inputs Latch Control

8

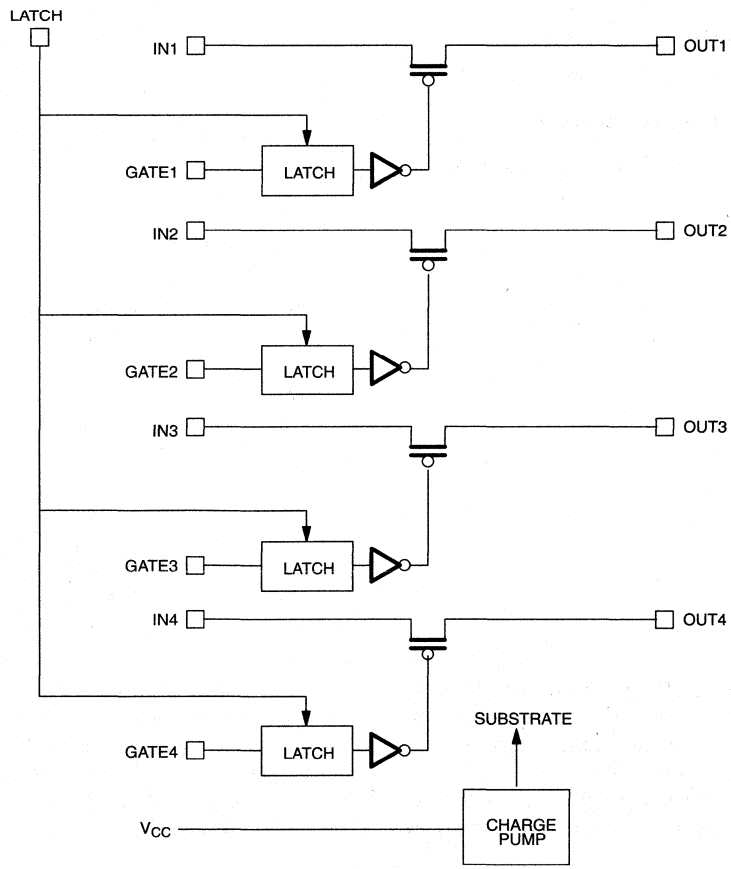
DESCRIPTION

The DS1640 contains four P channel power MOS FET's designed as switches to conserve power in personal computer systems. When connected to power management control units, power consuming devices like disk drives or display panel backlights can be routinely shut down to conserve battery or main power supply energy. The P channel power MOS FET's are individually controlled and are capable of handling 300 mA each continuously with less than 0.2 volts drop from input to output. The device requires a +3 → +5 volt power supply input which is used to power internal logic and to operate a gate bias generator.

OPERATION

With +3 ➛ +5 volts applied between the V_{CC} pin and ground, any one of four inputs can be connected or disconnected from its respective output based on the bias applied to the control gate (see Figure 1). A set of four internal latches is controlled by the latch input. The logic levels passed to the FET gates are controlled by the gate inputs and latch pin status. When the latch pin is logic 0, the gate input levels are inverted and passed directly to the control gates, enabling the switches to be switched both independently and asynchronously. With a transition from logic 0 to logic 1 on the latch pin, the input levels present on the gate inputs are locked by the four internal latches, maintaining the corresponding FET gates at those levels. As long as the latch input is maintained at logic 1, the FET gate levels are maintained. When the latch input is returned to logic 0, the gate inputs again are inverted and passed to the FET control gates without being latched. A TTL or CMOS logic 1 turns a switch completely on and TTL or CMOS logic 0 turns a switch completely off. The four switches can be operated independently or two or more can be connected in parallel for added current carrying capability. The four switches contained within the DS1640 are not designed to be operated in a linear manner. When V_{CC} is not applied to the DS1640 or if V_{CC} is not within nominal limits, the output levels and current carrying capability of the four switches are not guaranteed. When all four gate inputs are off (logic 0) the device enters a low V_{CC} current standby mode because the onboard charge pump is turned off. The gate and latch inputs are CMOS-compatible throughout the entire V_{CC} range and are TTL-compatible when V_{CC} falls between 4.5 and 5.5V.

DS1640 BLOCK DIAGRAM Figure 1



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	3.0		5.5	V	1, 2
Logic 0 Input 3.0 V ≤ V_{CC} ≤ 4.5 V	V_{IL2}	-0.3		+0.5	V	
Logic 0 Input 4.5 V ≤ V_{CC} ≤ 5.0 V	V_{IL1}	-0.3		+0.8	V	1
Logic 1 Input 3.0 V ≤ V_{CC} ≤ 5.0 V	V_{IH}	2.0		V_{CC}+0.5	V	1, 7
Source Voltage	V_{SOURCE}			V_{CC}+0.5	V	1, 7

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = +5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC1}		0.3	1	mA	3
Supply Current	I_{CC2}		0.1	1	µA	4
Switch Off Leakage	I_{SL}			100	nA	
Switch On Resistance	R_{ON}		0.3	.67	Ω	
Switch Current @ V_F = 200 mV	I_S			300	mA	5
Input Leakage	I_{IL}	-1		+1	µA	6
Gate Input Capacitance	C_G			5	pF	7

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = +5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Switching Time (OFF → ON)	t_{STON}			10	µs	
Switching Time (ON → OFF)	t_{STOFF}			10	µs	
Minimum Time to Engage Latch	t_{LM}			50	ns	

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NOTES:

1. All voltages are referenced to ground.
2. When V_{CC} is below minimum limits output levels are not guaranteed.
3. I_{CC1} is the supply current with one or more switches on.
4. I_{CC2} is when all switches are off and all inputs are within 0.5V of a supply rail.
5. Each switch is capable of carrying 300 mA maximum at 200 mV forward drop.
6. Input leakage applies to the four gate inputs and the latch input only.
7. Applies to each of four gate inputs and the latch input.

Dallas Semiconductor devices are built to the highest quality standards and manufactured for long term reliability. All DS1640 devices are made using the same quality materials and manufacturing methods. However, consumer versions of the DS1640 are not exposed to environmental stresses that some commercial device manufacturing flows require. Devices that are designated as consumer product have a "C" designator in the product number. For example, the DS1640C is a consumer grade product.

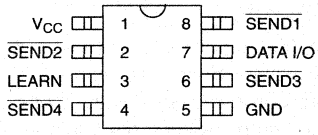
DALLAS SEMICONDUCTOR

DS1651
3-Code Lock
DS1652
Key Match Memory System

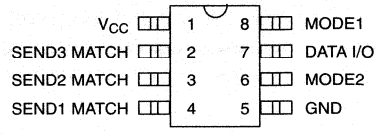
FEATURES

- The two–chip lock and key system forms the basis of a secure access system
- The match memory system is compatible with a variety of RF, serial, ultrasound, and optical transmission media
- The user–programmable 64–bit code or internally generated random 64–bit code prevents unauthorized copying of keys
- Each key and lock system is capable of generating and recognizing 3-code match conditions
- Keys are programmed from lock codes only under controlled user access/secure conditions
- Low–cost, economical
- Lock codes can be changed as many times as necessary
- 3V operation, 5V for programming
- Operating range of -25°C to +85°C
- All stored 64–bit codes in the lock and key are nonvolatile and retain the security code in the absence of power
- Applications include building entry, garage door openers, automobile entry and ignition, and local and remote identification

PIN ASSIGNMENT



DS1652 8-Pin DIP (300 Mil) and
DS1652S 8-Pin SOIC (208 Mil)
See Mech. Drawings
Section



DS1651 8-Pin DIP (300 Mil) and
DS1651S 8-Pin SOIC (208 Mil)
See Mech. Drawings
Section

DS1652 PIN DESCRIPTION

GND	-	Ground
DATA I/O	-	Serial Data Input/Output
$\overline{\text{SEND1}}$	-	Send Input 1
$\overline{\text{SEND2}}$	-	Send Input 2
$\overline{\text{SEND3}}$	-	Send Input 3
$\overline{\text{SEND4}}$	-	Send Input 4
LEARN	-	Learn Input

DS1651 PIN DESCRIPTION

MODE2	-	Function Control Pin
MODE1	-	Function Control Pin
V_{CC}	-	+3V to +5V Input
GND	-	Ground
DATA I/O	-	Serial Data Input/Output
SEND1 MATCH	-	Code Match Signal for SEND1
SEND2 MATCH	-	Code Match Signal for SEND2
SEND3 MATCH	-	Code Match Signal for SEND3

DESCRIPTION

The DS1651 Lock and DS1652 Key operate in combination to limit access of any secure system or area to keyholders. Both the DS1651 Lock and DS1652 Key contain a 64–bit memory which acts as the security code, controlling access. The code memory within the DS1651 Lock can be user–programmed with a known 64–bit code, or the DS1651 can generate a 64–bit code from a random number generator within the DS1651. Once set, the code is nonvolatile and can then be transferred to one or more DS1652 Key(s) under secure conditions.

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To gain access to the lock, the key's code must be transmitted to the lock via some user transmission media such as RF, optical, IR, ultrasound, or another serial medium. Upon receiving a transmission of a 64–bit key code, a DS1651 Lock will compare the requesting key's 64–bit code to the lock's programmed 64–bit code. If the key code matches the lock code, the lock generates a match signal, which can be used to allow access to the secure system.

OPERATION DS1651 LOCK

The main functional components of both the DS1651 and DS1652 are shown in Figures 3 and 4. The diagrams show that the internal functions of the lock and key are similar. From Figure 3, the primary components of the lock are its 64–bit–wide registers. The 64–bit code memories are the physical "lock" and contain the pattern against which all keys are measured for access. The 64–bit data memory records the 64–bit pattern transmitted by a potential key. The pulse input interpreter and reset generator accepts serial input data from the input pin.

The DS1651 Lock has four functional modes, which are controlled by the lock's mode control pins. The four modes are defined as follows:

MODE2	MODE1	FUNCTIONAL MODE
0	0	Operation Mode: Receiving codes from key(s).
0	1	Learn Mode: Program with user–provided 64–bit codes.
1	0	Duplicate Mode: Transmit 64-bit code memory contents.
1	1	Learn Mode: Program with internally generated, random 64 bits.

The Learn and Duplicate modes can only be entered from Operation mode. The DS1651 samples the level of MODE1 and MODE2 10 ms after a transition on either pin. This sample is used to tell the DS1651 in which mode it should be operating.

In the Learn modes, the DS1651 Lock's code memory can be either programmed directly by the user or programmed using a random set of 1's and 0's created by the DS1651's random number generator. A user must have physical access to the DS1651 to place it in Learn mode. To place the DS1651 Lock in Learn mode, the DS1651's V_{CC} input must be at 4.5V minimum with MODE1 or both MODE1 and MODE2 pins driven high, telling the DS1651 to enable the contents of its code memory to be rewritten. If MODE1 is high, then the DS1651 enables its code memory to be rewritten using a user–defined 64–bit code, which it expects to see on its data I/O pin. At the end of sending the 64–bit code to the DS1651, the mode pins must both be driven low, returning the lock to operation mode, before entering any other mode. (See timing diagram "Learn Modes DS1651 Lock.") If MODE2 and MODE1 are high, then the DS1651 Lock performs an internal operation in which it uses its internal random number generator to create a 64 bit pattern of 1's and 0's and loads it into the code data memory, from LSB to MSB. When all 64 bits have been written, the DS1651 has a new code memory that can be programmed into DS1652 Keys. After this operation is completed, the mode pins must both be driven low to return the DS1651 to operation mode, before entering any other mode.

The DS1651 will not reprogram its 64–bit code memory using its internal random number generator until another transition from 0 to 1 is seen on both its MODE2 and MODE1 pins.

For the DS1651 Lock to transfer its code memory into a DS1652 Key, the DS1651 must be in Duplication mode. To enter Duplication mode, the MODE2 pin must be driven high. The transition from 0 to 1 on the MODE2 pin and its maintenance at 1 causes the DS1651 Lock to transmit a reset signal followed by its 64–bit code memory through its data input/output pin. The lock will transmit the code only once. If another transmission is required, the mode pin must be driven to zero before being returned to 1 to send another 64–bit code copy. The data input/output pin of the DS1651 Lock must be physically connected to the data input pin of the target DS1652 Key in order to transfer a code from the lock to a key to be used with that lock. The target key must also be in Learn mode (see the section entitled "Operation DS1652 Key") for the key to accept as code the information transmitted by the lock. With these timing and hardware conditions satisfied, DS1652 Key programming can be performed quickly (<1 s) and easily with only one serial connection between the DS1651 and DS1652.

The DS1651 Lock is in its operation mode with its mode pins inactive. The receipt of a signal on the input/output pin which is active high for at least 720 µs is treated as a reset signal from a key about to transmit its code. The interpreted pattern of 1's and 0's sampled in the 2 ms

wide windows is written into the data memory for comparison to the lock's code memories. If the comparison shows a match with one of the memories, then the DS1651 drives the appropriate SENDX MATCH signal. If the code does not match, the DS1651 performs no operations, but waits for the next reset signal.

OPERATION DS1652 KEY

The operation of the DS1652 Key is similar to that of the DS1651 (Figure 4). The key is programmed with code generated by the DS1651 Lock with the lock in Duplication mode and the key in Learn mode.

For the DS1652 Key to be programmed, the LEARN pin must be driven active high. The DS1652 Key's data input pin must be physically connected to the DS1651 Lock's data input/output pin for the DS1652 Key to successfully accept a code from a DS1651 Lock. Once connected and in the Learn mode, the DS1652 Key is ready to accept its 64–bit code. The DS1652 Key will recognize the 720 µs wide active high reset signal and will use the rising edge of each subsequent signal to determine the contents of 64 consecutive 2 ms wide data windows as logic 1 or logic 0. The contents of the 64 consecutive windows, transmitted by the lock, become latched into the nonvolatile 64–bit code memory of the DS1652 Key. The key will perform no other operations until the LEARN pin becomes inactive, returning the DS1652 to its operation mode. The DS1652 Key will transmit a reset signal and its code memory out of its data output pin a maximum of three times as long as the $\overline{\text{SENDX}}$ input is asserted. The DS1652 Key will transmit a version of the code that is specifically tailored to the $\overline{\text{SENDX}}$ input being triggered. (See diagram entitled "DS1691 Lock, Match Signals.")

SERIAL PULSE PROTOCOL

The DS1651 and DS1652 transmit and receive data serially, according to the protocol listed in the timing diagrams.

The transmission and reception of data begins with the rising edge of the 720 µs reset signal. The DS1651 and DS1652 then begin looking for data in 2 ms windows. Each data window begins with the rising edge of a pulse. The duration of the pulse determines whether a logical one or logical 0 is present in that window (logical one pulse duration is six times as long as logical zero pulse duration).

For 128 ms, the DS1651 or DS1652 will time the duration of the active pulse in each window. Once the pulse is interpreted as a 1 or a 0, the data bit is written to the appropriate register (depending on the mode of the device). This iterative process continues through all 64 bits until they are written. For the DS1651 Lock, after 64 bits are written, a compare operation is performed. For the DS1652, after 64 bits are written, the key can be returned to its operation mode for use.

OPERATION, LOCK AND KEY

The DS1651 Lock and DS1652 Key provide a security code matching system which can be used as the code control logic of any security system. The unique DS1651 Lock provides the system designer with the option of pre-programming a lock or series of locks with a known set of 64–bit codes that can only be changed by having physical access to the lock. If known codes are not required, the DS1651 can generate its own 64–bit code randomly. If the random number generator of the DS1651 Lock is used, not even the person programming the lock knows the 64–bit code.

The DS1652 Key is programmed from the DS1651 Lock and can be repeatedly reprogrammed to accept new codes. This feature not only prolongs the usable life of the key, but also provides the user the ability to recycle keys from one lock to be programmed for use with another lock. Materials invested in building keys are never obsoleted because keys can always be reprogrammed.

A significant contribution to maintaining the security of the DS1651 Lock is limiting the manner by which a lock can program a key with the code to open the lock. The only way in which a DS1652 Key will accept a code is to connect its input pin directly to the data input/output pin of a DS1651 Lock. Therefore the only method of transferral is by physically connecting the device holding the DS1652 Key with the device holding the DS1651 Lock. A quick and efficient method of implementing this interface is illustrated in Figure 1.

By designing the system key with three external leads, one tied to LEARN, one tied to ground, and one tied to the data I/O pin, the system key can accept a new code from a system lock only through these three connections. Once placed in a system lock, the DS1651 Lock could be enabled to transmit its code memory to the key. Because of the physical connection required for the

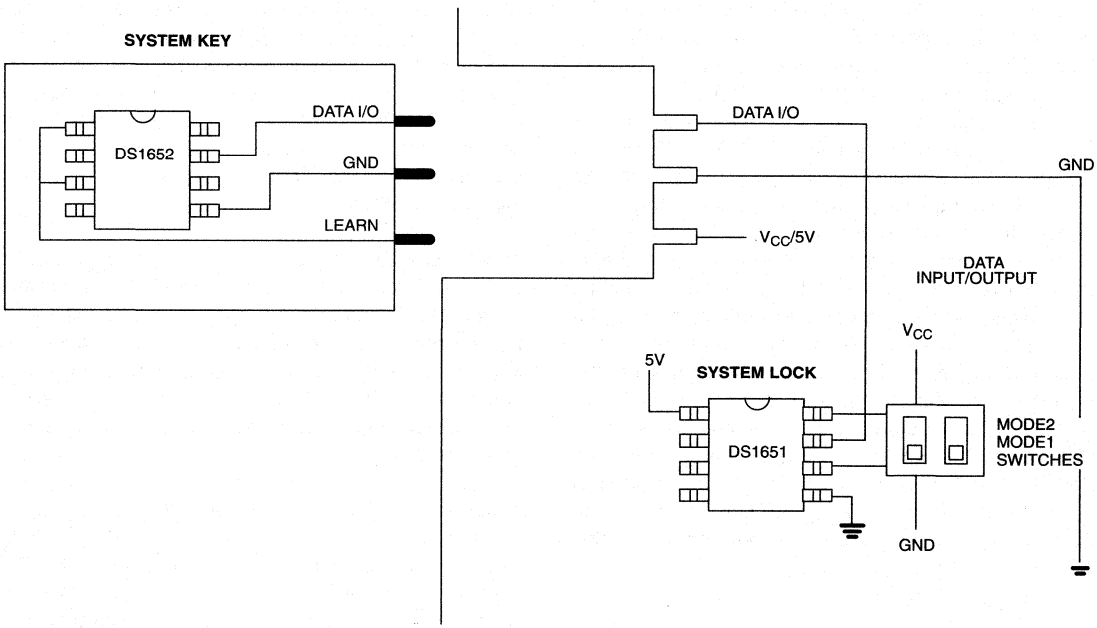
code data transfer, the lock and key combination is kept secure.

The method chosen to duplicate the key does not have to be the suggested method. This method is suggested as a way that

1. limits who can program keys
2. limits who can generate codes for the lock
3. limits who can, by generating a new code, invalidate the existing programmed keys.

As many keys as needed can be programmed. As required for security purposes or in case of the loss of a key, a new code can be generated and redistributed to the remaining keys. This enables the security system to continually reuse keys and obsolete the codes in any keys that become lost or stolen.

INTERIOR OF LOCK SECURED AREA Figure 1

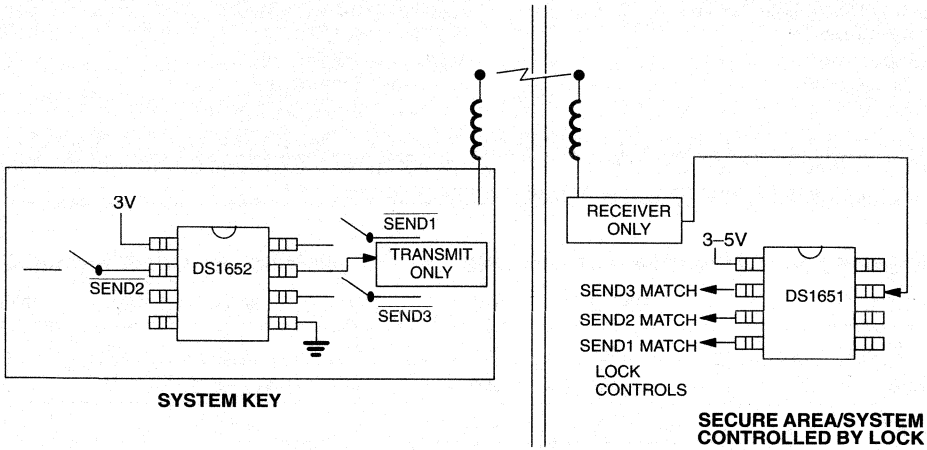


TYPICAL APPLICATION

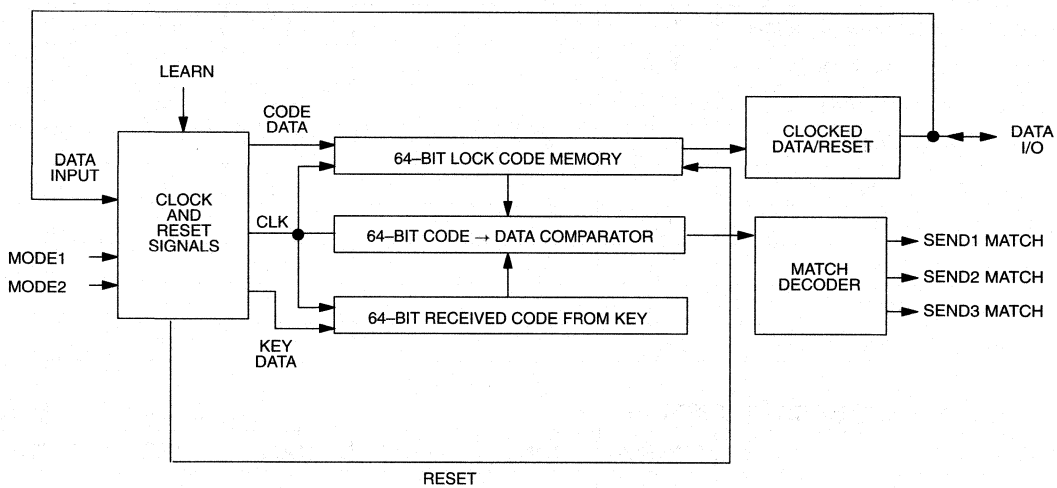
One of the easiest ways to implement the lock and key system is to use an RF transmitter to link the data input/output pin of the DS1652 Key to the DS1651's input pin.

For implementation, any transmission media capable of transmitting and receiving signals at the resolution required of the DS1651 and DS1652's serial pulse protocol can be used to link the key to a lock.

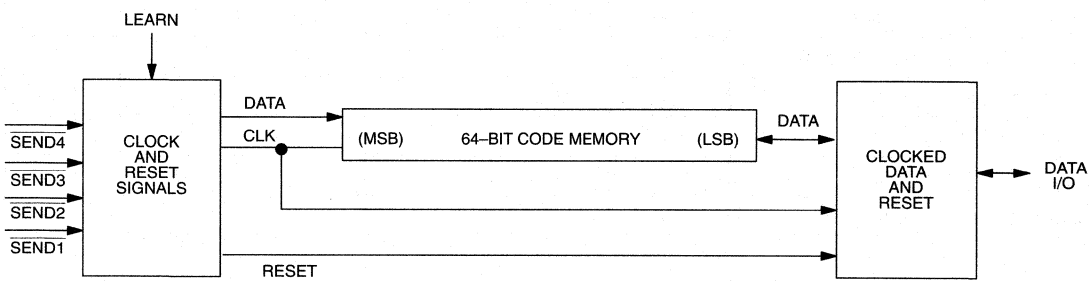
TYPICAL APPLICATION Figure 2



DS1651 LOCK BLOCK DIAGRAM Figure 3



DS1652 KEY BLOCK DIAGRAM Figure 4



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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to –V	-0.5V to +7.0V
Operating Temperature	–25°C to +85°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 15 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(-25°C to +85°C) DS1651 and DS1652

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	2.7	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.0	-	V_{CC}+0.3	V	1, 5
Logic 0 Input	V_{IL}	-0.3	-	+0.8	V	1, 5

DC ELECTRICAL CHARACTERISTICS

(-25°C to +85°C) DS1651

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current, Operation Mode	I_{CC1}		3	4	mA	2
Supply Current, Learn Mode	I_{CC2}		3	4	mA	2
Supply Current, Idle State	I_{CC3}		75	100	nA	2
V_{CC} Voltage, Learn Mode	V_{CCL}	4.5	5.0	5.5	V	1
Output High, Voltage	V_{OH}	2.4			V	1, 6
Output High, Current	I_{OH}	–1			mA	
Output Low, Voltage	V_{OL}	0.4			V	1, 6
Output Low, Current	I_{OL}	4			mA	
I/O Leakage Current	I_{IO}	-1		+1	µA	4

DC ELECTRICAL CHARACTERISTICS

(-25°C to +85°C) DS1652

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current, Send Mode	I_{CC1}		3	4	mA	2
Supply Current, Learn Mode	I_{CC2}		3	4	mA	2
Supply Current, Idle State	I_{CC3}	50	75	100	nA	2
V_{CC} Voltage, Learn Mode	V_{CCL}	4.5	5.0	5.5	V	1
Input Leakage (Data I/O pin)	I_{L1}	-1		+1	µA	3
Output High, Voltage	V_{OH}	2.4			V	1, 6
Output High, Current	I_{OH}	4			mA	
Output Low, Voltage	V_{OL}	0.4			V	1, 6
Output Low, Current	I_{OL}	1			mA	

AC ELECTRICAL CHARACTERISTICS DS1651 LOCK AND DS1652 KEY DATA TRANSMISSION PARAMETERS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Reset Active	t_R	540	720	900	µs	
Logic 1 Active	t_1	90	120	150	µs	
Logic 0 Active	t_0	15	20	25	µs	
SEND1 MATCH, SEND2 MATCH, and SEND3 MATCH	t_M	400	500	600	ms	
Data Sample Window	t_{DS}	1.5	2.0	2.5	ms	
Active Signal Pulse Width, Data I/O	t_{PW}	10		1080	µs	
Active Signal Pulse Width $\overline{\text{SEND1}}$ and $\overline{\text{SEND2}}$	t_S	100			ms	
Delay Between Last Mode Pin Transition to Operation Mode Change	t_T		10		ms	

CAPACITANCE

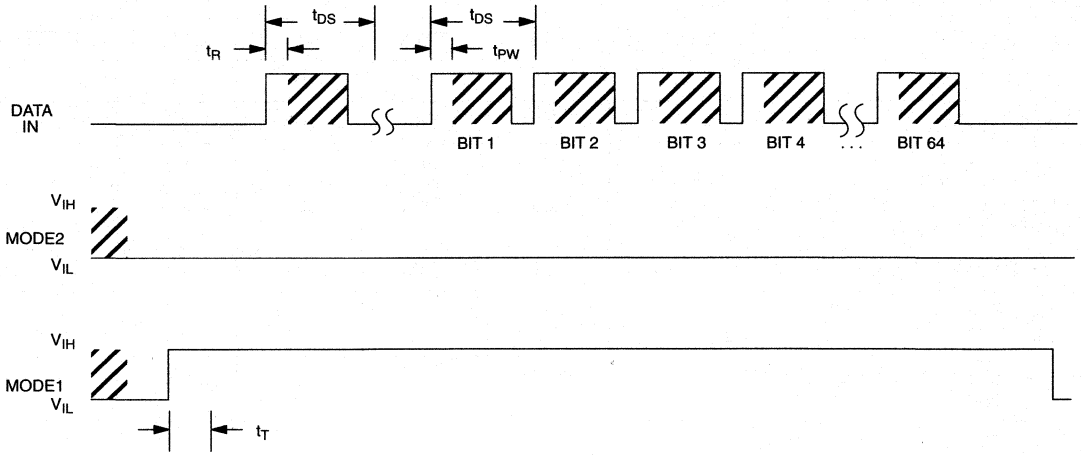
(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

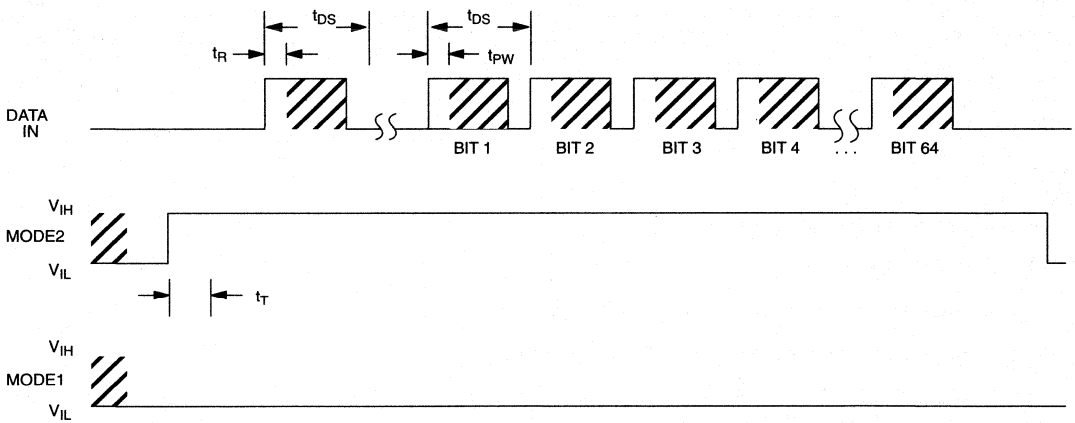
NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open.
3. Input leakage applies to DS1652 data I/O pin in input mode only.
4. Input/output leakage applies to the DS1651 data input/output pin.
5. The DS1652 $\overline{\text{SEND1}}$, $\overline{\text{SEND2}}$, $\overline{\text{SEND3}}$, and $\overline{\text{SEND4}}$ inputs are internally pulled up with 25KΩ resistors and require input levels of <0.5V for logic 0, and >V_{CC}–0.5V for logic 1. The DS1652 learn pin has an internal 10KΩ pulldown.
6. Valid for V_{CC}=5.0V ± 10%.

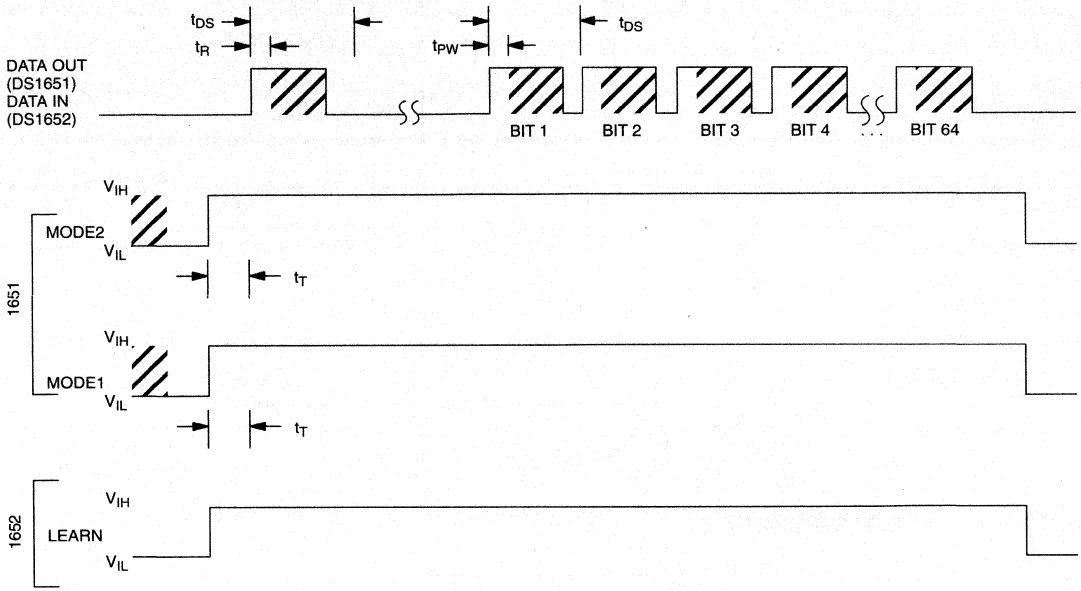
LEARN MODE DS1651 LOCK; USER PROGRAMMING



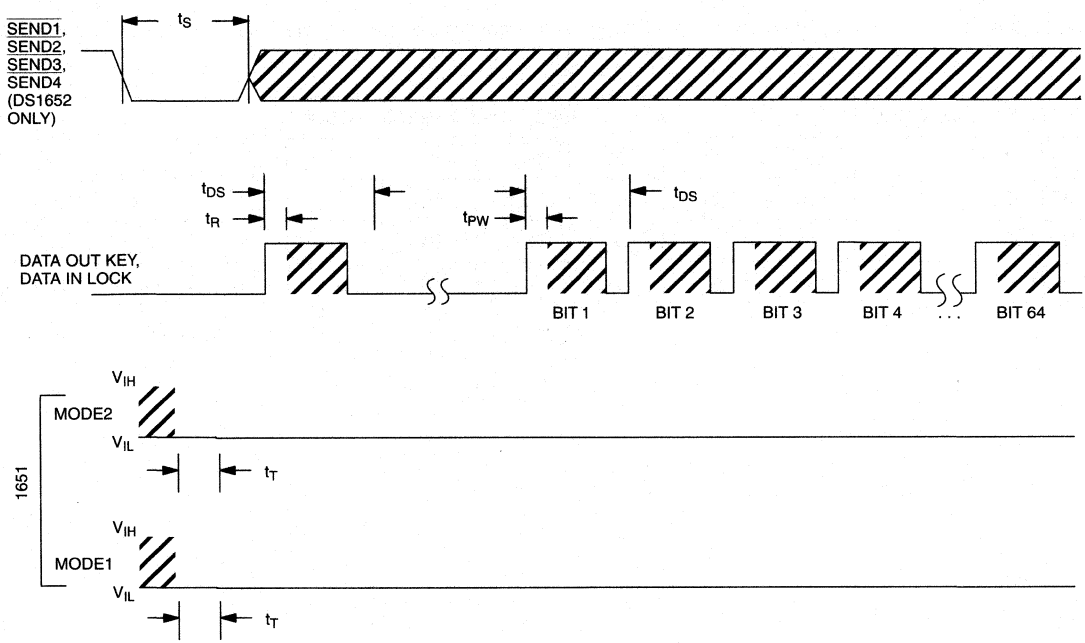
DS1652 LOCK; DUPLICATION MODE



LEARN MODE DS1652 KEY; LEARN MODE DS1651 LOCK, INTERNAL PROGRAMMING



OPERATION DS1651 LOCK AND DS1652 KEY



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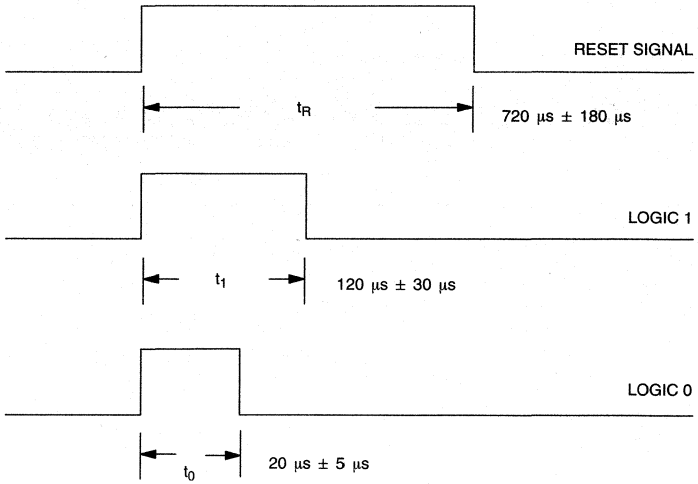
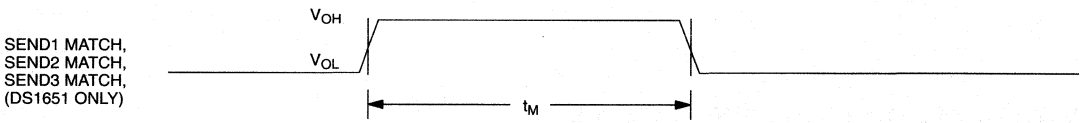
LOGIC TIMING DIAGRAMS



DS1651 LOCK, MATCH SIGNALS



When the DS1651 Lock's code comparator determines that code data it has received matches one of its code data memories, the appropriate match signal is driven active for the above diagram.

INPUT TRIGGERED	64 CODE TRANSMITTED AS:								
$\overline{SEND1}$	b_0	b_1	b_2	b_3	b_4	. . .	b_{61}	b_{62}	b_{63}
$\overline{SEND2}$	$\overline{b_0}$	$\overline{b_1}$	$\overline{b_2}$	$\overline{b_3}$	$\overline{b_4}$	. . .	$\overline{b_{61}}$	$\overline{b_{62}}$	$\overline{b_{63}}$
$\overline{SEND3}$	b_0	$\overline{b_1}$	b_2	$\overline{b_3}$	b_4	. . .	$\overline{b_{61}}$	b_{62}	$\overline{b_{63}}$
$\overline{SEND4}$	$\overline{b_0}$	b_1	$\overline{b_2}$	b_3	$\overline{b_4}$	. . .	b_{61}	$\overline{b_{62}}$	b_{63}

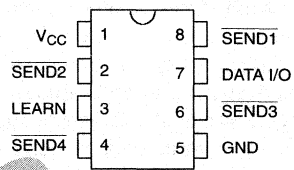
DALLAS SEMICONDUCTOR

DS1652B
Code Memory Key

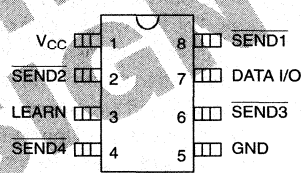
FEATURES

- The key forms the basis of a secure access system
- The DS1652B is compatible with a variety of RF, serial, ultrasound, and optical transmission media
- The user–programmable 64–bit code prevents unauthorized copying of keys
- Each key capable of generating 4–code conditions
- Keys are programmed from an external device only under controlled user access/secure conditions
- Low–cost, economical
- Key codes can be changed as many times as necessary
- 3V operation, 5V for programming
- Operating range of –25°C to +85°C
- All stored 64–bit codes in the key are nonvolatile and retain the security code in the absence of power
- Applications include building entry, garage door openers, automobile entry and ignition, and local and remote identification

PIN ASSIGNMENT



8-Pin DIP (300 Mil)
See Mech. Drawings Section



8-Pin SOIC (208 Mil)
See Mech. Drawings Section

PIN DESCRIPTION

V_{CC}	–	+3V to +5V Input
GND	–	Ground
DATA I/O	–	Serial Data Input/Output
$\overline{\text{SEND1}}$	–	Send Input 1
$\overline{\text{SEND2}}$	–	Send Input 2
$\overline{\text{SEND3}}$	–	Send Input 3
$\overline{\text{SEND4}}$	–	Send Input 4
LEARN	–	Learn Input

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DESCRIPTION

The DS1652B Code Memory Key operates as part of a system to limit access of any secure system or area to keyholders. The DS1652B key contains a 64–bit memory which acts as the security code, controlling access. Once set, the code is nonvolatile.

To gain access to a locked system, the key's code must be transmitted to the lock via some user transmission media such as RF, optical, IR, ultrasound, or another serial medium. Upon receiving a transmission of a 64–bit key code, a lock system must compare the requesting key's 64–bit code to the lock system's programmed code. If the key code matches the lock system code, the lock system must generate a match signal, which can be used to allow access to the secure system.

OPERATION DS1652B KEY

The operation of the DS1652B key is shown in Figure 1. The key is programmed with code from an external source with the key in Learn mode.

For the DS1652B key to be programmed, the LEARN pin must be driven active high, with V_{CC} on the DS1652B at least 4.5V. The DS1652B key's data input/output pin must be physically connected to the external programming device for the DS1652B key to successfully accept a code. Once connected and in the Learn mode, the DS1652B key is ready to accept its 64–bit code. The DS1652B key will recognize the 1600 µs wide active high reset signal, and will use the rising edge of each subsequent signal to determine the contents of 64 consecutive 2 ms wide data windows as logic 1 or logic 0. The contents of the 64 consecutive windows, transmitted by the external programming device, become latched into the nonvolatile 64–bit code memory of the DS1652B key. The key will perform no other operations until the LEARN pin becomes inactive, returning the DS1652B to its operation mode. The DS1652B key will transmit a reset signal and its code memory out of its data input/output pin a maximum of ten times as long as the $\overline{\text{SENDX}}$ input is asserted. The DS1652B key will transmit a version of the code that is specifically tailored to the $\overline{\text{SENDX}}$ input being triggered. (See Logic Timing Diagrams.)

SERIAL PULSE PROTOCOL

The DS1652B transmits and receives data serially, according to the protocol listed in the timing diagram.

The transmission and reception of data begins with the rising edge of the 1600 µs reset signal. The DS1652B then begins looking for data in 2 ms windows. Each data window begins with the rising edge of a pulse. The duration of the pulse determines whether a logical one or logical zero is present in that window (logical one pulse duration is twice as long as logical zero pulse duration).

For 128 ms, the DS1652B will time the duration of the active pulse in each window. Once the pulse is interpreted as a 1 or a 0, the data bit is written to the 64–bit code memory. This iterative process continues through all 64 bits until they are written. For the DS1652B, after 64 bits are written, the key may be returned to its operation mode for use.

OPERATION, LOCK AND KEY

The DS1652B key provides a security code matching system which can be used as the code control logic of any security system.

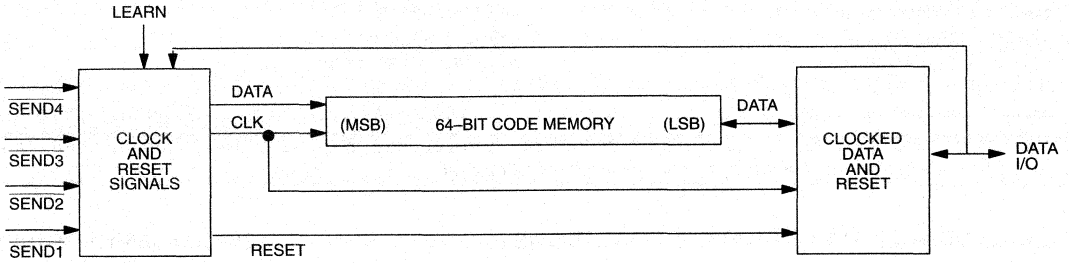
The DS1652B key is programmed from an external programming device and can be repeatedly reprogrammed to accept new codes. This feature not only prolongs the usable life of the key, but also provides the user the ability to recycle keys from one lock to be programmed for use with another lock. Materials invested in building keys are never obsoleted because keys may always be reprogrammed.

A significant contribution to maintaining the security of a DS1652B key based system is limiting the manner by which a key may be programmed with the code to open the lock. The only way in which a DS1652B key will accept code is to connect its data input/output pin directly to the external programming device. Therefore the only method of transferral is by physically connecting the device holding the DS1652B key with the device holding the programmer. A quick and efficient method of implementing this interface is illustrated in Figure 2.

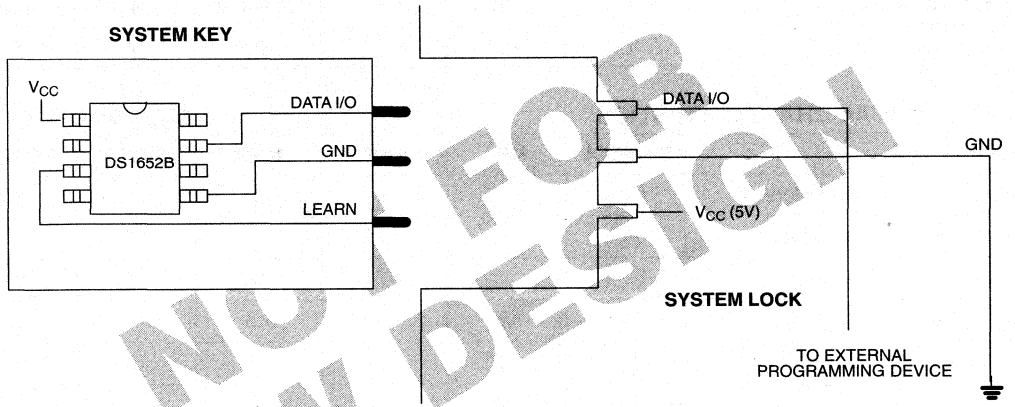
By designing the system key with three external leads, one tied to V_{CC} (5V), one tied to ground, and one tied to the input pin, the system key can accept a new code from a system lock only through these three connections.

As many keys as needed can be programmed. As required for security purposes, or in case of the loss of a key, a new code can be generated and redistributed to the remaining keys. This enables the security system to continually reuse keys and obsolete the codes in any keys that become lost or stolen.

DS1652B KEY BLOCK DIAGRAM Figure 1



INTERIOR OF LOCK SECURED AREA Figure 2



TYPICAL APPLICATION

One of the easiest ways to implement the lock and key system is to use an RF transmitter to link the data input/output pin of the DS1652B key to the system lock.

For implementation, any transmission media capable of transmitting and receiving signals at the resolution required of the DS1652B's serial pulse protocol can be used to link the key to the user's lock system.

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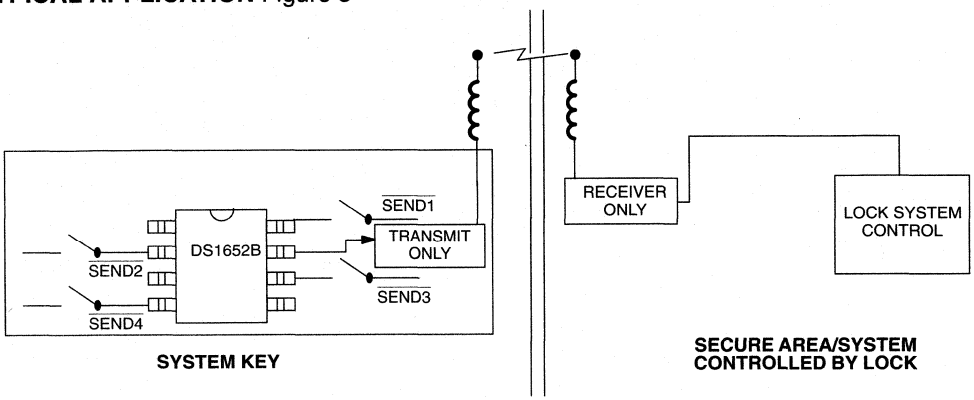
TYPICAL APPLICATION Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	–25°C to +85°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(-25°C to +85°C) DS1652B

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	2.7	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.0	–	V_{CC}+0.3	V	1, 4, 5, 6
Logic 0 Input	V_{IL}	–0.3	–	+0.8	V	1, 5, 6

DC ELECTRICAL CHARACTERISTICS

(-25°C to +85°C) DS1652B

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current, Send Mode	I_{CC1}		3	4	mA	2
Supply Current, Learn Mode	I_{CC2}		3	4	mA	2
Supply Current, Idle State	I_{CC3}		75	100	nA	2
V_{CC} Voltage, Learn Mode	V_L	4.5	5	5.5	V	1, 5
Input Leakage (Data Input)	I_{L1}	–1		+1	µA	3
Output High, Voltage	V_{OH}	2.4			V	1
Output High, Current	I_{OH}	–1			mA	
Output Low, Voltage	V_{OL}	0.4			V	1
Output Low, Current	I_{OL}	4			mA	

AC ELECTRICAL CHARACTERISTICS DS1652B KEY DATA TRANSMISSION PARAMETERS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Reset Active	t_R	1200	1600	2000	µs	
Logic 1 Active	t_1	600	800	1000	µs	
Logic 0 Active	t_0	300	400	500	µs	
Data Sample Window	t_{DS}	1.5	2.0	2.5	ms	
Active Signal Pulse Width, Data I/O	t_{PW}	300		2000	µs	
Active Signal Pulse Width $\overline{SEND1}$, $\overline{SEND2}$, $\overline{SEND3}$, and $\overline{SEND4}$	t_S	10			ms	
Delay Between LEARN Pin Transition and Operation Mode Change	t_T			10	ms	
Delay Between Minimum $\overline{SENDX}$ Assertion and Data Out Transmitted	t_{SD}			100	µs	
Number of Words Transmitted for 1 $\overline{SENDX}$ Input Recognized		10				

CAPACITANCE

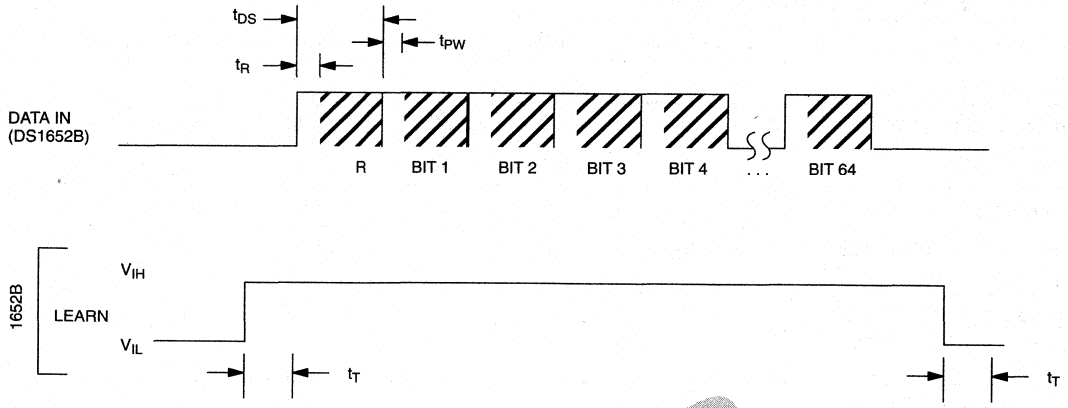
(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

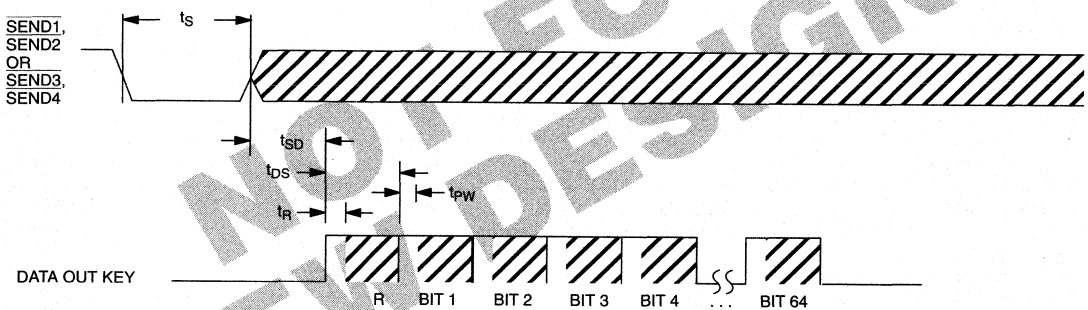
NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open.
3. Input leakage applies to DS1652B data input only.
4. Absolute maximum rating is 7.0V on any pin.
5. The DS1652B LEARN pin is internally pulled down with approximately a 10KΩ resistor.
6. The DS1652B $\overline{SEND1}$, $\overline{SEND2}$, $\overline{SEND3}$, and $\overline{SEND4}$ inputs are internally pulled up with approximately 25KΩ resistors.

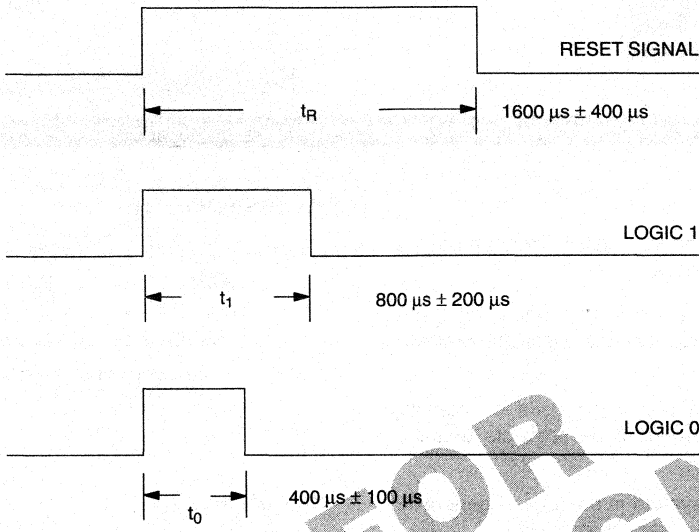
LEARN MODE DS1652B KEY



OPERATION DS1652B KEY



LOGIC TIMING DIAGRAMS



INPUT TRIGGERED	64 CODE TRANSMITTED AS:								
$\overline{\text{SEND1}}$ (DATA)*	b_0	b_1	b_2	b_3	b_4	. . .	b_{61}	b_{62}	b_{63}
$\overline{\text{SEND2}}$ ($\overline{\text{DATA}}$)	$\overline{b_0}$	$\overline{b_1}$	$\overline{b_2}$	$\overline{b_3}$	$\overline{b_4}$	. . .	$\overline{b_{61}}$	$\overline{b_{62}}$	$\overline{b_{63}}$
$\overline{\text{SEND3}}$ (ODD)	b_0	$\overline{b_1}$	b_2	$\overline{b_3}$	b_4	. . .	$\overline{b_{61}}$	b_{62}	$\overline{b_{63}}$
$\overline{\text{SEND4}}$ (EVEN)	$\overline{b_0}$	b_1	$\overline{b_2}$	b_3	$\overline{b_4}$	. . .	b_{61}	$\overline{b_{62}}$	b_{63}

*The bit pattern transmitted by the $\overline{\text{SEND1}}$ trigger it the unaltered contents of the DS1652B code memory. $\overline{\text{SEND2}}$, $\overline{\text{SEND3}}$, and $\overline{\text{SEND4}}$ transmit modified versions of this code a listed above.

8

DALLAS SEMICONDUCTOR

DS1653
4-Code Lock
DS1652
Key Match Memory System

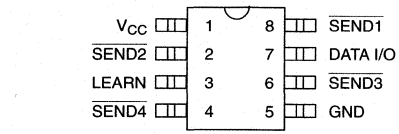
FEATURES

- The two–chip lock and key system form the basis of a secure access system
- The match memory system is compatible with a variety of RF, serial, ultrasound, and optical transmission media
- The user–programmable 64–bit code or internally generated random 64–bit code prevents unauthorized copying of keys
- Each key and lock system is capable of generating and recognizing 4-code match conditions
- Keys are programmed from lock codes only under controlled user access/secure conditions
- Low–cost, economical
- Lock codes can be changed as many times as necessary
- 3V operation, 5V for programming
- Operating range of -25°C to +85°C
- All stored 64–bit codes in the lock and key are nonvolatile and retain the security code in the absence of power
- Applications include building entry, garage door openers, automobile entry and ignition, and local and remote identification

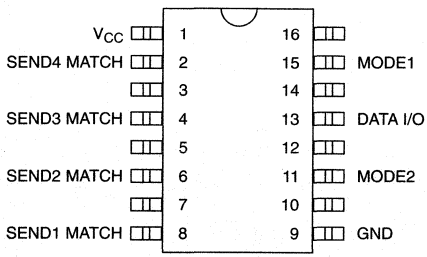
DESCRIPTION

The DS1653 Lock and DS1652 Key operate in combination to limit access of any secure system or area to keyholders. Both the DS1653 Lock and DS1652 Key contain a 64–bit memory which acts as the security code, controlling access. The code memory within the DS1653 Lock can be user programmed with a known 64–bit code, or the DS1653 can generate a 64–bit code from an internal random number generator. Once set, the code is nonvolatile and can then be transferred to one or more DS1652 Key(s) under secure conditions.

PIN ASSIGNMENT



DS1652 8-Pin DIP (300 Mil) and DS1652S 8-Pin SOIC (208 Mil)
See Mech. Drawings Section



DS1653 16-Pin DIP (300 Mil) and DS1653S 16-Pin SOIC (300 Mil)
See Mech. Drawings Section

DS1652 PIN DESCRIPTION

GND	-	Ground
DATA I/O	-	Serial Data Input/Output
$\overline{\text{SEND1}}$	-	Send Input 1
$\overline{\text{SEND2}}$	-	Send Input 2
$\overline{\text{SEND3}}$	-	Send Input 3
$\overline{\text{SEND4}}$	-	Send Input 4
LEARN	-	Learn Input
V_{CC}	-	+3V to +5V Input

DS1653 PIN DESCRIPTION

MODE2	-	Function Control Pin
MODE1	-	Function Control Pin
V_{CC}	-	+3V to +5V Input
GND	-	Ground
DATA I/O	-	Serial Data Input/Output
SEND1 MATCH	-	Code Match Signal for SEND1
SEND2 MATCH	-	Code Match Signal for SEND2
SEND3 MATCH	-	Code Match Signal for SEND3
SEND4 MATCH	-	Code Match Signal for SEND4

To gain access to the lock, the key's code must be transmitted to the lock via some user transmission media such as RF, optical, IR, ultrasound, or another serial medium. Upon receiving a transmission of a 64–bit key code, a DS1653 Lock will compare the requesting key's 64–bit code to the lock's programmed 64–bit code. If the key code matches the lock code, the lock generates a match signal, which can be used to allow access to the secure system.

OPERATION DS1653 LOCK

The main functional components of both the DS1653 and DS1652 are shown in Figures 3 and 4. The diagrams show that the internal functions of the lock and key are similar. From Figure 3, the primary components of the lock are its 64–bit–wide registers. The 64–bit code memories are the physical "lock" and contain the pattern against which all keys are measured for access. The 64–bit data memory records the 64–bit pattern transmitted by a potential key. The pulse input interpreter and reset generator accepts serial input data from the input pin.

The DS1653 Lock has four functional modes, which are controlled by the lock's mode control pins. The four modes are defined as follows:

MODE2	MODE1	FUNCTIONAL MODE
0	0	Operation Mode: Receiving codes from key(s).
0	1	Learn Mode: Program with user–provided 64–bit codes.
1	0	Duplicate Mode: Transmit 64-bit code memory contents.
1	1	Learn Mode: Program with internally generated random 64 bits.

The Learn and Duplicate modes can only be entered from Operation mode. The DS1653 samples the level of MODE1 and MODE2 10 ms after a transition on either pin. This sample is used to tell the DS1653 in which mode it should be operating.

In the Learn modes, the DS1653 Lock's code memory can be either programmed directly by the user or programmed using a random set of 1's and 0's created by the DS1653's random number generator. A user must have physical access to the DS1653 to place it in Learn mode. To place the DS1653 Lock in Learn mode, the DS1653's V_{CC} input must be at 4.5V minimum with MODE1 or both MODE1 and MODE2 pins driven high, telling the DS1653 to enable the contents of its code memory to be rewritten. If MODE1 is high, then the DS1653 enables its code memory to be rewritten using a user–defined, 64–bit code, which it expects to see on its data I/O pin. At the end of sending the 64–bit code to the DS1653, the mode pins must both be driven low, returning the lock to operation mode, before entering any other mode. (See timing diagram "Learn Modes DS1653 Lock.") If MODE2 and MODE1 are high, then the DS1653 Lock uses its internal random number generator to create a 64–bit pattern of 1's and 0's and loads it into the code data memory, from LSB to MSB. When all 64 bits have been written, the DS1653 has a new code memory that can be programmed into DS1652 Keys. After this operation is completed, the mode pins must both be driven low to return the DS1653 to operation mode before entering any other mode.

The DS1653 will not reprogram its 64–bit code memory using its internal random number generator until another transition from 0 to 1 is seen on both its MODE2 and MODE1 pins.

For the DS1653 Lock to transfer its code memory into a DS1652 Key, the DS1653 Lock must be in duplication mode. To enter the duplication mode, the MODE2 pin must be driven high. The transition from 0 to 1 on the MODE2 pin, and its maintenance at 1 causes the DS1653 Lock to transmit a reset signal followed by its 64–bit code memory through its data input/output pin. The lock will transmit the code only once. If another transmission is required, the mode pin must be driven to zero before being returned to 1 to send another 64–bit code copy. The data input/output pin of the DS1653 Lock must be physically connected to the data input pin of the target DS1652 Key in order to transfer a code from the lock to a key to be used with that lock. The target key must also be in Learn mode (see operation DS1652 Key) for the key to accept as code the information transmitted by the lock. With these timing and hardware conditions satisfied DS1652 Key programming can be performed quickly (<1 s) and easily with only one serial connection between the DS1653 and DS1652.

The DS1653 Lock is in its Operation mode with its mode pins inactive. The receipt of a signal on the input/output pin which is active high for at least 720 µs is treated as a reset signal from a key about to transmit its code. The interpreted pattern of 1's and 0's sampled in the 2 ms wide windows is written into the data memory for com-

parison to the lock's code memories. If the comparison shows a match with one of the memories, then the DS1653 drives the appropriate SENDX MATCH signal. If the code does not match, the DS1653 performs no operations, but waits for the next reset signal.

OPERATION DS1652 KEY

The operation of the DS1652 Key is similar to that of the DS1653 (Figure 2). The key is programmed with code generated by the DS1653 Lock with the lock in duplication mode and the key in Learn mode.

For the DS1652 Key to be programmed, the LEARN pin must be driven active high. The DS1652 Key's data input pin must be physically connected to the DS1653 Lock's data input/output pin for the DS1652 Key to successfully accept a code from a DS1653 Lock. Once connected and in the Learn mode, the DS1652 Key is ready to accept its 64–bit code. The DS1652 Key will recognize the 720 µs wide active high reset signal, and will use the rising edge of each subsequent signal to determine the contents of 64 consecutive 2 ms wide data windows as logic 1 or logic 0. The contents of the 64 consecutive windows, transmitted by the lock, become latched into the nonvolatile 64–bit code memory of the DS1652 Key. The key will perform no other operations until the LEARN pin becomes inactive, returning the DS1652 to its operation mode. The DS1652 Key will transmit a reset signal and its code memory out of its data output pin a maximum of three times as long as the $\overline{\text{SENDX}}$ input is asserted. The DS1652 Key will transmit a version of the code that is specifically tailored to the $\overline{\text{SENDX}}$ input being triggered. (See diagram "DS1693 Match Signals".)

SERIAL PULSE PROTOCOL

The DS1653 and DS1652 transmit and receive data serially, according to the protocol listed in the timing diagrams.

The transmission and reception of data begins with the rising edge of the 720 µs reset signal. The DS1653 and DS1652 then begin looking for data in 2 ms windows. Each data window begins with the rising edge of a pulse. The duration of the pulse determines whether a logical one or logical zero is present in that window (logical one pulse duration is six times as long as logical zero pulse duration).

For 128 ms, the DS1653 or DS1652 will time the duration of the active pulse in each window. Once the pulse is interpreted as a 1 or a 0, the data bit is written to the appropriate register (depending on the mode of the device). This iterative process continues through all 64 bits until they are written. For the DS1653 Lock, after 64 bits are written a compare operation is performed. For the DS1652, after 64 bits are written, the key can be returned to its operation mode for use.

OPERATION, LOCK AND KEY

The DS1653 Lock and DS1652 Key provide a security code matching system which can be used as the code control logic of any security system. The unique DS1653 Lock provides the system designer with the option of pre-programming a lock or series of locks with a known set of 64–bit codes that can only be changed by having physical access to the lock. If known codes are not required, the DS1653 can generate its own 64–bit code randomly. If the random number generator of the DS1653 Lock is used, not even the person programming the lock knows the 64–bit code.

The DS1652 Key is programmed from the DS1653 Lock and can be repeatedly reprogrammed to accept new codes. This feature not only prolongs the usable life of the key, but also provides the user the ability to recycle keys from one lock to be programmed for use with another lock. Materials invested in building keys are never obsoleted because keys can always be reprogrammed.

A significant contribution to maintaining the security of the DS1653 Lock is limiting the manner by which a lock can program a key with the code to open the lock. The only way in which a DS1652 Key will accept code is to connect its input pin directly to the data input/output pin of a DS1653 Lock. Therefore the only method of transferral is by physically connecting the device holding the DS1652 Key with the device holding the DS1653 Lock. A quick and efficient method of implementing this interface is illustrated in Figure 1.

By designing the system key with three external leads, one tied to LEARN, one tied to ground, and one tied to the data I/O pin, the system key can accept a new code from a system lock only through these three connections. Once placed in a system lock, the DS1653 Lock

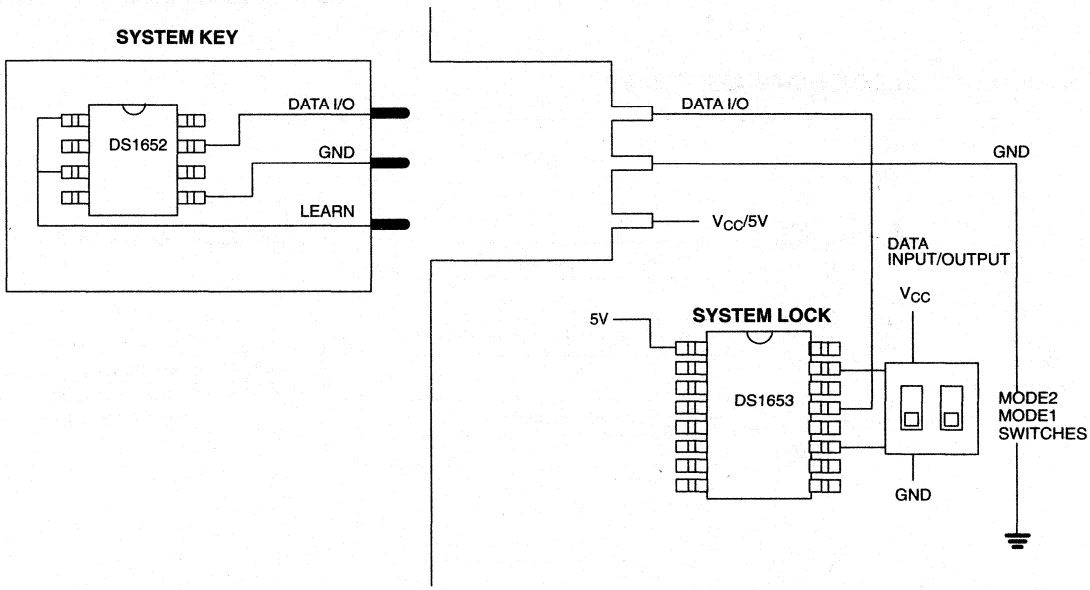
could be enabled to transmit its code memory to the key. Because of the physical connection required for the code data transfer, the lock and key combination is kept secure.

The method chosen to duplicate the key does not have to be the suggested method. This method is suggested as a way that

1. limits who can program keys
2. limits who can generate codes for the lock
3. limits who can, by generating a new code, invalidate the existing programmed keys.

As many keys as needed can be programmed. As required for security purposes or in case of the loss of a key, a new code can be generated and redistributed to the remaining keys. This enables the security system to continually reuse keys and obsolete the codes in any keys that become lost or stolen.

INTERIOR OF LOCK SECURED AREA; PROGRAMMING MODE Figure 1



TYPICAL APPLICATION

One of the easiest ways to implement the lock and key system is to use an RF transmitter to link the data input/output pin of the DS1652 Key to the DS1653's input pin.

For implementation, any transmission media capable of transmitting and receiving signals at the resolution required of the DS1653 and DS1652's serial pulse protocol can be used to link the key to a lock.

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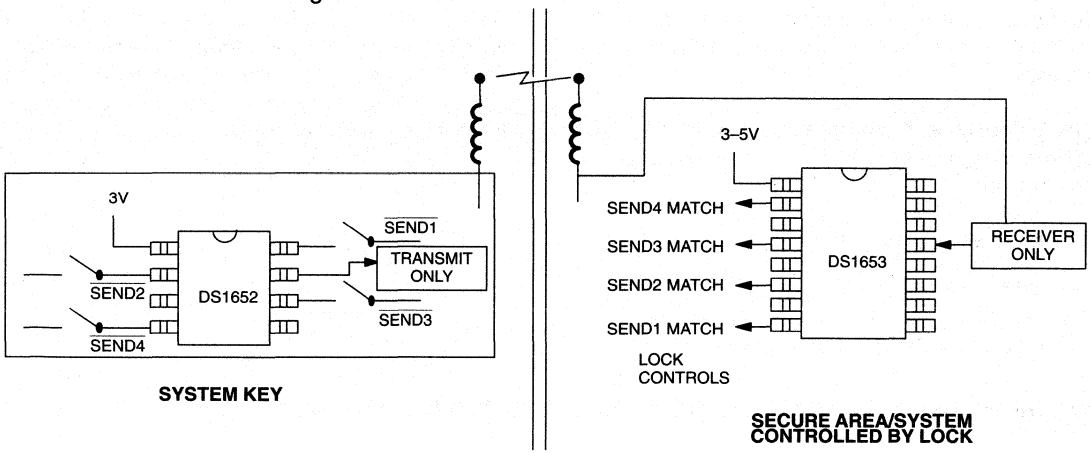
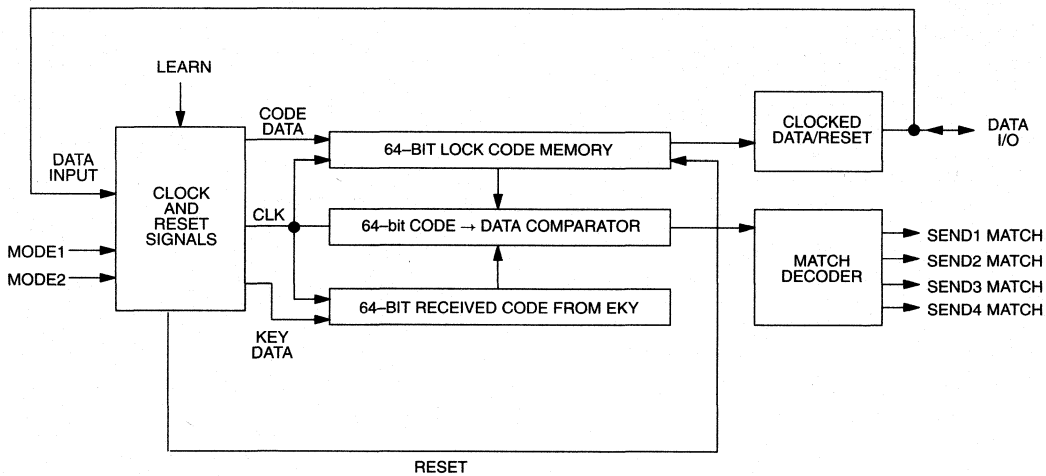
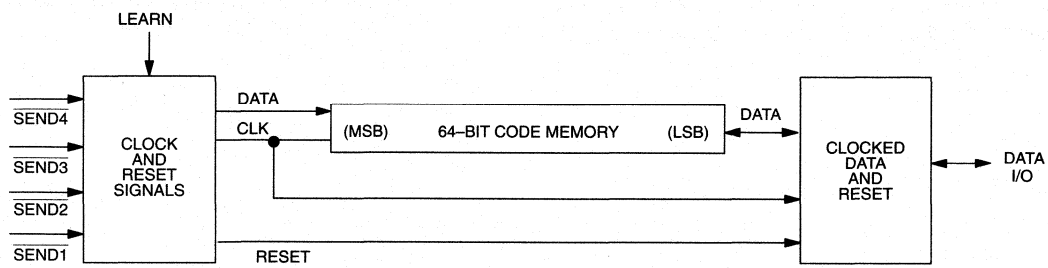
TYPICAL APPLICATION Figure 2



DS1653 LOCK BLOCK DIAGRAM Figure 3



DS1652 KEY BLOCK DIAGRAM Figure 4



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to -V	-0.5V to +7.0V
Operating Temperature	-25°C to +85°C
Programming Temperature	-10°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 15 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(-25°C to + 85°C) DS1653 and DS1652

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	2.7	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.0	-	V_{CC}+0.3	V	1, 5, 6
Logic 0 Input	V_{IL}	-0.3	-	+0.8	V	1, 5, 6

DC ELECTRICAL CHARACTERISTICS

(-25°C to 85°C) DS1653

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current, Operation Mode	I_{CC1}		3	4	mA	2
Supply Current, Learn Mode	I_{CC2}		3	4	mA	2
Supply Current, Idle State	I_{CC3}		75	100	nA	2
V_{CC} Voltage, Learn Mode	V_{CCL}	4.5	5.0	5.5	V	1, 5
Output High, Voltage	V_{OH}	2.4			V	1, 7
Output High, Current	I_{OH}	–1			mA	
Output Low, Voltage	V_{OL}	0.4			V	1, 7
Output Low, Current	I_{OL}	4			mA	
I/O Leakage Current	I_{IO}	-1		+1	µA	4

DC ELECTRICAL CHARACTERISTICS

(-25°C to 85°C) DS1652

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current, Send Mode	I_{CC1}		3	4	mA	2
Supply Current, Learn Mode	I_{CC2}		3	4	mA	2
Supply Current, Idle State	I_{CC3}	50	75	100	nA	2
V_{CC} Voltage, Learn Mode	V_{CCL}	4.5	5.0	5.5	V	1, 5
Input Leakage (Data Input)	I_{L1}	-1		+1	µA	3
Output High, Voltage	V_{OH}	2.4			V	1, 7
Output High, Current	I_{OH}	4			mA	
Output Low, Voltage	V_{OL}	0.4			V	1, 7
Output Low, Current	I_{OL}	1			mA	

AC ELECTRICAL CHARACTERISTICS DS1653 LOCK AND DS1652 KEY DATA TRANSMISSION PARAMETERS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Reset Active	t_R	540	720	900	µs	
Logic 1 Active	t_1	90	120	150	µs	
Logic 0 Active	t_0	15	20	25	µs	
SEND1 MATCH, SEND2 MATCH, SEND3 MATCH, and SEND4 MATCH	t_M	400	500	600	ms	
Data Sample Window	t_{DS}	1.5	2.0	2.5	ms	
Active Signal Pulse Width, Data I/O	t_{PW}	10		1080	µs	
Active Signal Pulse Width $\overline{SEND1}$ and $\overline{SEND2}$	t_S	100			ms	
Delay Between Last Mode Pin Transition to Operation Mode Change	t_T		10		ms	

CAPACITANCE

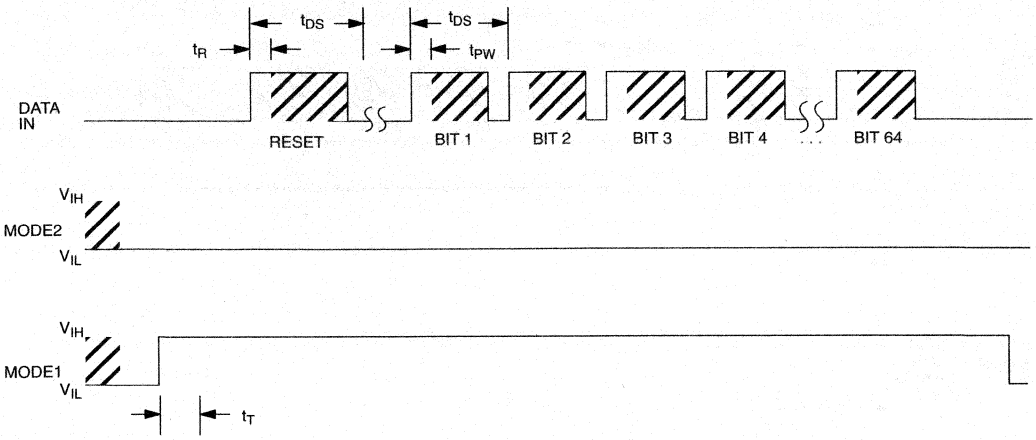
(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

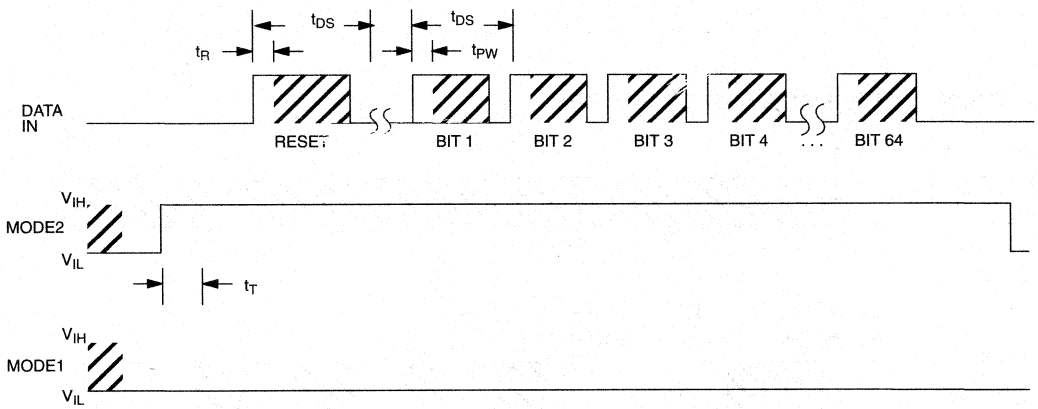
NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open.
3. Input leakage applies to DS1652 data I/O pin in input mode only.
4. Input/output leakage applies to the DS1653 data input/output pin.
5. The DS1652 LEARN pin has an internal pulldown.
6. Temperature range for programming is -10°C to +85°C.
7. These output voltages are valid for a typical V_{CC} of 5.0V ± 10%.

LEARN MODE DS1653 LOCK; USER PROGRAMMING



DS1653 LOCK; DUPLICATION MODE



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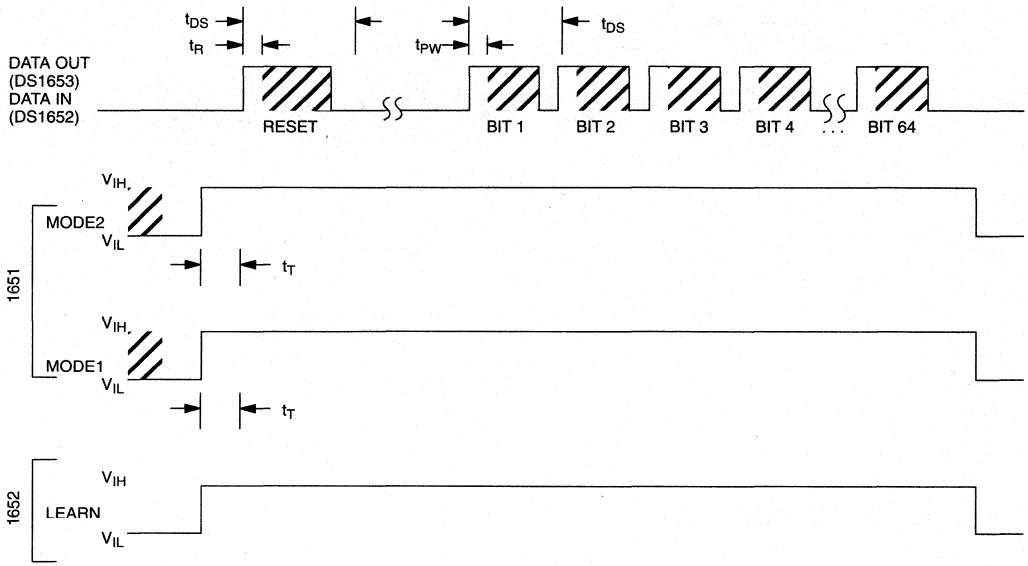
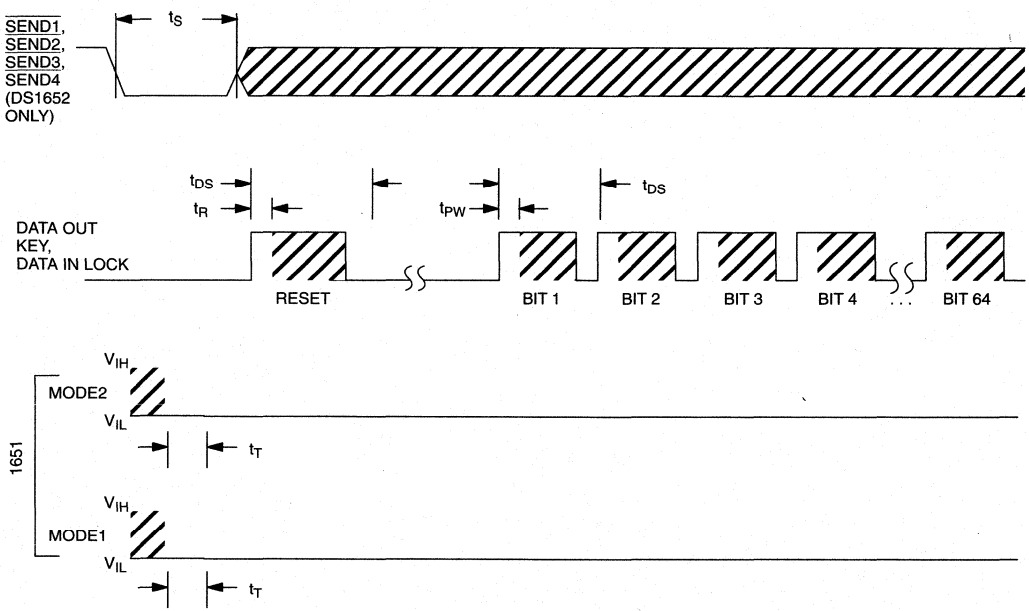
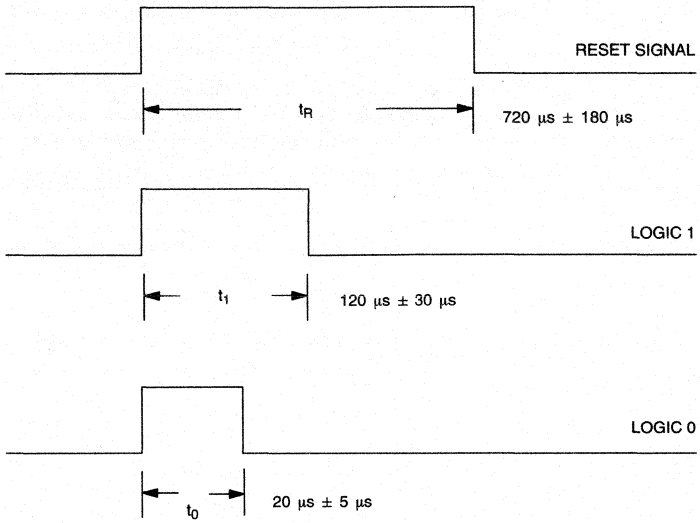
LEARN MODE DS1652 KEY; LEARN MODE DS1653 LOCK, INTERNAL PROGRAMMING



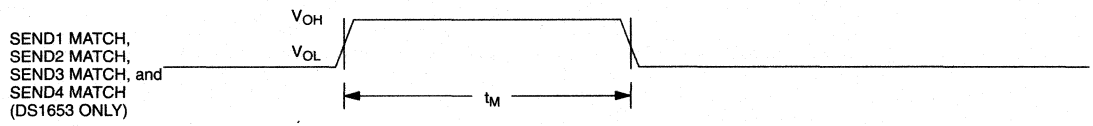
OPERATION DS1653 LOCK AND DS1652 KEY



LOGIC TIMING DIAGRAMS



DS1653 LOCK, MATCH SIGNALS



When the DS1653 Lock's code comparator determines that code data it has received matches one of its code data memories, the appropriate match signal is driven active for the above diagram.

INPUT TRIGGERED	64 CODE TRANSMITTED AS:								
$\overline{SEND1}$	b_0	b_1	b_2	b_3	b_4	. . .	b_{61}	b_{62}	b_{63}
$\overline{SEND2}$	$\overline{b_0}$	$\overline{b_1}$	$\overline{b_2}$	$\overline{b_3}$	$\overline{b_4}$	. . .	$\overline{b_{61}}$	$\overline{b_{62}}$	$\overline{b_{63}}$
$\overline{SEND3}$	b_0	$\overline{b_1}$	b_2	$\overline{b_3}$	b_4	. . .	$\overline{b_{61}}$	b_{62}	$\overline{b_{63}}$
$\overline{SEND4}$	$\overline{b_0}$	b_1	$\overline{b_2}$	b_3	$\overline{b_4}$	. . .	b_{61}	$\overline{b_{62}}$	b_{63}

8

TERMINATION PRODUCTS

9

PRELIMINARY

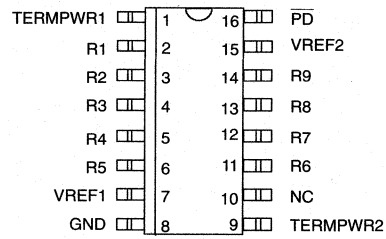
DALLAS SEMICONDUCTOR

DS2105
SCSI Terminator

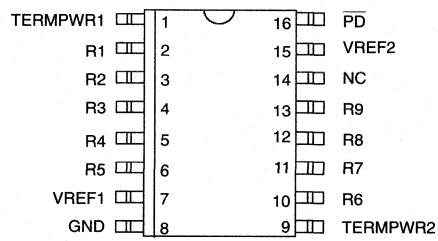
FEATURES

- Fully compliant with SCSI, SCSI-2, and emerging SCSI-3 standards
- Functionally compatible to the DS21S07A, targeted for high volume applications
- Provides active termination for 9 signal lines
- Laser-trimmed 110 ohm termination resistors have 5% tolerance
- Low dropout voltage
- Power-down mode isolates termination resistors from the bus
- Fully supports actively negated SCSI signals
- Onboard thermal shutdown circuitry
- 16-pin plastic SOIC (DS2105)

PIN ASSIGNMENT



DS2105Z 16-Pin SOIC (150 mil)



DS2105S 16-Pin SOIC (300 mil)

DESCRIPTION

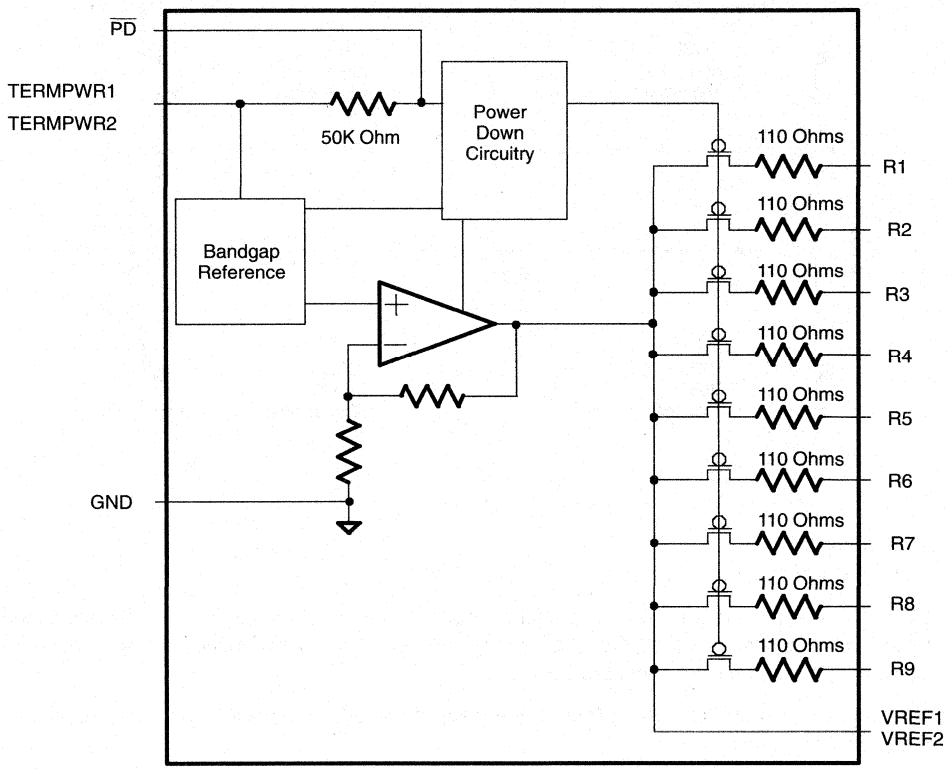
The SCSI-2 and SCSI–3 standards recommend the use of active terminations at both ends of every cable segment in a SCSI system with single-ended drivers and receivers. The DS2105 SCSI Terminator, which is fully compliant with these standards, enables the designer to gain the benefits of active termination: greater immunity to voltage drops on the TERMPWR (TERMination PoWeR) line, enhanced high-level noise immunity, intrinsic TERMPWR decoupling, and very low quiescent current consumption. The DS2105, which integrates a regulator and nine precise switched 110 ohm termination resistors into a monolithic IC, is a functionally compatible version of the DS21S07A. With relaxed output current and termination tolerances, the DS2105 is intended for high volume applications which require active termination but not the high performance of the DS21S07A. The DS2105 is offered in both 300 mil and 150 mil SOIC packages.

FUNCTIONAL DESCRIPTION

The DS2105 consists of a bandgap reference, buffer amplifier, and nine termination resistors (Figure 1). The bandgap reference circuit produces a precise 2.55V level which is fed to a buffer amplifier. The buffer produces a 2.85V level and is capable of sourcing at least 24 mA into each of the termination resistors when the signal line is low (active). When the driver for a given signal line turns off, the terminator will pull the signal line to 2.85V (quiescent state). To handle actively negated SCSI signals, the buffer can sink 200 mA. When all lines settle in the quiescent state, the regulator will consume about 5 mA. When the DS2105 is put into power-down mode by bringing $\overline{PD}$ low, the power-down circuitry will turn off the transistors on each signal line. This will isolate the DS2105 from the signal lines and effectively remove it from the circuit. The power-down pin ($\overline{PD}$) has an internal 50K ohm pull-up resistor. To place the DS2105 into an active state, the $\overline{PD}$ pin should be left open circuited.

To ensure proper operation, both the TERMPWR1 and TERMPWR2 pins must be connected to the SCSI bus TERMPWR line and both the VREF1 and VREF2 pins must be tied together externally. Each DS2105 requires a 4. 7 µF capacitor connected between the VREF pins and ground. Figure 2 details a typical SCSI bus configuration. In an 8-bit wide SCSI bus arrangement ("A" Cable), two DS2105's would be needed at each end of the SCSI cable in order to terminate the 18 active signal lines. In a 16-bit wide SCSI bus arrangement ("P" Cable), three DS2105's would be needed at each end of the SCSI cable in order to terminate the 27 active signal lines.

DS2105 BLOCK DIAGRAM Figure 1



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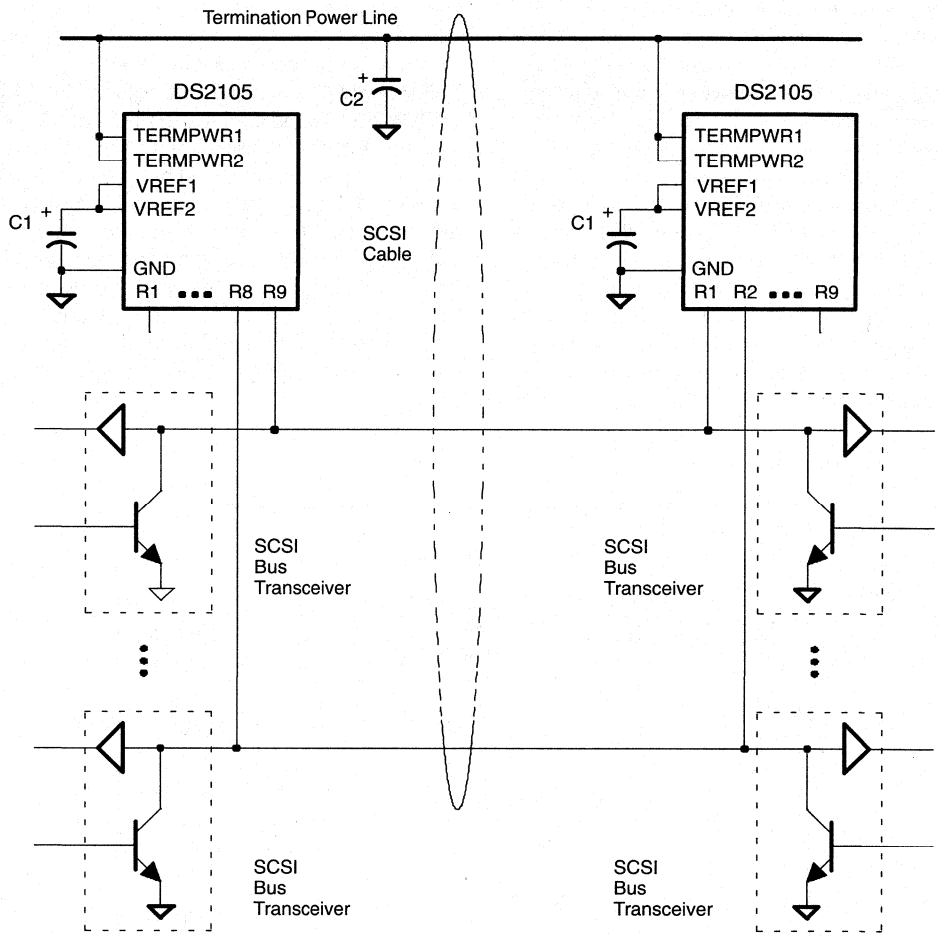
TYPICAL SCSI BUS CONFIGURATION Figure 2



NOTES:

1. C1 = 4.7 µF tantalum
   C2 = 2.2 µF tantalum or 4.7 µF aluminum
2. If the DS2105 is to be embedded into a peripheral that will act as a target on a SCSI bus, it is recommended that TERMPWR be derived from the SCSI cable, not generated locally. In this configuration, if a power failure occurs in the peripheral, it will not affect the bus.
3. A high frequency bypass capacitor (0.1 µF recommended) can be added in parallel to C1 for applications using fast rise/fall time drivers.

PIN DESCRIPTION Table 1

DS2105S PIN	DS2105Z PIN	SYMBOL	DESCRIPTION
1	1	TERMPWR1	**Termination Power 1.** Should be connected to the SCSI TERMPWR line. Must be decoupled with either a 2.2 µF or 4.7 µF. See Figure 2.
2	2	R1	**Signal Termination 1.** 110 ohm termination.
3	3	R2	**Signal Termination 2.** 110 ohm termination.
4	4	R3	**Signal Termination 3.** 110 ohm termination.
5	5	R4	**Signal Termination 4.** 110 ohm termination.
6	6	R5	**Signal Termination 5.** 110 ohm termination.
7	7	VREF1	**Reference Voltage 1.** Must be externally connected directly to the VREF2 pin. Must be decoupled with a 4.7 µF capacitor as shown in Figure 2.
8	8	GND	**Ground.** Signal ground; 0.0V.
9	9	TERMPWR2	**Termination Power 2.** Should be connected to the SCSI TERMPWR line. Must be decoupled with either a 2.2 µF or 4.7 µF. See Figure 2.
10	11	R6	**Signal Termination 6.** 110 ohm termination.
11	12	R7	**Signal Termination 7.** 110 ohm termination.
12	13	R8	**Signal Termination 8.** 110 ohm termination.
13	14	R9	**Signal Termination 9.** 110 ohm termination.
15	15	VREF2	**Reference Voltage 2.** Must be externally connected directly to the VREF1 pin. Must be decoupled with a 4.7 µF capacitor as shown in Figure 2.
16	16	$\overline{PD}$	**Power Down.** When tied low, the DS2105 enters a power-down mode. Contains an internal 50K pull-up. Strap low to deactivate the DS2105, leave open circuited to activate the DS2105.
14	10	NC	**No Connect.** Do not connect any signal to this pin.

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to 125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TERMPWR Voltage	V_{TP}	4.00		5.25	V	
$\overline{PD}$ Active	V_{PDA}	-0.3		0.8	V	
$\overline{PD}$ Inactive	V_{PDI}	2.0		V_{TP} +0.3	V	

DC CHARACTERISTICS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TERMPWR Current	I_{TP}			250	mA	1,3
	I_{TP}		5	8	mA	1,4
Power Down Current	I_{PD}		500		µA	1,2,5
Termination Resistance	R_{TERM}	104.5	110	115.5	ohms	1,2
Die Thermal Shutdown	T_{SD}		150		°C	1
Power Down Termination Capacitance	C_{PD}		3.0	4.5	pF	1,2,5,6
Input Leakage High	I_{IH}	−1.0			µA	1,8
Input Leakage Low	I_{IL}			1.0	µA	1,7

REGULATOR CHARACTERISTICS

(0°C to 70°C)

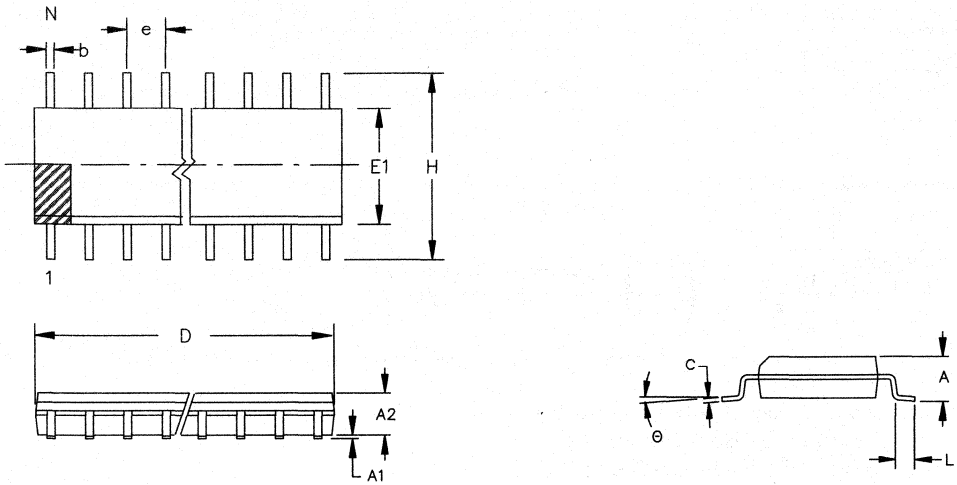
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Voltage	V_{REF}	2.71	2.85	2.99	V	1,2
Drop Out Voltage	V_{DROP}		0.75	1.0	V	3,6
Output Current	I_{OUT}			24.0	mA	9
Line Regulation	LI_{REG}		1.0	2.0	%	1,4
Load Regulation	LO_{REG}		1.3	3.0	%	1,2
Current Limit	I_{LIM}	300		450	mA	1
Sink Current	I_{SINK}	200			mA	1

NOTES:

1. 4.00V < TERMPWR < 5.25V.
2. 0.0V < signal lines < 3.0V.
3. All signal lines = 0.0V.
4. All signal lines open.
5. $\overline{PD}$ = 0.0V.

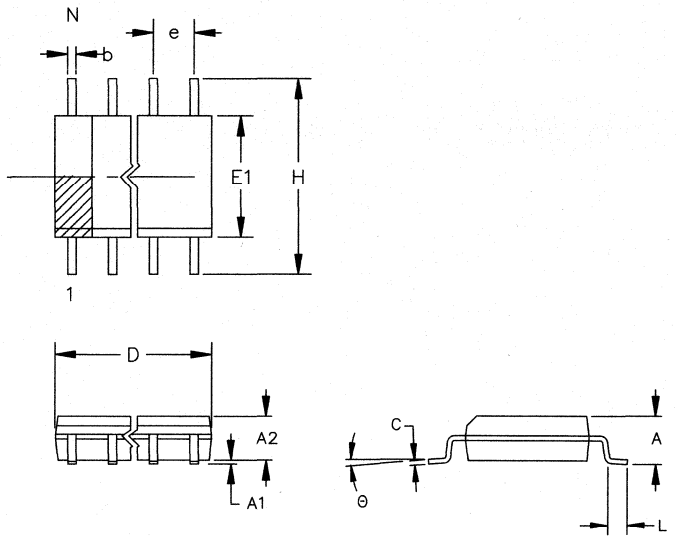
6. Guaranteed by design; not production tested.
7. R_1 through R_9 only.
8. R_1 through R_9 and $\overline{PD}$.
9. V_{SIGNAL}=0.2V.

DS2105Z SCSI TERMINATOR 16-PIN SOIC (150 MIL)



PKG	16-PIN	
DIM	MIN	MAX
A IN. MM	0.053 1.35	0.069 1.75
A1 IN. MM	0.004 0.10	0.010 0.25
A2 IN. MM	0.048 1.24	0.062 1.57
b IN. MM	0.012 0.30	0.020 0.50
C IN MM	0.007 0.17	0.011 0.28
D IN. MM	0.386 9.80	0.393 9.98
e IN. MM	0.050 BSC 1.27 BSC	
E1 IN. MM	0.150 3.81	0.158 4.01
H IN. MM	0.230 5.84	0.244 6.20
L IN. MM	0.016 0.40	0.050 0.89
Θ	0°	8°

DS2105S SCSI TERMINATOR 16-PIN SOIC (300 MIL)



The chamfer on the body is optional. If it is not present, a terminal 1 identifier must be positioned so that 1/2 or more of its area is contained in the hatched zone.

PKG	16-PIN	
DIM	MIN	MAX
A IN. MM	0.094 2.38	0.105 2.68
A1 IN. MM	0.004 0.102	0.012 0.30
A2 IN. MM	0.089 2.26	0.095 2.41
b IN. MM	0.013 0.33	0.020 0.51
C IN MM	0.009 0.229	0.013 0.33
D IN. MM	0.398 10.11	0.412 10.46
e IN. MM	.050 BSC 1.27 BSC	
E1 IN. MM	0.290 7.37	0.300 7.62
H IN MM	0.398 10.11	0.416 10.57
L IN MM	0.016 0.40	0.040 1.02
Θ	0°	8°

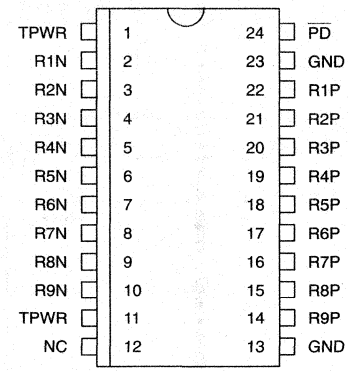
DALLAS SEMICONDUCTOR

DS2108
Differential SCSI Switchable Terminator

FEATURES

- Fully compliant with SCSI, SCSI–2 and SCSI–3 standards
- Conforms to EIA RS–485 standard
- Provides differential termination for 9 pairs of signal lines
- Operates with SCSI signal voltages of –7 to +12 Volts
- Laser–trimmed 330 and 150 ohm termination resistors have ±5% tolerance over full temperature range
- Switchable power down mode
- Low power down capacitance of 6 pF
- 24–pin plastic SOIC (DS2108S)

PIN ASSIGNMENT



DS2108S 24–PIN SOIC (300 MIL)

DESCRIPTION

The DS2108 SCSI Terminator has been specifically designed for Differential SCSI systems requiring switchable termination. The DS2108 integrates eighteen 330 ohm and nine 150 ohm precise switched termination resistors into a monolithic IC. The surface mount SOIC package saves board space over conventional resistor SIPs. The termination resistors can be isolated from the SCSI bus under software or hardware control. While in the powered down mode, the DS2108 isolates the 9 terminator blocks from the bus while adding only 6 pF capacitance to each signal line of the SCSI bus.

FUNCTIONAL DESCRIPTION

The DS2108 consists of power down circuitry, eighteen 330 ohm and nine 150 ohm termination resistors (Figure 1). The DS2108 can be removed from the circuit by bringing the power down pin ($\overline{PD}$) low. The power down capacitance on the terminating resistors is 6 pF, well below the SCSI–3 allotment of 25 pF. The DS2108 supports SCSI signal voltages of –7 to +12 volts when powered on or off. When all lines settle into the quiescent state (no signal transitions), 56 mA is typically consumed. Only 1 mA is typically consumed in the powered down mode.

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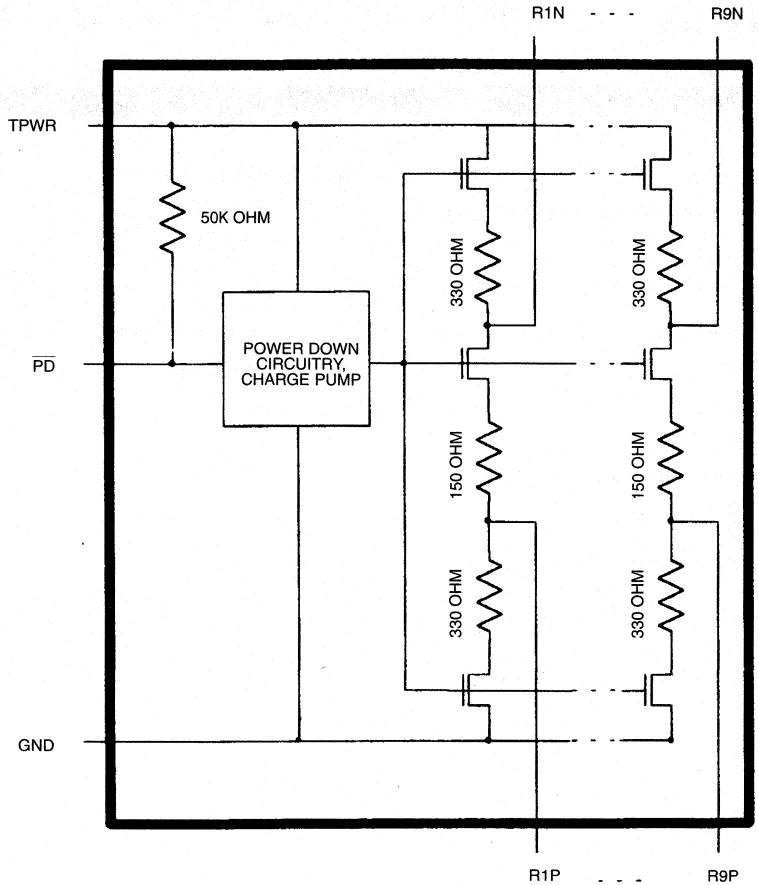
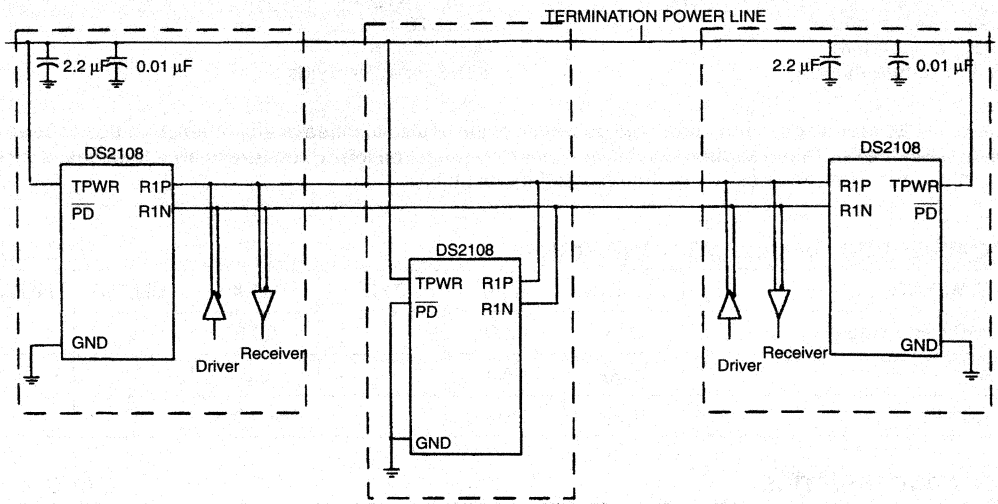
DS2108 BLOCK DIAGRAM Figure 1



TYPICAL DIFFERENTIAL SCSI BUS CONFIGURATION Figure 2



NOTES:

1. Two DS2108s required per 8–bit SCSI device and three DS2108s per 16–bit SCSI device.
2. Mid–bus termination effectively removed by grounding $\overline{PD}$ pin.
3. Termination power to be provided as specified in SCSI–3 Parallel Interface (SPI) document.
4. Local TERMPWR bypassing is recommended by the SPI document with values shown. The bypass capacitors should be located as close as possible to the DS2108s. Only one pair of capacitors is required per SCSI device (may be shared between DS2108s on same device).

PIN DESCRIPTION Table 1

PIN	SYMBOL	DESCRIPTION
1, 11	TPWR	Termination Power. Should be connected to the SCSI TERMPWR line. Bypass with a 2.2 µF cap in parallel with a 0.1 µF cap as shown in Figure 2.
2, 3, 4, 5, 6, 7, 8, 9, 10	R1N. . .R9N	Signal Termination Negative. Connect to –SIGNAL of SCSI bus.
12	NC	No Connect. Do not connect any signal to this pin.
13, 23	GND	Ground. Signal ground; 0.0V.
14, 15, 16, 17, 18, 19, 20, 21, 22	R1P...R9P	Signal Termination Positive. Connect to +SIGNAL of SCSI bus.
24	$\overline{PD}$	Power Down. When tied low, the DS2108 enters a power–down mode. Contains an internal 50K pullup. Strap low to deactivate the DS2108, leave open circuited to activate the DS2108.

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–7.0V to +12.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to 125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TERMPWR Voltage	V_{TP}	4.00		5.25	V	
$\overline{PD}$ Active	V_{PDA}	–0.3		0.8	V	
$\overline{PD}$ Inactive	V_{PDI}	2.00		V_{TP}+0.3	V	

DC CHARACTERISTICS

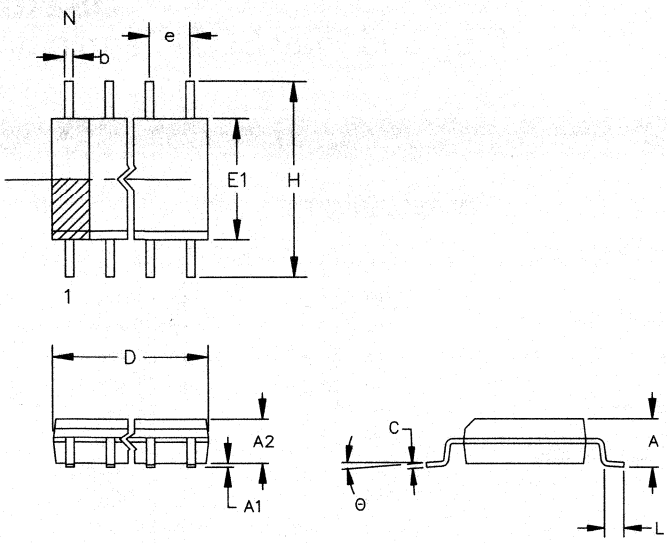
(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TERMPWR Current	I_{TP}		56	65	mA	1, 6
Power Down Current	I_{PD}		1	2	mA	1, 5
Termination Resistance	R_{TTN}	313.5	330	346.5	ohms	2
Termination Resistance	R_{TNP}	142.5	150	157.5	ohms	3
Termination Resistance	R_{TPG}	313.5	330	346.5	ohms	4
Power Down Termination Capacitance	C_{PD}		5	6	pF	1, 5, 7

NOTES:

1. 4.00V < TERMPWR < 5.25V
2. 330 Ω resistor between TERMPWR and –SIGNAL.
3. 150 Ω resistor between –SIGNAL and +SIGNAL.
4. 330 Ω resistor between +SIGNAL and GDN.
5. $\overline{PD}$ = 0.0V.
6. Signal pins left open.
7. Guaranteed by design; not production tested.

24–PIN SOIC (300 MIL)



The chamfer on the body is optional. If it is not present, a terminal 1 identifier must be positioned so that 1/2 or more of its area is contained in the hatched zone.

PKG	24-PIN	
DIM	MIN	MAX
A IN. MM	0.094 2.38	0.105 2.68
A1 IN. MM	0.004 0.102	0.012 0.30
A2 IN. MM	0.089 2.26	0.095 2.41
b IN. MM	0.013 0.33	0.020 0.51
C IN MM	0.009 0.229	0.013 0.33
D IN. MM	0.598 15.19	0.612 15.54
e IN. MM	.050 BSC 1.27 BSC	
E1 IN. MM	0.290 7.37	0.300 7.62
H IN MM	0.398 10.11	0.416 10.57
L IN MM	0.016 0.40	0.040 1.02
Θ	0°	8°

9

PRELIMINARY

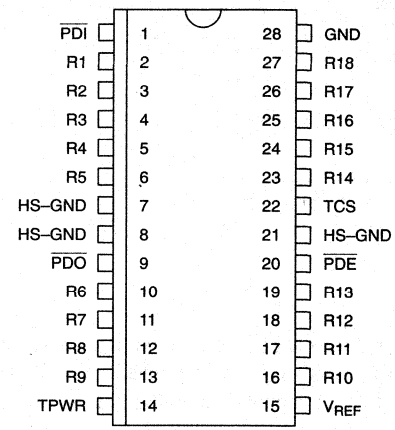
DALLAS SEMICONDUCTOR

DS2109
Plug and Play SCSI Terminator

FEATURES

- Fully compliant with SCSI, SCSI–2 and SCSI–3 standards
- Compatible with Plug and Play SCSI Specification
- Functionally compatible with DS21S07A
- Provides active termination for 18 signal lines
- 2% tolerance on termination resistors and voltage regulator
- Bus termination sensing
- Low power down capacitance of 3 pF
- Onboard thermal shutdown circuitry

PIN ASSIGNMENT



DS2109 28–PIN SOIC (300 MIL)

DESCRIPTION

The DS2109 is intended for one chip Plug and Play (PnP) SCSI termination. Plug and Play SCSI requires the exit–point terminator on computer motherboards or host bus adapters to automatically switch off if an external device is connected to the system. The DS2109 satisfies this requirement by offering the engineer a choice of onboard current sensing circuitry or onboard ground detect circuitry. If an external device is connected, the DS2109 will automatically be isolated from the SCSI bus thereby maintaining proper system termination.

The DS2109 integrates a low drop–out regulator, 18 precise switched 110 ohm termination resistors, and bus termination sensors into a 28–pin 300 mil SOIC package. Active termination provides: greater immunity to voltage drops on the TERMPWR (TERMination PoWeR) line, enhanced high–level noise immunity, intrinsic TERMPWR decoupling, and very low quiescent current consumption. The DS2109 contains an output port that can control the power down pin of additional terminators (DS21S07A) for Wide SCSI applications.

REFERENCE DOCUMENTS

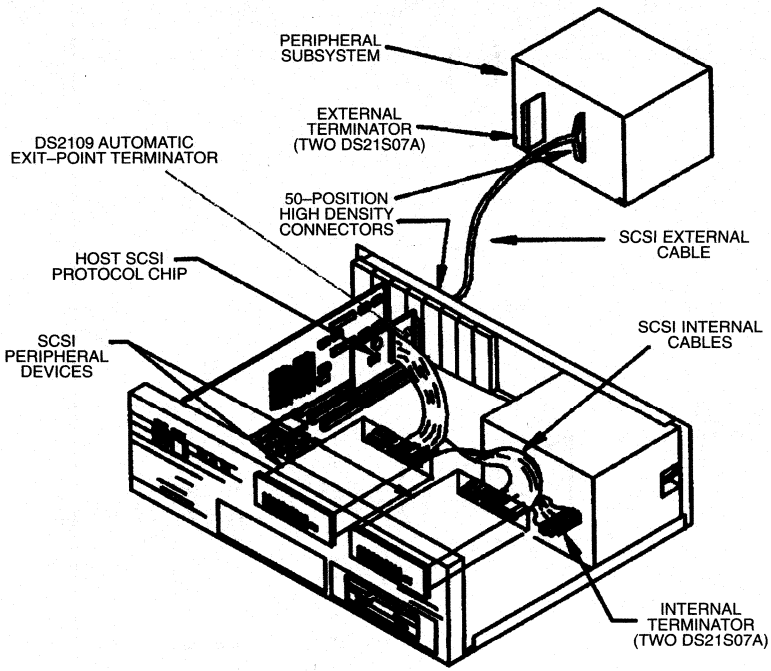
SCSI–2 (X3.131–1994)
SCSI–3 Parallel Interface (X3T10/855D)
Available from: Global Engineering Documents
15 Inverness Way East
Englewood, CO 80112–5704
Phone: (800) 854–7179,(303) 792–2181
Fax: (303) 792–2192

PnP SCSI Specification
PnP ISA Specification
PnP BIOS Specification
PnP Option ROM Specification
Available from: Plug and Play forum on
CompuServe (Go plugplay).

FUNCTIONAL DESCRIPTION

The DS2109 is designed to be a single chip termination subsystem for use in PnP SCSI systems, Figure 1. When embedded on a host bus adapter or motherboard, the DS2109 can automatically sense the termination status of the SCSI bus and attach or isolate its resistors as needed to maintain proper bus termination. External and internal active termination can be provided by the DS21S07A.

DS2109 APPLICATION ENVIRONMENT Figure 1



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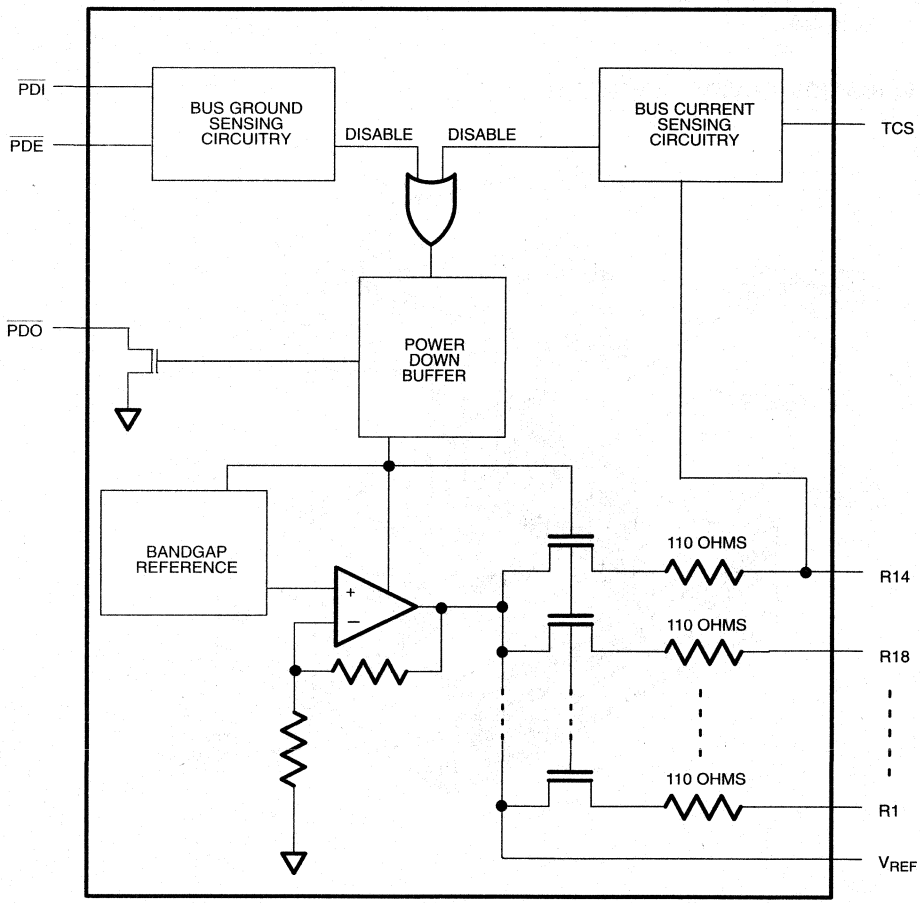
The DS2109 consists of 3 major functional blocks, Figure 2:

- Voltage reference, terminating resistors, and isolation switches
- Bus current sensing circuitry
- Bus ground sensing circuity

When the Bus Ground Sensing Circuitry or Bus Current Sensing Circuitry determine that the SCSI bus is properly terminated without the DS2109, the power down buffer isolates the resistors from the SCSI bus and disables the power amp, thereby placing the DS2109 in a low power mode (the bus sensing circuitry always stays active). The $\overline{PD}$ (Power Down Output) pin can be connected to the pin of a DS21S07A SCSI terminator for Wide SCSI configurations, Figure 8.

DS2109 BLOCK DIAGRAM Figure 2



DETAILED PIN DESCRIPTION Table 1

PIN	SYMBOL	FCN	DESCRIPTION
1	$\overline{PDI}$	I	**Power Down Internal.** For Bus Ground Sensing Circuit connect to pin 22 of internal SCSI connector, see Figure 4.
2–6, 10–13, 16–19, 24–27	R1...R13 R15...18	T	**Signal Termination.** 110 ohm termination. Connect to SCSI bus signal lines. For Bus Current Sensing Circuit connect to data, parity, and control lines, except SCSI–RST line, see Figure 6.
7, 8, 21	HS–GND	P	**Heat Sink Ground.** Internally connected to the mounting pad. Should be either grounded or electronically isolated from other circuitry.
9	$\overline{PDO}$	O	**Power Down Output.** Connect to DS21S07A for Wide SCSI applications, see Figure 8.
14	TPWR	P	**Termination Power.** Connect to the SCSI TERMPWR line. Bypass with a 2.2 µF capacitor, see Figures 4 and 6.
15	V_{REF}	O	**Reference Voltage.** 2.85 volt reference; must be decoupled with a 4.7 µF capacitor, see Figures 4 and 6.
20	$\overline{PDE}$	I	**Power Down External.** For Bus Ground Sensing Circuit, connect to pin 36 of external SCSI connector, see Figure 4.
22	TCS	I	**Termination Current Sense.** Used to sense current on the SCSI bus. For Bus Current Sensing Circuit, connect to SCSI signal line –RST, see Figure 6.
23	R14	T	**Signal Termination.** 110 ohm termination. Connect to SCSI bus signal line. For Bus Current Sensing Circuit connect to SCSI controller chip, see Figure 6.
28	GND	P	**Ground.** Signal ground; 0.0 volts.

ACTIVE TERMINATION

The voltage regulator circuitry (bandgap reference and class AB power amplifier) produces a precise laser–trimmed 2.85 volt level and is capable of sourcing 24 mA into each of the terminating resistors when the signal line is low (active). When the external driver for a given signal line turns off, the active terminator will pull that signal line to 2.85 volts (quiescent state). When used with an active negation driver, the power amp can sink 22 mA per line while keeping the voltage reference in regulation; the terminating resistors maintain their 110 W value over the entire voltage range. To maintain the specified regulation, a 4.7 µF capacitor is required between the V_{REF} pin and ground. A high frequency cap (0.1 µF ceramic recommended) can also be placed on the V_{REF} pin in applications that use fast rise/fall time drivers. The power down capacitance on terminating resistors R1–R13 and R15–R18 is <4 pF; R14 is slightly higher due to the bus current sensing circuitry.

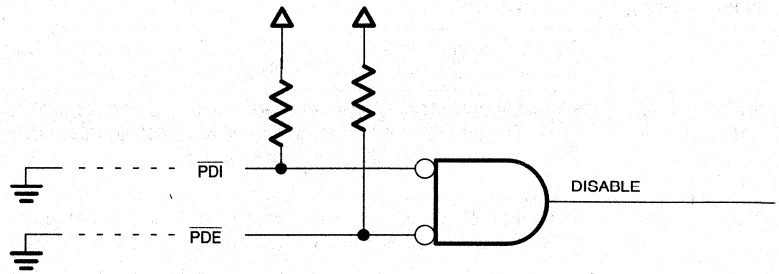
The DS2109 can be removed from the SCSI bus by using either of two automatic methods, Bus Ground Sensing or Bus Current Sensing.

As with all analog circuitry, the TERMPWR lines should be bypassed locally. A 2.2 µF capacitor is recommended between TPWR and ground and placed as close as possible to the DS2109. The DS2109 should be placed as close as possible to the connector to minimize signal and power trace length, thereby resulting in less input capacitance and reflections which can degrade the bus signals.

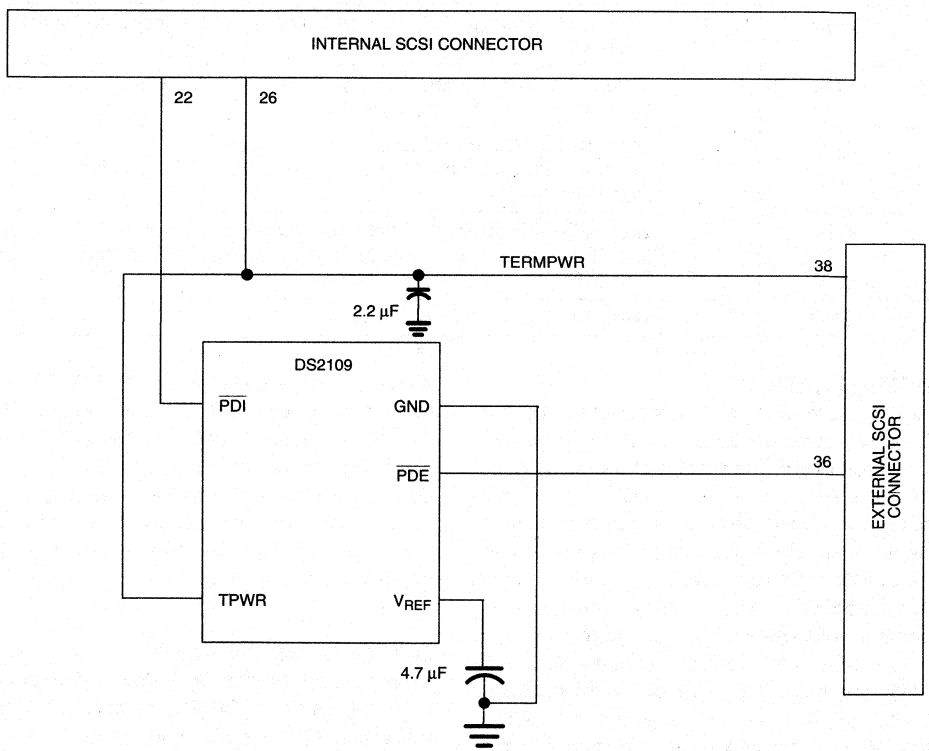
BUS GROUND SENSING

If internal and external SCSI devices are connected to the SCSI bus, the DS2109 will disconnect from the SCSI bus according to the circuit in Figure 3. To utilize this automatic disconnect method of bus sensing, configure the DS2109 as shown in Figure 4. The $\overline{PDI}$ (Power Down Internal) pin should be connected to pin 22 of the internal SCSI connector, and the $\overline{PDE}$ (Power Down External) connected to pin 36 of the external SCSI connector.

BUS GROUND SENSING CIRCUIT Figure 3



BUS GROUND DETECT CONFIGURATION Figure 4



BUS CURRENT SENSING

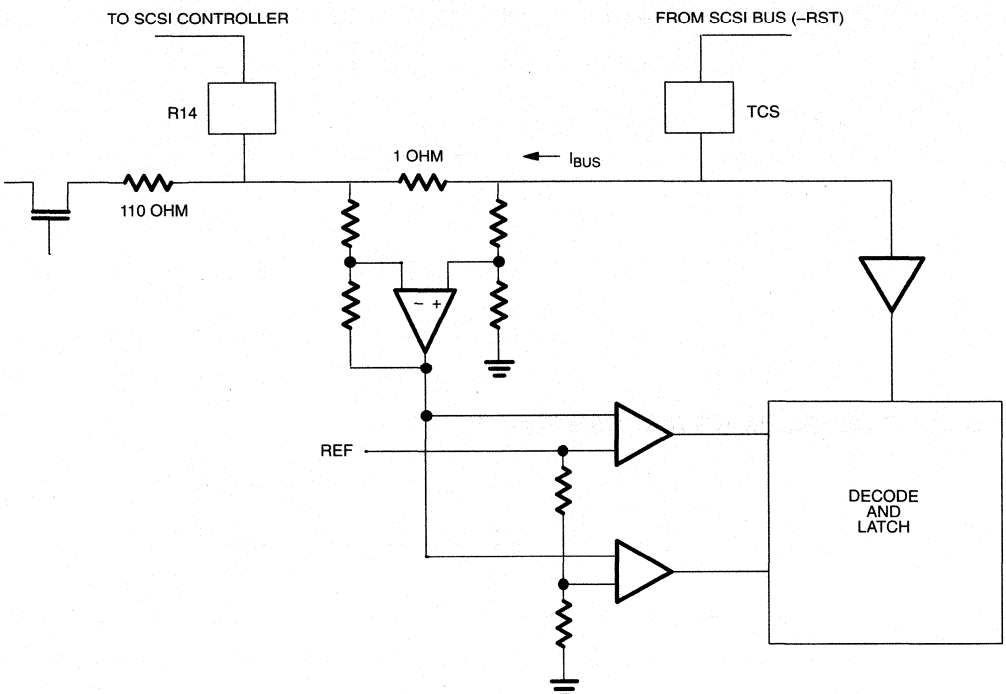
The DS2109 has the capability to use current sensing to determine if the SCSI bus is over– or under–terminated. A series 1 ohm resistor between pads R14 and TCS is inserted into the SCSI bus (preferably the –RST line) and used to monitor the current when that line pulls low (active, or "asserted" state). Based on the current measured, the DS2109 will disconnect or connect from the SCSI bus. The configuration for this automatic isolation technique is shown in Figure 6.

Figure 5 shows a simplified diagram of the sensing circuit. The voltage across the 1 ohm sense resistor is differentially amplified and converted into a single–ended voltage with respect to ground. This is fed into a bank of comparators and measured against a reference voltage. The circuit takes a measurement each time TCS is driven below a 0.8 volts threshold and the outputs are latched on the rising edge of TCS. If I_{BUS} is greater than 32 mA, the DS2109 will be isolated from the SCSI bus. It is recommended that the signal on TCS be asserted for at least 25 msec to allow the signal (and comparator outputs) to settle into a known state. A timing diagram of the sensing and latching operation is shown in Figure 7.

It is preferred that the –RST line be used for monitoring the bus termination status because –RST is only asserted during power up or during a major change in bus configuration. Note that R14 will have a higher input capacitance than the other lines because of the additional circuitry required for bus sensing.

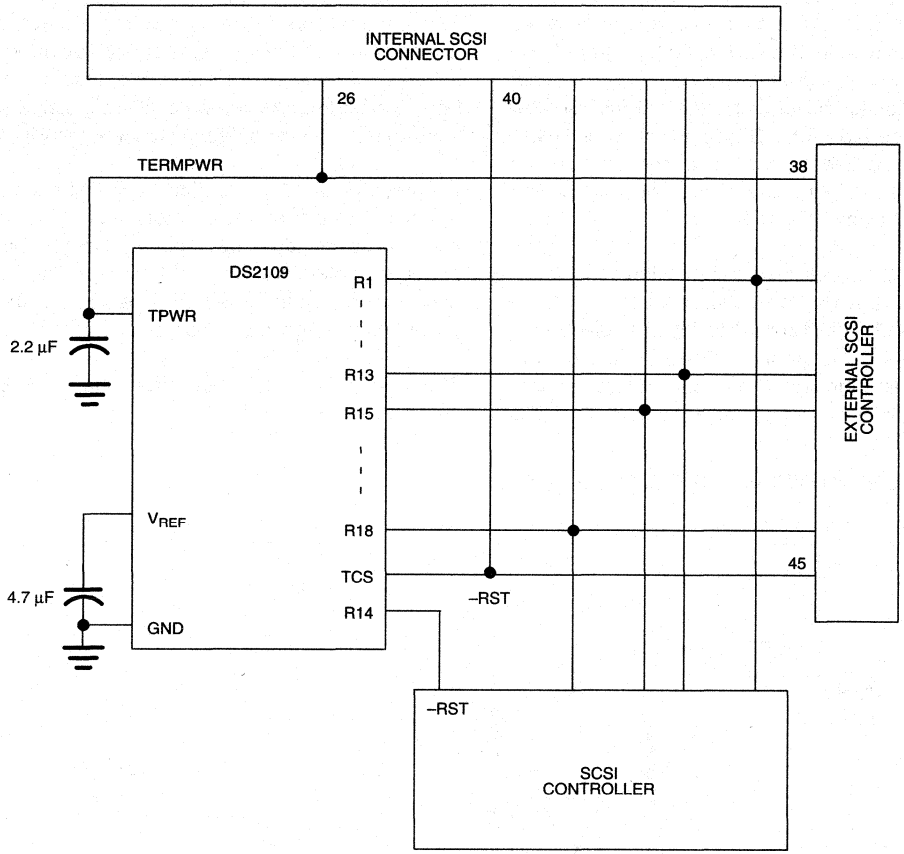
The DS2109 will be isolated from the SCSI bus as shown in Table 2.

BUS CURRENT SENSING CIRCUITRY Figure 5

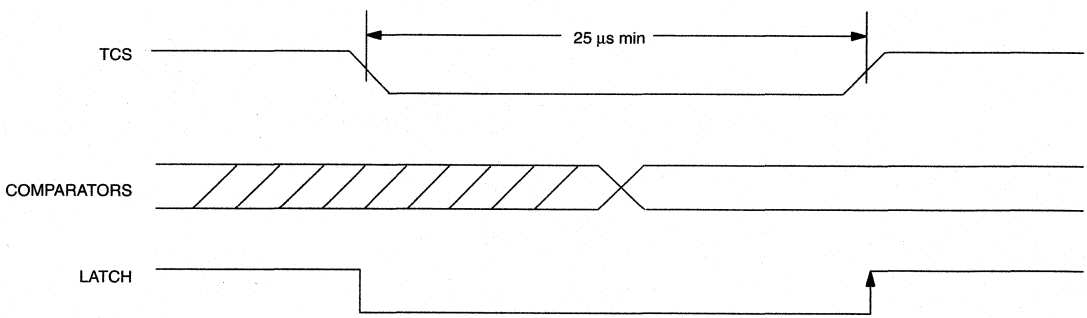


9

BUS CURRENT SENSE CONFIGURATION Figure 6



BUS CURRENT SENSE TIMING DIAGRAM Figure 7

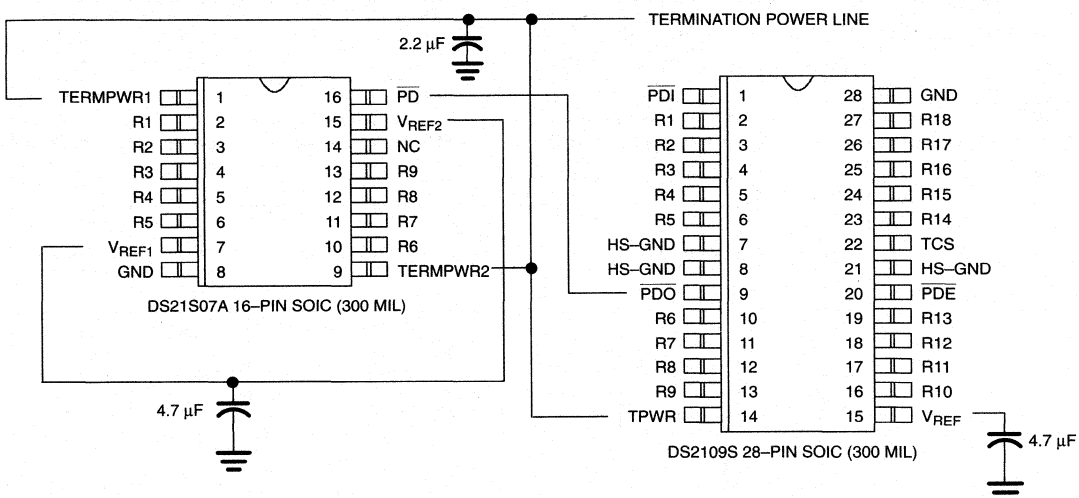


DISCONNECT MODES Table 2

$\overline{PDI}$	$\overline{PDE}$	I_{BUS} > 32 mA?	DS2109 ISOLATED FROM SCSI BUS?
0	0	No	Isolated
0	1	No	Connected
1	0	No	Connected
1	1	No	Connected
0	0	Yes	Isolated
0	1	Yes	Isolated
1	0	Yes	Isolated
1	1	Yes	Isolated

NOTE: "1" denotes pin left open circuited.

WIDE SCSI CONFIGURATION Figure 8



9

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to 125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TERMPWR Voltage	V_{TP}	4.00		5.25	V	
Logic 1	V_{IH}	2.0		V_{TP}+0.3	V	1
Logic 0	V_{IL}	–0.3		+0.8	V	1

DC CHARACTERISTICS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TERMPWR Current	I_{TP} I_{TP}		 10	500 14	mA mA	2, 4 2, 5
Power Down Current	I_{PD}		1	2	mA	2, 3, 6
Termination Resistance	R_{TERM}	108	110	112	ohms	2, 3
Die Thermal Shutdown	TS_D		150		°C	2
Power Down Termination Capacitance	C_{PD} C_{14}		3 8	4.5 10	pF pF	2, 3, 6, 7 2,3,6,7,8
Input Leakage High	I_{IH}	–1.0			µA	2
Input Leakage Low	I_{IL}			1.0	µA	2, 9
Output Current	I_O	4			mA	10
Bus Current Sense Trip Point	I_{BCST}		32		mA	11

REGULATOR CHARACTERISTICS

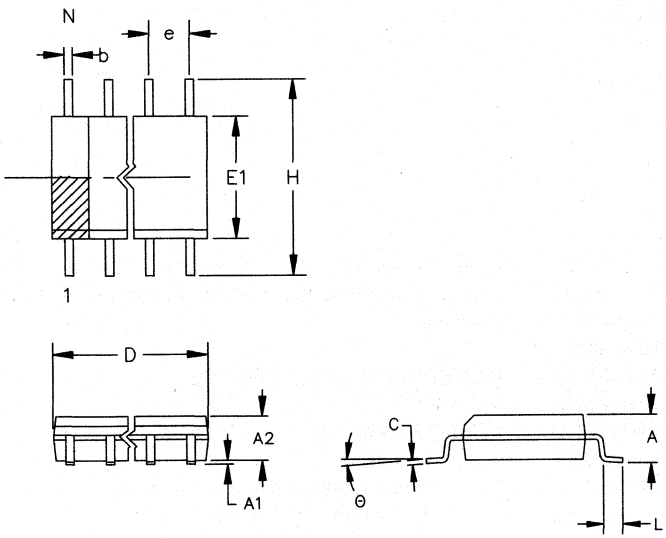
(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Voltage	V_{REF}	2.79	2.85	2.91	V	2, 3
Drop Out Voltage	V_{DROP}		0.75	1.0	V	4, 7
Line Regulation	LI_{REG}		1.0	2.0	%	2, 5
Load Regulation	LO_{REG}		1.3	3.0	%	2, 3
Current Limit	I_L	600	700	800	mA	2
Sink Current	I_{SINK}		400		mA	2

NOTES:

1. $\overline{PDI}$, $\overline{PDE}$, TCS
2. 4.00V < TERMPWR < 5.25V.
3. 0.0V < signal lines < 3.0V.
4. All signal lines = 0.0V.
5. All signal lines open.
6. Power down enabled.
7. Guaranteed by design; not production tested.
8. C_{14} slightly higher capacitance due to sensing circuitry.
9. Excluding $\overline{PDI}$, $\overline{PDE}$ pins.
10. $\overline{PDO}$ output pin.
11. I_{BCST} > 32 mA – disable termination.

28–PIN SOIC (300 MIL)



The chamfer on the body is optional. If it is not present, a terminal 1 identifier must be positioned so that 1/2 or more of its area is contained in the hatched zone.

PKG	28-PIN	
DIM	MIN	MAX
A IN. MM	0.094 2.39	0.105 2.67
A1 IN. MM	0.004 0.102	0.012 0.30
A2 IN. MM	0.089 2.26	0.095 2.41
b IN. MM	0.013 0.33	0.020 0.51
C IN MM	0.009 0.229	0.013 0.33
D IN. MM	0.698 17.73	0.712 18.08
e IN. MM	.050 BSC 1.27 BSC	
E1 IN. MM	0.290 7.37	0.300 7.62
H IN MM	0.398 10.11	0.416 10.57
L IN MM	0.016 0.40	0.040 1.02
Θ	0°	8°

9

PRODUCT PREVIEW

DALLAS SEMICONDUCTOR

DS2110
Plug and Play SCSI Terminator with EEPROM

FEATURES

- Fully compliant with SCSI, SCSI–2 and SCSI–3 standards
- Compatible with Plug and Play SCSI Specification
- Functionally compatible with DS21S07A
- Provides active termination for 18 signal lines
- 2% tolerance on termination resistors and voltage regulator
- 4–wire microcontroller interface
- Intelligent bus termination sensing and control
- Terminator status register
- 1K/2K/4K bits EEPROM
- Low power down capacitance of 3 pF

PIN ASSIGNMENT

PINOUT AND PACKAGE TBD

DESCRIPTION

The DS2110 is intended for one chip Plug and Play (PnP) SCSI termination. Plug and Play SCSI requires the exit–point terminator on computer motherboards or host bus adapters to automatically switch off if an external device is connected to the system. The DS2110 satisfies this requirement with onboard current sensing circuitry. If an external device is connected, the DS2110 will automatically be isolated from the SCSI bus thereby maintaining proper system termination. The DS2110 integrates a low drop–out regulator, 18 precise switched 110 ohm termination resistors, a microprocessor interface, bus termination sensor, and EEPROM into a TBD package. Active termination provides: greater immunity to voltage drops on the TERMPWR (TERMination PoWeR) line, enhanced high–level noise immunity, intrinsic TERMPWR decoupling, and very low quiescent current consumption. The DS2110 contains an output port that can control the power down pin of additional terminators (DS21S07A) for Wide SCSI applications. 1K, 2K or 4K bits of EEPROM is included to store Plug and Play register parameters. An external microcontroller can access the EEPROM as well as control and monitor the status of the terminator via a 4–wire interface.

REFERENCE DOCUMENTS

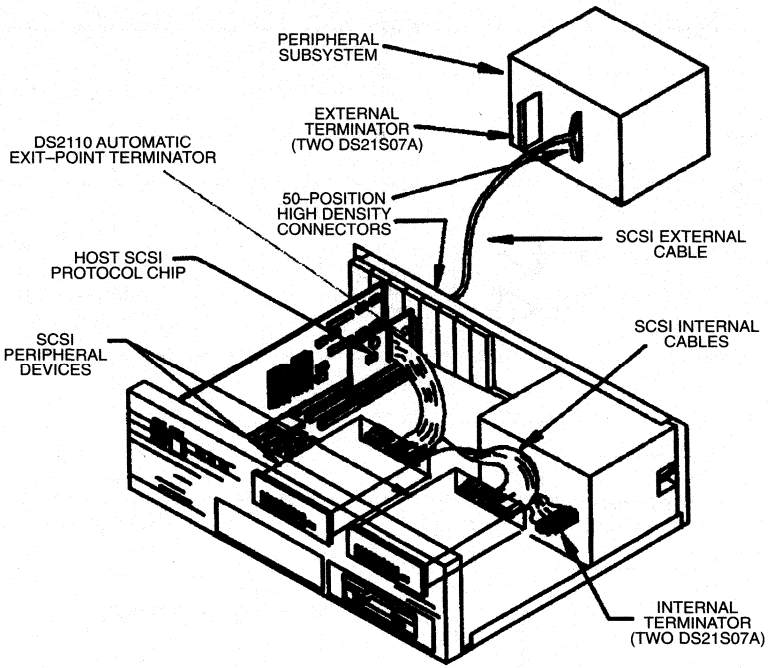
SCSI–2 (X3.131–1994)
SCSI–3 Parallel Interface (X3T10/855D)
Available from:
Global Engineering Documents
15 Inverness Way East
Englewood, CO 80112–5704
Phone: (800) 854–7179, (303) 792–2181
Fax: (303) 792–2192

PnP SCSI Specification
PnP ISA Specification
PnP BIOS Specification
PnP Option ROM Specification
Available from:
Plug and Play forum on CompuServe
(Go plugplay)

FUNCTIONAL DESCRIPTION

The DS2110 is designed to be a single chip termination subsystem for use in PnP SCSI systems. (See Figure 1.) When embedded on a host bus adapter or motherboard, the DS2110 can automatically sense the termination status of the SCSI bus and attach or isolate its resistors as needed to maintain proper bus termination. External and internal active termination can be provided by the DS21S07A.

DS2110 APPLICATION ENVIRONMENT Figure 1



The DS2110 consists of 4 major functional blocks as illustrated in Figure 2:

- Voltage reference, terminating resistors, and isolation switches
- Bus sensing circuitry
- EEPROM
- Microcontroller interface and status register

The power down mode isolates the resistors from the SCSI bus and disables the power amp, thereby placing the DS2110 in a low power mode (the bus sensing circuitry always stays active). The power down mode can be entered either by strapping (Power Down Input Output) low or via the control register under software command. The pin is dominant over the control register; therefore, to enable software control, the pin must be left open. The pin can also be connected to the pin of a DS21S07A SCSI terminator for Wide SCSI configurations. (See Figure TBD.)

The microcontroller interface allows access to several unique features of the DS2110:

- Power up/down the DS2110 to attach/isolate the terminator to/from the bus
- Enable auto–termination mode
- Write/read EEPROM registers
- Determine bus termination status
- Query the port to read DS2110 status register

A simple 4–wire serial interface is used to communicate with a microcontroller.

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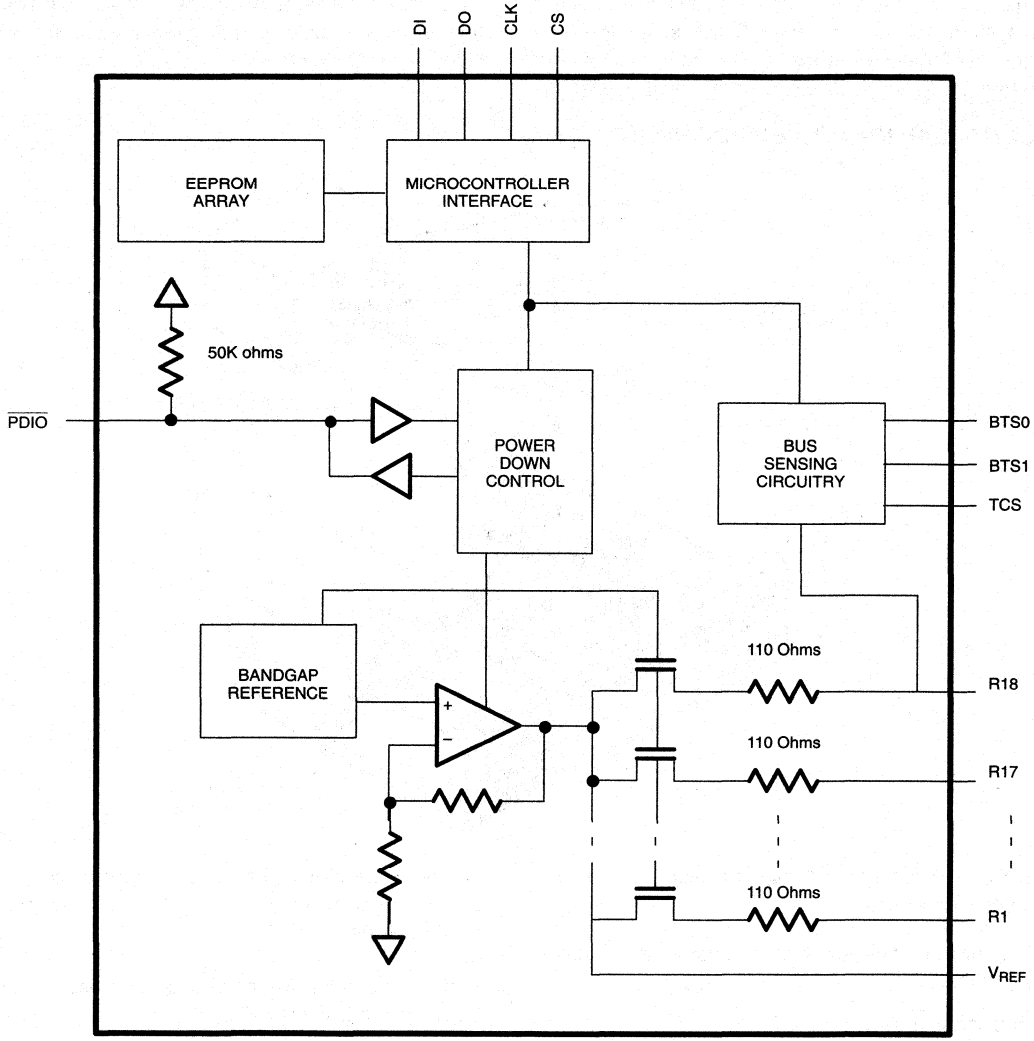
DS2110 BLOCK DIAGRAM Figure 2



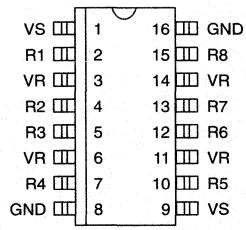
DALLAS SEMICONDUCTOR

DS2112
BTL Terminator

FEATURES

- Complies with Backplane Transceiver Logic (BTL) specifications (IEEE 1194.1–1991) and Futurebus+ specifications (IEEE 896.2–1991)
- Provides active termination for eight signal lines
- Laser–trimmed 33Ω termination resistors have 2.5% tolerance from 0°C to 70°C
- Onboard precise 2.1V (±2%) voltage regulator
- Package optimized for minimum parasitic inductance and resistance
- 16–pin (300 mil) plastic SOIC package

PIN ASSIGNMENT



16–PIN SOIC
(300 MIL)

DESCRIPTION

The DS2112 BTL Terminator provides active termination for Backplane Transceiver Logic (BTL) drivers and is fully compliant with IEEE 1194.1–1991, as well as the Futurebus+ specification (IEEE 896.2–1991). The DS2112 integrates a low dropout regulator and eight precision resistors into a single monolithic CMOS IC that is optimized for the high switching speeds and current required of BTL systems. The DS2112 allows the user to provide a distributed 2.1 volt supply that supports the instantaneous current required in incident wave switching while meeting the stringent ripple requirements of BTL without using a costly high speed specialized power supply.

FUNCTIONAL DESCRIPTION

The DS2112 consists of a bandgap reference, a power amplifier, and eight precise 33Ω terminating resistors (see Figure 1). The bandgap reference produces a laser–trimmed 1.26 volt source which is amplified to 2.1 volts and fed to the unity gain power amp. The power amp is capable of sourcing 41 mA into each of the eight terminating resistors when the signal line is driven low. When the driver releases the line, the terminator will pull it back to 2.1 volts. When all lines are in the quiescent state, the DS2112 consumes about 10 mA (V_S=5.0 volts). The DS2112 can operate with supply voltages as low as 4.0 volts and meet all BTL specifications.

Due to the high switching speeds and the amount of current that can be switched, layout and bypass capacitor placement is critical to the proper operation of the DS2112's regulator. The DS2112 die, pinout and package have been optimized to reduce parasitic inductance and resistance, thereby minimizing the effects of large di/dt. The V_S pins should be connected to the backplane power supply and bypassed with a 10 µA tantalum; the two sets of V_R pins are designed to be separately bypassed. The preferred configuration would be to tie pins 3 and 6 together and connect a 2 µF low ESR/ESL ceramic capacitor to ground; repeat this with pins 11 and 14. This balances out the currents in all the resistors, thereby minimizing parasitic resistances and inductances. The traces making all connections to the DS2112 should be as short as possible. A typical configuration for one DS2112 is shown in Figure 2.

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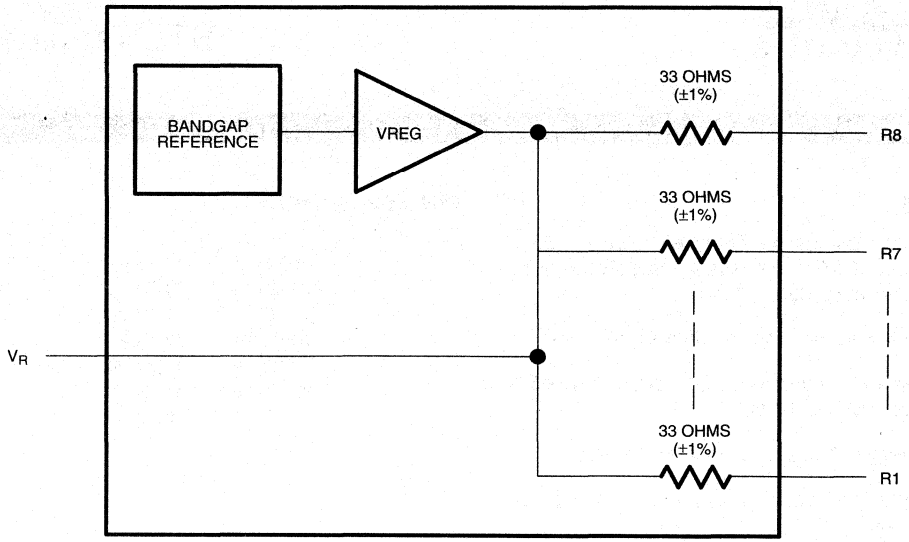
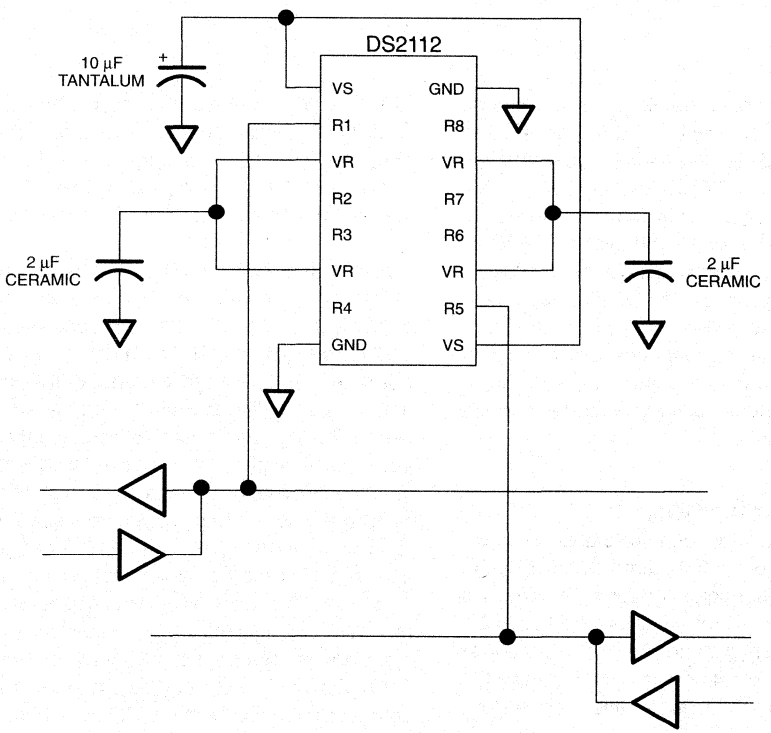
FUNCTIONAL BLOCK DIAGRAM Figure 1



TYPICAL CONFIGURATION Figure 2



PIN DESCRIPTION Table 1

PIN	SYMBOL	DESCRIPTION
1, 9	VS	**Power Supply**. Decouple with 10 µF tantalum, see Figure 2.
8, 16	GND	**Ground**. Signal ground; 0.0 volt.
3, 6	VR	**Reference Voltage**. Tie together and connect to 2 µF ceramic; see Figure 2.
11, 14	VR	**Reference Voltage**. Tie together and connect to 2 µF ceramic; see Figure 2.
2, 4, 5, 7, 10, 12, 13, 15	R	**Termination Resistor**. 33 ohm termination.

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–1.0V to 7.0V
Operating Temperature	0°C to +70°C
Storage Temperature	–55°C to 125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_S	4.0		5.5	V	

DC CHARACTERISTICS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{TP} I_{TP}			350 15	mA mA	1, 3 1, 4
Termination Resistance	R_{TERM}	32.18	33.00	33.82	Ω	1, 2

REGULATOR CHARACTERISTICS

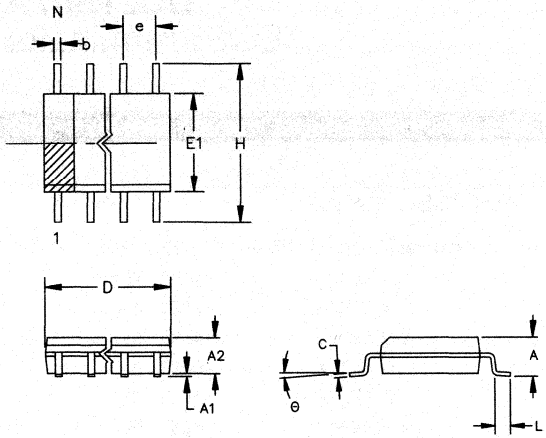
(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Voltage	V_R	2.058	2.100	2.142	V	1, 2
Load Regulation	LO_{REG}			2	%	1, 2, 5, 8
AC Ripple Voltage	V_{RIPPLE}	–50		+50	mV	1, 2, 5, 7
Regulation Time	T_{REG}			100	µs	6, 7
Input Capacitance	C_{IN}			5	pF	7

NOTES:

1. $4.0V < V_S < 5.5V$
2. 0.75V < signal lines < 2.0V
3. All signal lines = 0.75V.
4. All signal lines open.
5. R1 to R8 switching simultaneously between 1.0V and 2.0V with 2 ns rise/fall time.
6. Measured from the time V_S reaches 4.0V until V_R reaches regulation.
7. Guaranteed by design and characterization, not tested in production.
8. Production test for this device is at DC conditions.

16–PIN SOIC (300 MIL)



The chamfer on the body is optional. If it is not present, a terminal 1 identifier must be positioned so that 1/2 or more of its area is contained in the hatched zone.

PKG	16-PIN	
DIM	MIN	MAX
A IN. MM	0.094 2.38	0.105 2.68
A1 IN. MM	0.004 0.102	0.012 0.30
A2 IN. MM	0.089 2.26	0.095 2.41
b IN. MM	0.013 0.33	0.020 0.51
C IN MM	0.009 0.229	0.013 0.33
D IN. MM	0.398 10.11	0.412 10.46
e IN. MM	.050 BSC 1.27 BSC	
E1 IN. MM	0.290 7.37	0.300 7.62
H IN MM	0.398 10.11	0.416 10.57
L IN MM	0.016 0.40	0.040 1.02
Θ	0°	8°

9

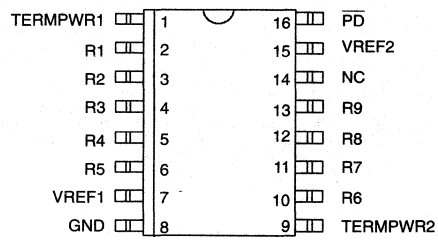
DALLAS SEMICONDUCTOR

DS21S07A
SCSI Terminator

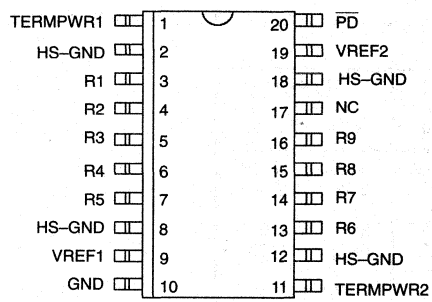
FEATURES

- Fully compliant with SCSI, SCSI-2, and emerging SCSI-3 standards
- Backward compatible to the DS2107 and DS2107A
- Provides active termination for 9 signal lines
- Laser-trimmed 110 ohm termination resistors have 2% tolerance
- Low dropout voltage regulator
- Power-down mode isolates termination resistors from the bus
- SCSI bus hot plug-compatible
- Fully supports actively negated SCSI signals
- Onboard thermal shutdown circuitry
- 16-pin plastic SOIC (DS21S07AS) and 20-pin plastic TSSOP (Thin Shrink Small Outline Package) (DS21S07AE)

PIN ASSIGNMENT

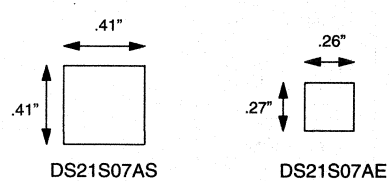


DS21S07AS 16-Pin SOIC (300 mil)



DS21S07AE 20-Pin TSSOP (173 mil)

ACTUAL FOOTPRINT SIZE



DS21S07AS DS21S07AE

DESCRIPTION

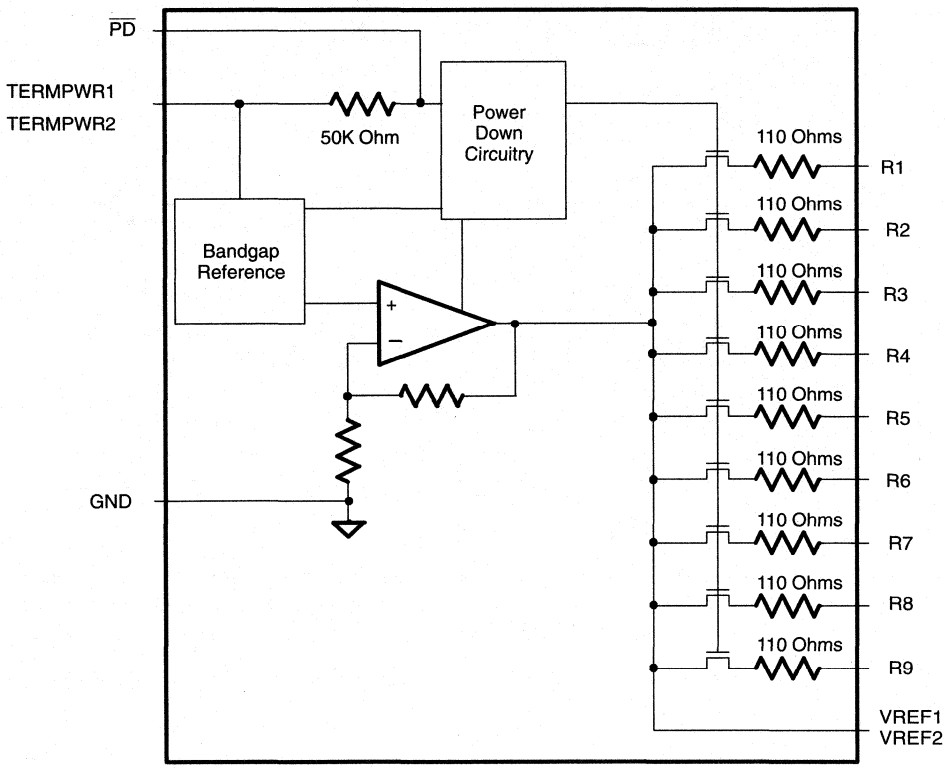
The SCSI-2 and SCSI–3 standards recommend the use of active terminations at both ends of every cable segment in a SCSI system with single-ended drivers and receivers. The DS21S07A SCSI Terminator, which is fully compliant with these standards, enables the designer to gain the benefits of active termination: greater immunity to voltage drops on the TERMPWR (TERMination PoWeR) line, enhanced high-level noise immunity, intrinsic TERMPWR decoupling, and very low quiescent current consumption. The DS21S07A integrates a regulator and nine precise switched 110 ohm termination resistors into a monolithic IC. The DS21S07A can be electrically isolated from the SCSI bus without physical removal from the SCSI device.

FUNCTIONAL DESCRIPTION

The DS21S07A consists of a bandgap reference, buffer amplifier, and nine termination resistors (Figure 1). The bandgap reference circuit produces a precise 2.55V level which is fed to a buffer amplifier. The buffer produces a 2.85V level and is capable of sourcing at least 24 mA into each of the termination resistors when the signal line is low (active). When the driver for a given signal line turns off, the terminator will pull the signal line to 2.85V (quiescent state). To handle actively negated SCSI signals, the buffer can sink at least 200 mA. When all lines settle in the quiescent state, the regulator will consume about 2.5 mA. When the DS21S07A is put into power-down mode by bringing $\overline{PD}$ low, the power-down circuitry will turn off the transistors on each signal line. This will isolate the DS21S07A from the signal lines and effectively remove it from the circuit. The power-down pin ($\overline{PD}$) has an internal 50K ohm pull-up resistor. To place the DS21S07A into an active state, the $\overline{PD}$ pin should be left open circuited. When installed on disk drives or RAID system components, the DS21S07A will not affect the SCSI bus during a hot plug operation.

To ensure proper operation, both the TERMPWR1 and TERMPWR2 pins must be connected to the SCSI bus TERMPWR line and both the VREF1 and VREF2 pins must be tied together externally. Each DS21S07A requires a 4. 7 µF capacitor connected between the VREF pins and ground. Figure 2 details a typical SCSI bus configuration. In an 8-bit wide SCSI bus arrangement ("A" Cable), two DS21S07A's would be needed at each end of the SCSI cable in order to terminate the 18 active signal lines. In a 16-bit wide SCSI bus arrangement ("P" Cable), three DS21S07A's would be needed at each end of the SCSI cable in order to terminate the 27 active signal lines.

DS21S07A BLOCK DIAGRAM Figure 1



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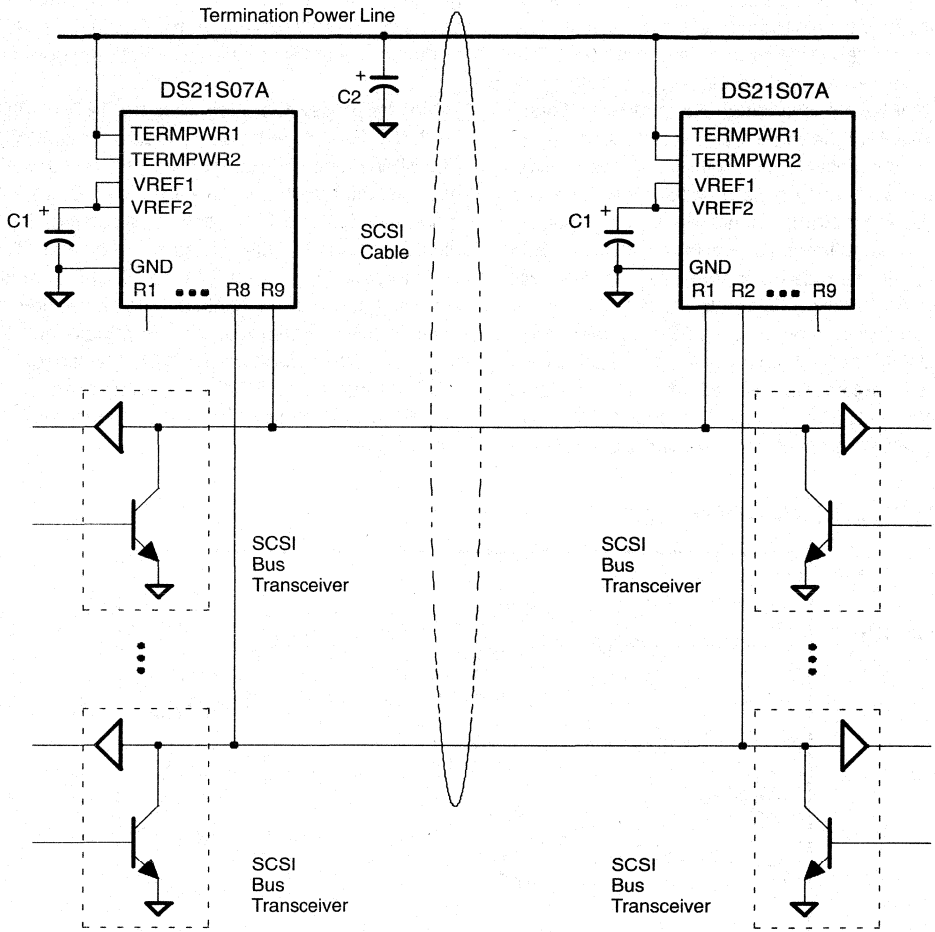
TYPICAL SCSI BUS CONFIGURATION Figure 2



NOTES:

1. C1 = 4.7 µF tantalum
   C2 = 2.2 µF tantalum or 4.7 µF aluminum
2. If the DS21S07A is to be embedded into a peripheral that will act as a target on a SCSI bus, it is recommended that TERMPWR be derived from the SCSI cable, not generated locally. In this configuration, if a power failure occurs in the peripheral, it will not affect the bus.
3. A high frequency bypass capacitor (0.1 µF recommended) can be added in parallel to C1 for applications using fast rise/fall time drivers.

PIN DESCRIPTION Table 1

DS21S07AE PIN	DS21S07AS PIN	SYMBOL	DESCRIPTION
1	1	TERMPWR1	**Termination Power 1.** Should be connected to the SCSI TERMPWR line. Must be decoupled with either a 2.2 µF or 4.7 µF. See Figure 2.
3	2	R1	**Signal Termination 1.** 110 ohm termination.
4	3	R2	**Signal Termination 2.** 110 ohm termination.
5	4	R3	**Signal Termination 3.** 110 ohm termination.
6	5	R4	**Signal Termination 4.** 110 ohm termination.
7	6	R5	**Signal Termination 5.** 110 ohm termination.
9	7	VREF1	**Reference Voltage 1.** Must be externally connected directly to the VREF2 pin. Must be decoupled with a 4.7 µF capacitor as shown in Figure 2.
10	8	GND	**Ground.** Signal ground; 0.0V.
11	9	TERMPWR2	**Termination Power 2.** Should be connected to the SCSI TERMPWR line. Must be decoupled with either a 2.2 µF or 4.7 µF. See Figure 2.
13	10	R6	**Signal Termination 6.** 110 ohm termination.
14	11	R7	**Signal Termination 7.** 110 ohm termination.
15	12	R8	**Signal Termination 8.** 110 ohm termination.
16	13	R9	**Signal Termination 9.** 110 ohm termination.
17	14	NC	**No Connect.** Do not connect any signal to this pin.
19	15	VREF2	**Reference Voltage 2.** Must be externally connected directly to the VREF1 pin. Must be decoupled with a 4.7 µF capacitor as shown in Figure 2.
20	16	$\overline{PD}$	**Power Down.** When tied low, the DS21S07A enters a power-down mode. Contains an internal 50K pull-up. Strap low to deactivate the DS21S07A, leave open circuited to activate the DS21S07A.
2,8,12,18	N/A	HS–GND	**Heat Sink Ground.** Internally connected to the mounting pad. Should be either grounded or electrically isolated from other circuitry.

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to +70°C
Storage Temperature	-55°C to 125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TERMPWR Voltage	V_{TP}	4.00		5.50	V	
$\overline{PD}$ Active	V_{PDA}	-0.3		0.8	V	
$\overline{PD}$ Inactive	V_{PDI}	2.0		V_{TP} +0.3	V	

DC CHARACTERISTICS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TERMPWR Current	I_{TP} I_{TP}		 2.5	250 3	mA mA	1,3 1,4
Power Down Current	I_{PD}		100	150	µA	1,2,5
Termination Resistance	R_{TERM}	108	110	112	ohms	1,2
Die Thermal Shutdown	T_{SD}	150			°C	1, 6
Power Down Termination Capacitance	C_{PD}		3.0	5.0	pF	1,2,5,6
Input Leakage High	I_{IH}	–1.0			µA	1,8
Input Leakage Low	I_{IL}			1.0	µA	1,7

REGULATOR CHARACTERISTICS

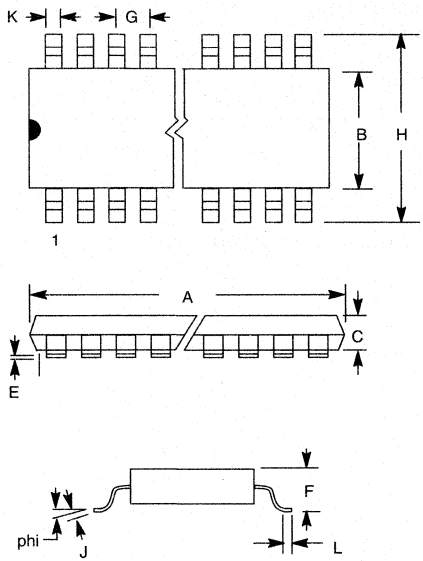
(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Voltage	V_{REF}	2.79	2.85	2.93	V	1,2
Drop Out Voltage	V_{DROP}		0.50	0.75	V	3,6
Line Regulation	LI_{REG}		1.0	2.0	%	1,4
Load Regulation	LO_{REG}		1.3	3.0	%	1,3
Current Limit	I_{LIM}	300		450	mA	1
Sink Current	I_{SINK}	200			mA	1

NOTES:

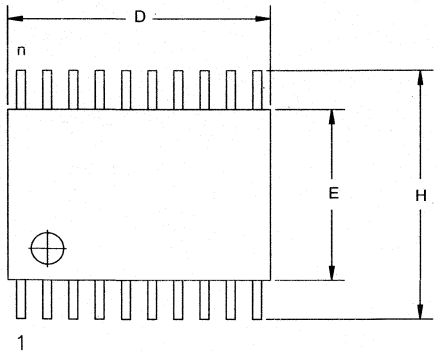
1. 4.00V < TERMPWR < 5.50V.
2. 0.0V < signal lines < TERMPWR.
3. All signal lines = 0.0V.
4. All signal lines open.
5. $\overline{PD}$ = 0.0V.
6. Guaranteed by design; not production tested.
7. R_1 through R_9 only.
8. R_1 through R_9 and $\overline{PD}$.

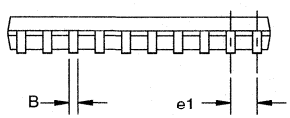
DS21S07AS SCSI TERMINATOR 16-PIN SOIC (300 MIL)

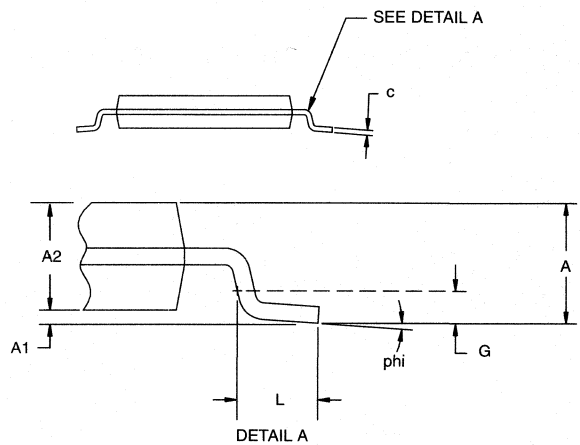


PKG	16-PIN	
DIM	MIN	MAX
A IN. MM	0.402 10.21	0.412 10.46
B IN. MM	0.290 7.37	0.300 7.65
C IN. MM	0.089 2.26	0.095 2.41
E IN. MM	0.004 0.102	0.012 0.30
F IN. MM	0.094 2.38	0.105 2.68
G IN. MM	0.050 BSC 1.27 BSC	
H IN. MM	0.398 10.11	0.416 10.57
J IN. MM	0.009 0.229	0.013 0.33
K IN. MM	0.013 0.33	0.019 0.48
L IN. MM	0.016 0.40	0.040 1.02
phi	0°	8°

DS21S07AE SCSI TERMINATOR 20-PIN TSSOP







DIM	MIN	MAX
A MM	–	1.10
A1 MM	0.05	–
A2 MM	0.75	1.05
C MM	0.09	0.18
L MM	0.50	0.70
e1 MM	0.65 BSC	
B MM	0.18	0.30
D MM	6.40	6.90
E MM	4.40 NOM	
G MM	0.25 REF	
H MM	6.25	6.55
phi	0°	8°

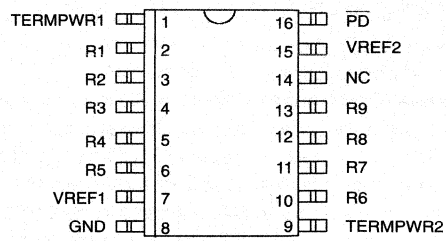
DALLAS SEMICONDUCTOR

DS21S07C
SCSI Terminator

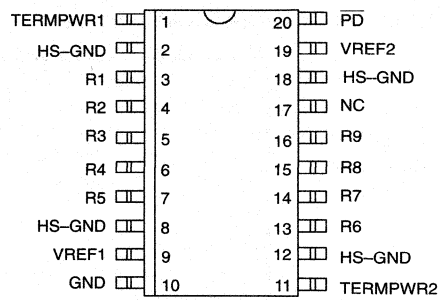
FEATURES

- Fully compliant with SCSI, SCSI-2, and emerging SCSI-3 standards
- Backward compatible to the DS2107C
- Provides active termination for 9 signal lines
- Laser-trimmed 110 ohm termination resistors have 2% tolerance
- Low dropout voltage regulator
- Power-down mode isolates termination resistors from the bus; voltage regulator remains active
- SCSI bus hot plug-compatible
- Fully supports actively negated SCSI signals
- Onboard thermal shutdown circuitry
- 16-pin plastic SOIC (DS21S07CS) and 20-pin plastic TSSOP (Thin Shrink Small Outline Package) (DS21S07CE)

PIN ASSIGNMENT

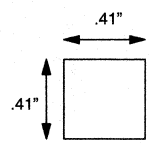


DS21S07CS 16-Pin SOIC (300 mil)

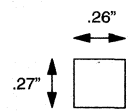


DS21S07CE 20-Pin TSSOP (173 mil)

ACTUAL FOOTPRINT SIZE



DS21S07AS



DS21S07AE

9

DESCRIPTION

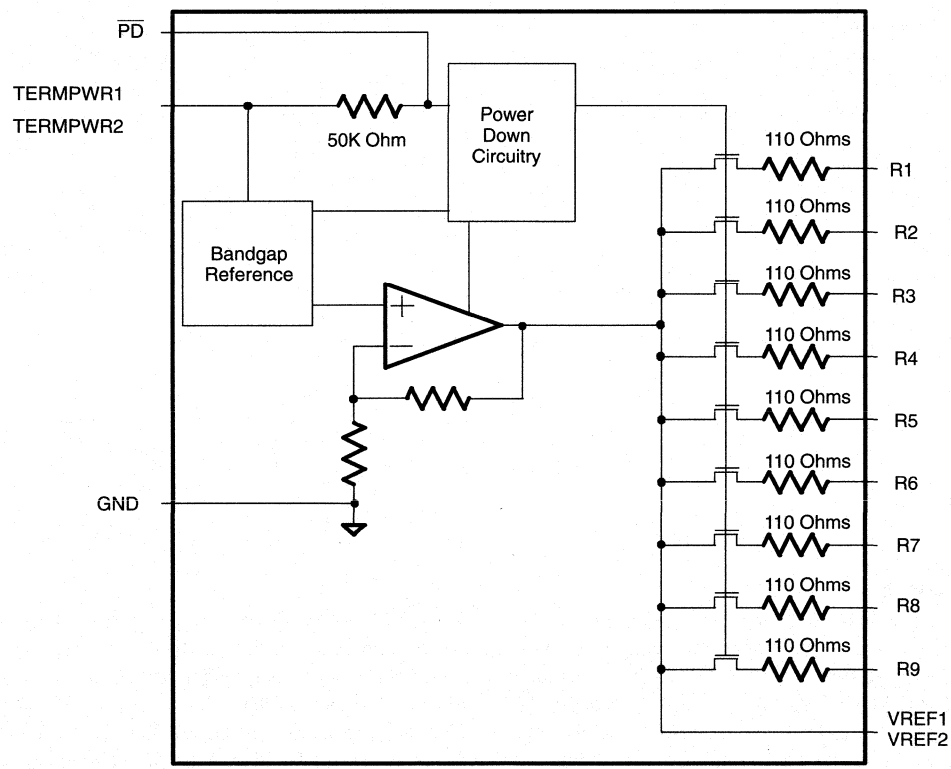
The SCSI-2 and SCSI–3 standards recommend the use of active terminations at both ends of every cable segment in a SCSI system with single-ended drivers and receivers. The DS21S07C SCSI Terminator, which is fully compliant with these standards, enables the designer to gain the benefits of active termination: greater immunity to voltage drops on the TERMPWR (TERMination PoWeR) line, enhanced high-level noise immunity, intrinsic TERMPWR decoupling, and very low quiescent current consumption. The DS21S07C integrates a regulator and nine precise switched 110 ohm termination resistors into a monolithic IC. The DS21S07C can be electrically isolated from the SCSI bus without physical removal from the SCSI device. The voltage regulator is still active in this power-down mode.

FUNCTIONAL DESCRIPTION

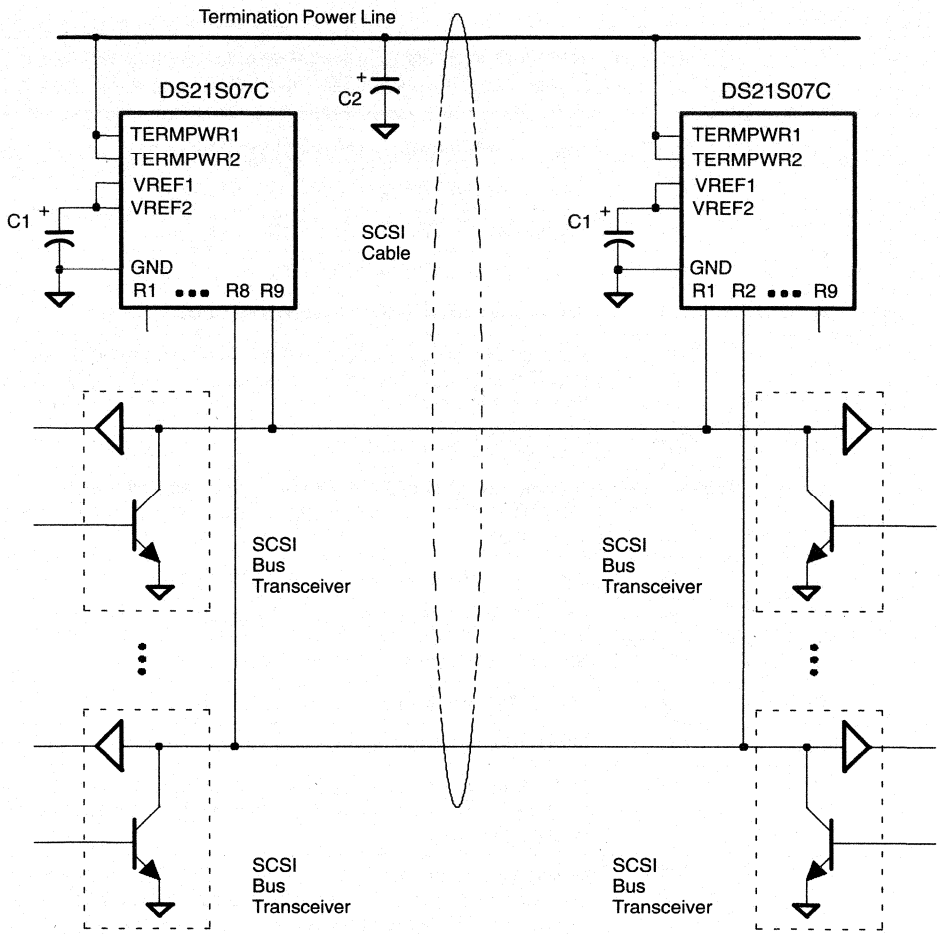
The DS21S07C consists of a bandgap reference, buffer amplifier, and nine termination resistors (Figure 1). The bandgap reference circuit produces a precise 2.55V level which is fed to a buffer amplifier. The buffer produces a 2.85V level and is capable of sourcing at least 24 mA into each of the termination resistors when the signal line is low (active). When the driver for a given signal line turns off, the terminator will pull the signal line to 2.85V (quiescent state). To handle actively negated SCSI signals, the buffer can sink at least 200 mA. When all lines settle in the quiescent state, the regulator will consume about 2.5 mA. When the DS21S07C is put into power-down mode by bringing $\overline{PD}$ low, the power-down circuitry will turn off the transistors on each signal line. This will isolate the DS21S07C from the signal lines and effectively remove it from the circuit; the voltage regulator remains active for access to the 2.85V reference voltage via the VREF pins. The power-down pin ($\overline{PD}$) has an internal 50K ohm pull-up resistor. To place the DS21S07C into an active state, the $\overline{PD}$ pin should be left open circuited. When installed on disk drives or RAID system components, the DS21S07C will not affect the SCSI bus during a hot plug operation.

To ensure proper operation, both the TERMPWR1 and TERMPWR2 pins must be connected to the SCSI bus TERMPWR line and both the VREF1 and VREF2 pins must be tied together externally. Each DS21S07C requires a 4. 7 µF capacitor connected between the VREF pins and ground. Figure 2 details a typical SCSI bus configuration. In an 8-bit wide SCSI bus arrangement ("A" Cable), two DS21S07C's would be needed at each end of the SCSI cable in order to terminate the 18 active signal lines. In a 16-bit wide SCSI bus arrangement ("P" Cable), three DS21S07C's would be needed at each end of the SCSI cable in order to terminate the 27 active signal lines.

DS21S07C BLOCK DIAGRAM Figure 1



TYPICAL SCSI BUS CONFIGURATION Figure 2



NOTES:

1. C1 = 4.7 µF tantalum
   C2 = 2.2 µF tantalum or 4.7 µF aluminum
2. If the DS21S07C is to be embedded into a peripheral that will act as a target on a SCSI bus, it is recommended that TERMPWR be derived from the SCSI cable, not generated locally. In this configuration, if a power failure occurs in the peripheral, it will not affect the bus.
3. A high frequency bypass capacitor (0.1 µF recommended) can be added in parallel to C1 for applications using fast rise/fall time drivers.

9

PIN DESCRIPTION Table 1

DS21S07CE PIN	DS21S07CS PIN	SYMBOL	DESCRIPTION
1	1	TERMPWR1	**Termination Power 1.** Should be connected to the SCSI TERMPWR line. Must be decoupled with either a 2.2 µF or 4.7 µF. See Figure 2.
3	2	R1	**Signal Termination 1.** 110 ohm termination.
4	3	R2	**Signal Termination 2.** 110 ohm termination.
5	4	R3	**Signal Termination 3.** 110 ohm termination.
6	5	R4	**Signal Termination 4.** 110 ohm termination.
7	6	R5	**Signal Termination 5.** 110 ohm termination.
9	7	VREF1	**Reference Voltage 1.** Must be externally connected directly to the VREF2 pin. Must be decoupled with a 4.7 µF capacitor as shown in Figure 2.
10	8	GND	**Ground.** Signal ground; 0.0V.
11	9	TERMPWR2	**Termination Power 2.** Should be connected to the SCSI TERMPWR line. Must be decoupled with either a 2.2 µF or 4.7 µF. See Figure 2.
13	10	R6	**Signal Termination 6.** 110 ohm termination.
14	11	R7	**Signal Termination 7.** 110 ohm termination.
15	12	R8	**Signal Termination 8.** 110 ohm termination.
16	13	R9	**Signal Termination 9.** 110 ohm termination.
17	14	NC	**No Connect.** Do not connect any signal to this pin.
19	15	VREF2	**Reference Voltage 2.** Must be externally connected directly to the VREF1 pin. Must be decoupled with a 4.7 µF capacitor as shown in Figure 2.
20	16	$\overline{PD}$	**Power Down.** When tied low, the DS21S07C enters a power-down mode. Contains an internal 50K pull-up. Strap low to isolate the DS21S07C, leave open circuited to attach the DS21S07C to the SCSI bus. In both modes VREF remains active.
2,8,12,18	N/A	HS–GND	**Heat Sink Ground.** Internally connected to the mounting pad. Should be either grounded or electrically isolated from other circuitry.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to +70°C
Storage Temperature	-55°C to 125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TERMPWR Voltage	V_{TP}	4.00		5.50	V	
$\overline{PD}$ Active	V_{PDA}	-0.3		0.8	V	
$\overline{PD}$ Inactive	V_{PDI}	2.0		V_{TP} +0.3	V	

DC CHARACTERISTICS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TERMPWR Current	I_{TP} I_{TP}		 2.5	250 3	mA mA	1,3 1,4
Power Down Current	I_{PD}		2.5	3	mA	1,2,5
Termination Resistance	R_{TERM}	108	110	112	ohms	1,2
Die Thermal Shutdown	T_{SD}	150			°C	1, 6
Power Down Termination Capacitance	C_{PD}		3.0	5.0	pF	1,2,5,6
Input Leakage High	I_{IH}	–1.0			µA	1,8
Input Leakage Low	I_{IL}			1.0	µA	1,7

REGULATOR CHARACTERISTICS

(0°C to 70°C)

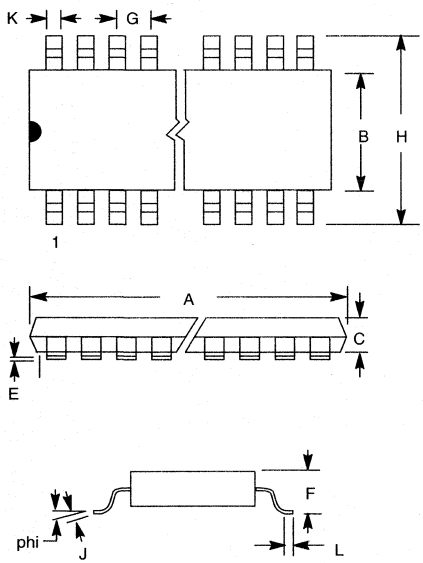
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Voltage	V_{REF}	2.79	2.85	2.93	V	1,2
Drop Out Voltage	V_{DROP}		0.50	0.75	V	3,6
Line Regulation	LI_{REG}		1.0	2.0	%	1,4
Load Regulation	LO_{REG}		1.3	3.0	%	1,3
Current Limit	I_{LIM}	300		450	mA	1
Sink Current	I_{SINK}	200			mA	1

9

NOTES:

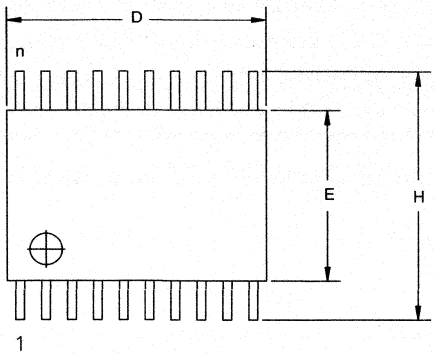
1. 4.00V < TERMPWR < 5.50V.
2. 0.0V < signal lines < TERMPWR.
3. All signal lines = 0.0V.
4. All signal lines open.
5. $\overline{PD}$ = 0.0V.
6. Guaranteed by design; not production tested.
7. R_1 through R_9 only.
8. R_1 through R_9 and $\overline{PD}$.

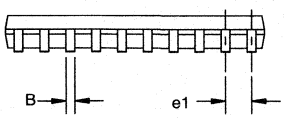
DS21S07CS SCSI TERMINATOR 16-PIN SOIC (300 MIL)

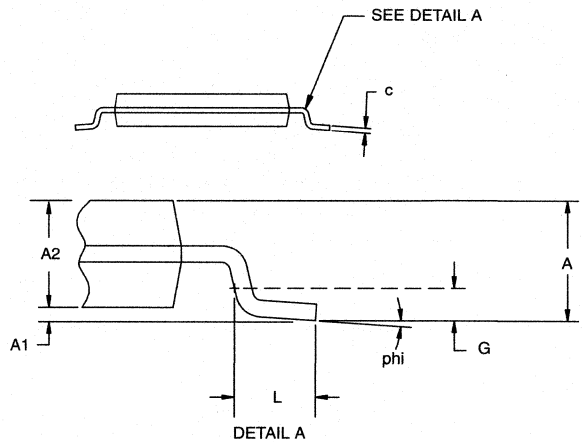


PKG	16-PIN	
DIM	MIN	MAX
A IN. MM	0.402 10.21	0.412 10.46
B IN. MM	0.290 7.37	0.300 7.65
C IN. MM	0.089 2.26	0.095 2.41
E IN. MM	0.004 0.102	0.012 0.30
F IN. MM	0.094 2.38	0.105 2.68
G IN. MM	0.050 BSC 1.27 BSC	
H IN. MM	0.398 10.11	0.416 10.57
J IN. MM	0.009 0.229	0.013 0.33
K IN. MM	0.013 0.33	0.019 0.48
L IN. MM	0.016 0.40	0.040 1.02
phi	0°	8°

DS21S07CE SCSI TERMINATOR 20-PIN TSSOP







DIM	MIN	MAX
A MM	–	1.10
A1 MM	0.05	–
A2 MM	0.75	1.05
C MM	0.09	0.18
L MM	0.50	0.70
e1 MM	0.65 BSC	
B MM	0.18	0.30
D MM	6.40	6.90
E MM	4.40 NOM	
G MM	0.25 REF	
H MM	6.25	6.55
phi	0°	8°

9

THERMAL MANAGEMENT

10

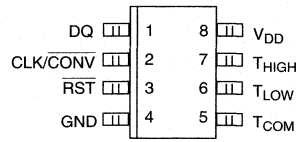
DALLAS SEMICONDUCTOR

DS1620
Digital Thermometer and Thermostat

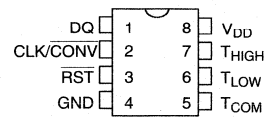
FEATURES

- Requires no external components
- Measures temperatures from –55°C to +125°C in 0.5°C increments. Fahrenheit equivalent is –67°F to 257°F in 0.9°F increments
- Temperature is read as a 9–bit value
- Converts temperature to digital word in 200 ms, typical
- Thermostatic settings are user–definable and non–volatile
- Data is read from/written via a 3–wire serial interface (CLK, DQ, $\overline{RST}$)
- Applications include thermostatic controls, industrial systems, consumer products, thermometers, or any thermally sensitive system
- 8–pin DIP or SOIC package

PIN ASSIGNMENT



DS1620S
8–PIN SOIC (208 MIL)
See Mech. Drawings Section



DS1620
8–PIN DIP
See Mech. Drawings Section

PIN DESCRIPTION

DQ	–	3–Wire Input/Output
CLK/$\overline{CONV}$	–	3–Wire Clock Input and Standalone Convert Input
$\overline{RST}$	–	3–Wire Reset Input
GND	–	Ground
T_{HIGH}	–	High Temperature Trigger
T_{LOW}	–	Low Temperature Trigger
T_{COM}	–	High/Low Combination Trigger
V_{DD}	–	Power Supply Voltage (+5V)

DESCRIPTION

The DS1620 Digital Thermometer and Thermostat provides 9–bit temperature readings which indicate the temperature of the device. With three thermal alarm outputs, the DS1620 can also act as a thermostat. T_{HIGH} is driven high if the DS1620's temperature is greater than or equal to a user–defined temperature TH. T_{LOW} is driven high if the DS1620's temperature is less than or equal to a user–defined temperature TL. T_{COM} is driven high when the temperature exceeds TH and stays high until the temperature falls below that of TL.

User–defined temperature settings are stored in non–volatile memory, so parts can be programmed prior to insertion in a system, as well as used in standalone applications without a CPU. Temperature settings and temperature readings are all communicated to/from the DS1620 over a simple 3–wire interface.

OPERATION–READING TEMPERATURE

The DS1620 measures temperatures through the use of an onboard, proprietary temperature measurement technique. The temperature reading is provided in a 9–bit, two's complement format. Table 1 describes the exact relationship of output data to measured temperature. The data is transmitted serially through the 3–wire serial interface, LSB first. The DS1620 can measure temperature over the range of –55°C to +125°C in 0.5°C increments. For Fahrenheit usage, a lookup table or conversion factor must be used.

Since data is transmitted over the 3–wire bus LSB first, temperature data can be written to/read from the DS1620 as either a 9–bit word (taking $\overline{RST}$ low after the 9th (MSB) bit), or as two transfers of 8–bit words, with the most significant 7 bits being ignored or set to zero, as illustrated in Table 1. After the MSB, the DS1620 will output 0's.

Note that temperature is represented in the DS1620 in terms of a $^1/_2$°C LSB, yielding the following 9–bit format:

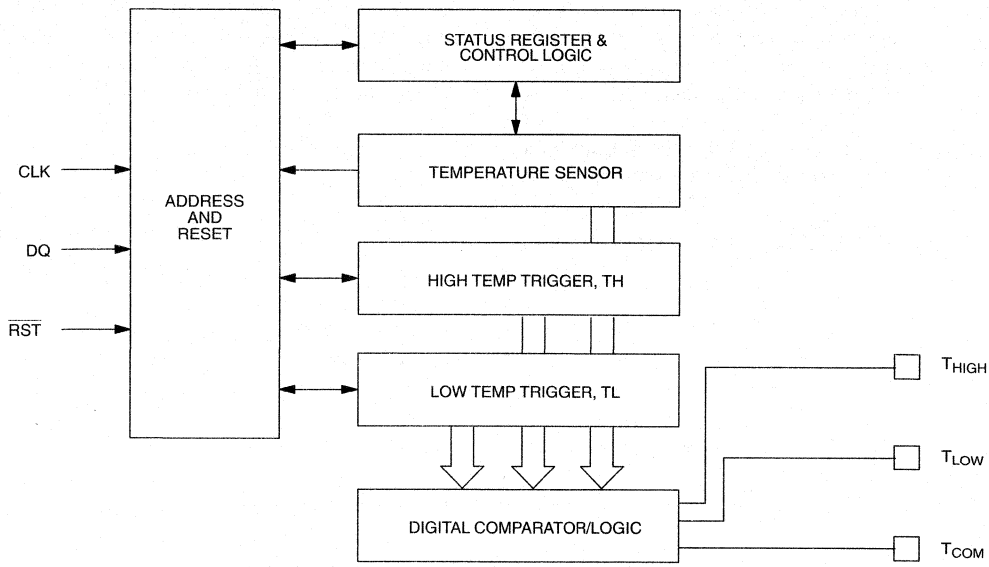
MSB								LSB							
X	X	X	X	X	X	X	1	1	1	0	0	1	1	1	0

T = –25°C

TEMPERATURE/DATA RELATIONSHIPS Table 1

TEMP	DIGITAL OUTPUT (Binary)	DIGITAL OUTPUT (Hex)
+125°C	0 11111010	00FA
+25°C	0 00110010	0032h
$^1/_2$°C	0 00000001	0001h
0°C	0 00000000	0000h
–$^1/_2$°C	1 11111111	01FFh
–25°C	1 11001110	01CEh
–55°C	1 10010010	0192h

DS1620 FUNCTIONAL BLOCK DIAGRAM Figure 1



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DETAILED PIN DESCRIPTION Table 2

PIN	SYMBOL	DESCRIPTION
1	DQ	**Data Input/Output pin** for 3–wire communication port.
2	CLK/$\overline{CONV}$	**Clock input pin** for 3–wire communication port. When the DS1620 is used in a standalone application with no 3–wire port, this pin can be used as a convert pin. Temperature conversion will begin on the falling edge of $\overline{CONV}$.
3	$\overline{RST}$	**Reset input pin** for 3–wire communication port.
4	GND	**Ground pin**.
5	T_{COM}	**High/Low Combination Trigger**. Goes high when temperature exceeds TH; will reset to low when temperature falls below TL.
6	T_{LOW}	**Low Temperature Trigger**. Goes high when temperature falls below TL.
7	T_{HIGH}	**High Temperature Trigger**. Goes high when temperature exceeds TH.
8	V_{DD}	**Supply Voltage**. 5V input power pin.

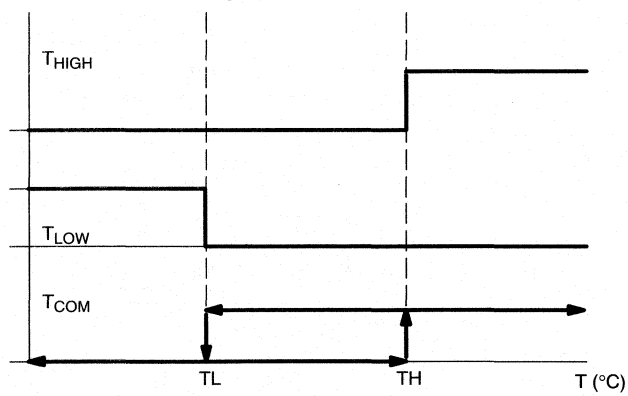
OPERATION–THERMOSTAT CONTROLS

Three thermally triggered outputs, T_{HIGH}, T_{LOW}, and T_{COM}, are provided to allow the DS1620 to be used as a thermostat, as shown in Figure 2. When the DS1620's temperature meets or exceeds the value stored in the high temperature trip register, the output T_{HIGH} becomes active (high) and remains active until the DS1620's measured temperature becomes less than the stored value in the high temperature register, TH. The T_{HIGH} output can be used to indicate that a high temperature tolerance boundary has been met or exceeded, or as part of a closed loop system can be used to activate a cooling system and to deactivate it when the system temperature returns to tolerance.

The T_{LOW} output functions similarly to the T_{HIGH} output. When the DS1620's measured temperature equals or falls below the value stored in the low temperature register, the T_{LOW} output becomes active. T_{LOW} remains active until the DS1620's temperature becomes greater than the value stored in the low temperature register, TL. The T_{LOW} output can be used to indicate that a low temperature tolerance boundary has been met or exceeded, or as part of a closed loop system, can be used to activate a heating system and to deactivate it when the system temperature returns to tolerance.

The T_{COM} output goes high when the measured temperature meets or exceeds TH, and will stay high until the temperature equals or falls below TL. In this way, any amount of hysteresis can be obtained.

THERMOSTAT OUTPUT OPERATION Figure 2



OPERATION AND CONTROL

The DS1620 must have temperature settings resident in the TH and TL registers for thermostatic operation. A configuration/status register is also used to determine the method of operation that the DS1620 will use in a particular application, as well as indicating the status of the temperature conversion operation. The configuration register is defined as follows:

CONFIGURATION/STATUS REGISTER

DONE	THF	TLF	NVB	1	0	CPU	1SHOT

where

DONE = Conversion Done bit. 1=conversion complete, 0=conversion in progress.

THF = Temperature High Flag. This bit will be set to 1 when the temperature is greater than or equal to the value of TH. It will remain 1 until reset by writing 0 into this location or by removing power from the device. This feature provides a method of determining if the DS1620 has ever been subjected to temperatures above TH while power has been applied.

TLF = Temperature Low Flag. This bit will be set to 1 when the temperature is less than or equal to the value of TL. It will remain 1 until reset by writing 0 into this location or by removing power from the device. This feature provides a method of determining if the DS1620 has ever been subjected to temperatures below TL while power has been applied.

NVB = Nonvolatile Memory Busy Flag. 1=write to an E^2 memory cell in progress. 0=nonvolatile memory is not busy. A write to E^2 may take up to 10 ms.

CPU = CPU use bit. If CPU=0, the CLK/$\overline{\text{CONV}}$ pin acts as a conversion start control, when $\overline{\text{RST}}$ is low. If CPU is 1, the DS1620 will be used with a CPU communicating to it over the 3–wire port, and the operation of the CLK/$\overline{\text{CONV}}$ pin is as a normal clock in concert with DQ and $\overline{\text{RST}}$. This bit is stored in nonvolatile E^2 memory, capable of at least 50,000 writes.

1SHOT = One–Shot Mode. If 1SHOT is 1, the DS1620 will perform one temperature conversion upon reception of the Start Convert T protocol. If 1SHOT is 0, the DS1620 will continuously perform temperature conversion. This bit is stored in nonvolatile E^2 memory, capable of at least 50,000 writes.

For typical thermostat operation, the DS1620 will operate in continuous mode. However, for applications where only one reading is needed at certain times, and to conserve power, the one–shot mode may be used. Note that the thermostat outputs (T_{HIGH}, T_{LOW}, T_{COM}) will remain in the state they were in after the last valid temperature conversion cycle when operating in one–shot mode.

OPERATION IN STANDALONE MODE

In applications where the DS1620 is used as a simple thermostat, no CPU is required. Since the temperature limits are nonvolatile, the DS1620 can be programmed prior to insertion in the system. In order to facilitate operation without a CPU, the CLK/$\overline{\text{CONV}}$ pin (pin 2) can be used to initiate conversions. Note that the CPU bit must be set to 0 in the configuration register to use this mode of operation.

To use the CLK/$\overline{\text{CONV}}$ pin to initiate conversions, $\overline{\text{RST}}$ must be low and CLK/$\overline{\text{CONV}}$ must be high. If CLK/$\overline{\text{CONV}}$ is driven low and then brought high in less than 10 ms, one temperature conversion will be performed and then the DS1620 will return to an idle state. If CLK/$\overline{\text{CONV}}$ is driven low and remains low, continuous conversions will take place until CLK/$\overline{\text{CONV}}$ is brought high again. With the CPU bit set to 0, the CLK/$\overline{\text{CONV}}$ will override the 1–shot bit if it is equal to 1. This means that even if the part is set for one–shot mode, driving CLK/$\overline{\text{CONV}}$ low will initiate conversions.

3–WIRE COMMUNICATIONS

The 3–wire bus is comprised of three signals. These are the $\overline{\text{RST}}$ (reset) signal, the CLK (clock) signal, and the DQ (data) signal. All data transfers are initiated by driving the $\overline{\text{RST}}$ input high. Driving the $\overline{\text{RST}}$ input low terminates communication. (See Figures 3 and 4.) A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of a clock cycle. Data bits are output on the falling edge of the clock, and remain valid through the rising edge.

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When reading data from the DS1620, the DQ pin goes to a high impedance state while the clock is high. Taking $\overline{RST}$ low will terminate any communication and cause the DQ pin to go to a high impedance state.

Data over the 3–wire interface is communicated LSB first. The command set for the 3–wire interface as shown in Table 3 is as follows; only these protocols should be written to the DS1620, as writing other protocols to the device may result in permanent damage to the part.

Read Temperature [AAh]
This command reads the contents of the register which contains the last temperature conversion result. The next nine clock cycles will output the contents of this register.

Write TH [01h]
This command writes to the TH (HIGH TEMPERATURE) register. After issuing this command, the next nine clock cycles clock in the 9–bit temperature limit which will set the threshold for operation of the T_{HIGH} output.

Write TL [02h]
This command writes to the TL (LOW TEMPERATURE) register. After issuing this command, the next nine clock cycles clock in the 9–bit temperature limit which will set the threshold for operation of the T_{LOW} output.

Read TH [A1h]
This command reads the value of the TH (HIGH TEMPERATURE) register. After issuing this command, the next nine clock cycles clock out the 9–bit temperature limit which sets the threshold for operation of the T_{HIGH} output.

Read TL [A2h]
This command reads the value of the TL (LOW TEMPERATURE) register. After issuing this command, the next nine clock cycles clock out the 9–bit temperature limit which sets the threshold for operation of the T_{LOW} output.

Start Convert T [EEh]
This command begins a temperature conversion. No further data is required. In one–shot mode, the temperature conversion will be performed and then the DS1620 will remain idle. In continuous mode, this command will initiate continuous conversions.

Stop Convert T [22h]
This command stops temperature conversion. No further data is required. This command may be used to halt a DS1620 in continuous conversion mode. After issuing this command, the current temperature measurement will be completed, and then the DS1620 will remain idle until a Start Convert T is issued to resume continuous operation.

Write Config [0Ch]
This command writes to the configuration register. After issuing this command, the next eight clock cycles clock in the value of the configuration register.

Read Config [ACh]
This command reads the value in the configuration register. After issuing this command, the next eight clock cycles output the value of the configuration register.

DS1620 COMMAND SET Table 3

INSTRUCTION	DESCRIPTION	PROTOCOL	3–WIRE BUS DATA AFTER ISSUING PROTOCOL	NOTES
TEMPERATURE CONVERSION COMMANDS				
Read Temperature	Reads last converted temperature value from temperature register.	AAh	<read data>	
Start Convert T	Initiates temperature conversion.	EEh	idle	1
Stop Convert T	Halts temperature conversion.	22h	idle	1
THERMOSTAT COMMANDS				
Write TH	Writes high temperature limit value into TH register.	01h	<write data>	2
Write TL	Writes low temperature limit value into TL register.	02h	<write data>	2
Read TH	Reads stored value of high temperature limit from TH register.	A1h	<read data>	2
Read TL	Reads stored value of low temperature limit from TL register.	A2h	<read data>	2
Write Config	Writes configuration data to configuration register.	0Ch	<write data>	2
Read Config	Reads configuration data from configuration register.	ACh	<read data>	2

NOTES:

1. In continuous conversion mode, a Stop Convert T command will halt continuous conversion. To restart, the Start Convert T command must be issued. In one–shot mode, a Start Convert T command must be issued for every temperature reading desired.
2. Writing to the E^2 typically requires 10 ms at room temperature. After issuing a write command, no further writes should be requested for at least 10 ms.

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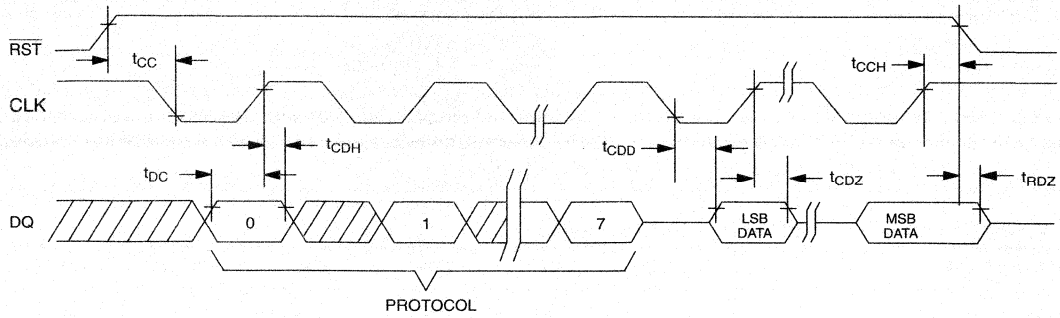
FUNCTION EXAMPLE

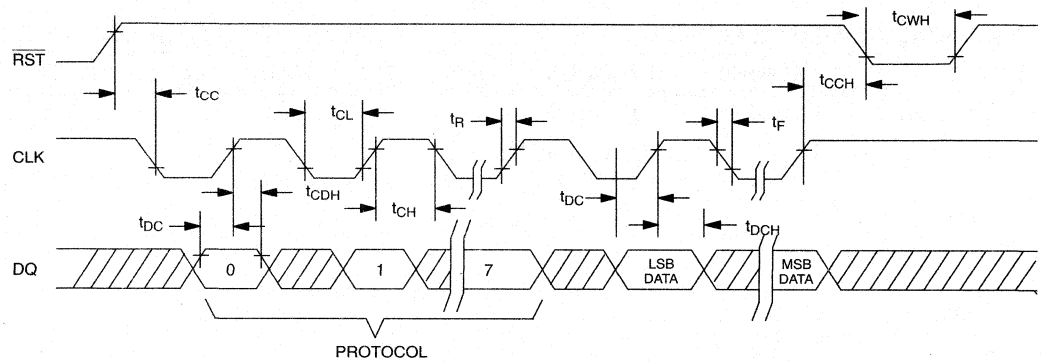
Example: CPU sets up DS1620 for continuous conversion and thermostatic function.

CPU MODE	DS1620 MODE (3–WIRE)	DATA (LSB FIRST)	COMMENTS
TX	RX	0Ch	CPU issues Write Config command.
TX	RX	02h	CPU sets DS1620 up for continuous conversion.
TX	RX	Toggle $\overline{RST}$	CPU issues Reset to DS1620.
TX	RX	01h	CPU issues Write TH command.
TX	RX	0050h	CPU sends data for TH limit of +40°C.
TX	RX	Toggle $\overline{RST}$	CPU issues Reset to DS1620.
TX	RX	02h	CPU issues Write TL command.
TX	RX	0014h	CPU sends data for TL limit of +10°C.
TX	RX	Toggle $\overline{RST}$	CPU issues Reset to DS1620.
TX	RX	A1h	CPU issues Read TH command.
RX	TX	0050h	DS1620 sends back stored value of TH for CPU to verify.
TX	RX	Toggle $\overline{RST}$	CPU issues Reset to DS1620.
TX	RX	A2h	CPU issues Read TL command.
RX	TX	0014h	DS1620 sends back stored value of TL for CPU to verify.
TX	RX	Toggle $\overline{RST}$	CPU issues Reset to DS1620.
TX	RX	EEh	CPU issues Start Convert T command.
TX	RX	Toggle $\overline{RST}$	CPU issues Reset to DS1620.

READ DATA TRANSFER Figure 3



WRITE DATA TRANSFER Figure 4



NOTE: t_{CL}, t_{CH}, t_R, and t_F apply to both read and write data transfer.

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	–55°C to +125°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

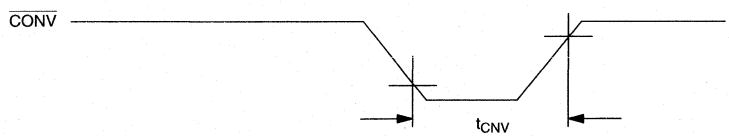
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply	V_{DD}	4.5	5.0	5.5	V	1
Logic 1	V_{IH}	2.0		V_{CC}+0.3	V	1
Logic 0	V_{IL}	–0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(–55°C to +125°C; V_{DD}=4.5V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Thermometer Error	T_{ERR}	0°C to +70°C			±0.5	°C	10, 11
		–55°C to +0°C and 70°C to 125°C	See Typical Curve				
Long-term Stability		105°C, 1000 hours		±0.1		°C	
Logic 0 Output	V_{OL}				0.4	V	3
Logic 1 Output	V_{OH}		2.4			V	2
Input Resistance	R_I	DQ,$\overline{RST}$ to GND, CLK to V_{DD}	1 1			MΩ MΩ	
Active Supply Current	I_{CC}	0°C to +70°C			1	mA	4, 5
Standby Supply Current	I_{STBY}	0°C to +70°C			1	µA	4, 5

SINGLE CONVERT TIMING DIAGRAM (STAND–ALONE MODE)



AC ELECTRICAL CHARACTERISTICS

(–55°C to +125°C; V_{DD}=4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Temperature Conversion Time	T_{TC}		200	500	ms	
Data to CLK Setup	t_{DC}	35			ns	6
CLK to Data Hold	t_{CDH}	40			ns	6
CLK to Data Delay	t_{CDD}			100	ns	6, 7, 8
CLK Low Time	t_{CL}	285			ns	6
CLK High Time	t_{CH}	285			ns	6
CLK Frequency	f_{CLK}	DC		1.75	MHz	6
CLK Rise and Fall	t_R, t_F			500	ns	
$\overline{RST}$ to CLK Setup	t_{CC}	100			ns	6
CLK to $\overline{RST}$ Hold	t_{CCH}	40			ns	6
$\overline{RST}$ Inactive Time	t_{CWH}	125			ns	6, 9
CLK High to I/O High Z	t_{CDZ}			50	ns	6
$\overline{RST}$ Low to I/O High Z	t_{RDZ}			50	ns	6
Convert Pulse Width	t_{CNV}	250 ns		500 ms		
NV Write Cycle Time	t_{WR}		10	50	ms	

AC ELECTRICAL CHARACTERISTICS

(–55°C to +125°C; V_{DD}=4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_I		5		pF	
I/O Capacitance	$C_{I/O}$		10		pF	

NOTES:

1. All voltages are referenced to ground.
2. Logic one voltages are specified at a source current of 1 mA.
3. Logic zero voltages are specified at a sink current of 4 mA.
4. I_{CC} specified with DQ pin open.
5. I_{CC} specified with V_{CC} at 5.0V and $\overline{RST}$=GND.
6. Measured at V_{IH} = 2.0V or V_{IL} = 0.8V.
7. Measured at V_{OH} = 2.4V or V_{OL} = 0.4V.
8. Load capacitance = 50 pF.
9. t_{CWH} must be 10 ms minimum following any write command that involves the E^2 memory.
10. See Figure 5 for specification limits outside 0°C to 70°C range.
11. Thermometer error reflects temperature accuracy as tested during calibration.

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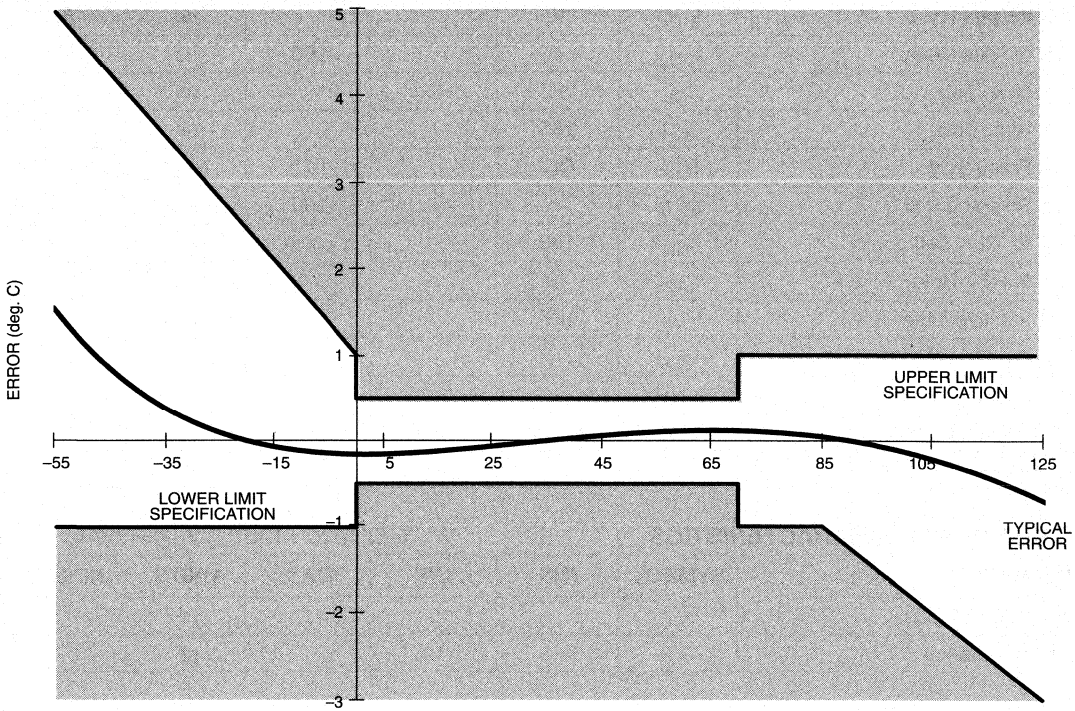
TYPICAL PERFORMANCE CURVE Figure 5

DS1620 DIGITAL THERMOMETER AND THERMOSTAT
TEMPERATURE READING ERROR



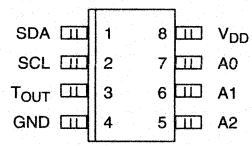
DALLAS SEMICONDUCTOR

DS1621
Digital Thermometer and Thermostat

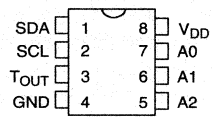
FEATURES

- Temperature measurements require no external components
- Measures temperatures from –55°C to +125°C in 0.5°C increments. Fahrenheit equivalent is –67°F to 257°F in 0.9°F increments
- Temperature is read as a 9–bit value (two byte transfer)
- Converts temperature to digital word in 1 second
- Thermostatic settings are user definable and nonvolatile
- Data is read from/written via a 2–wire serial interface (open drain I/O lines)
- Applications include thermostatic controls, industrial systems, consumer products, thermometers, or any thermal sensitive system.
- 8–pin DIP or SOIC package

PIN ASSIGNMENT



DS1621S
8–PIN SOIC (150 MIL)
See Mech. Drawings
Section



DS1621
8–PIN DIP (300 MIL)
See Mech. Drawings
Section

PIN DESCRIPTION

SDA	–	2–Wire Serial Data Input/Output
SCL	–	2–Wire Serial Clock
GND	–	Ground
T_{OUT}	–	Thermostat Output Signal
A0	–	Chip Address Input
A1	–	Chip Address Input
A2	–	Chip Address Input
V_{DD}	–	Power Supply Voltage

DESCRIPTION

The DS1621 digital thermometer and thermostat provides 9 bit temperature readings which indicate the temperature of the device. The thermal alarm output, T_{OUT}, is active when the temperature of the device exceeds a user–defined temperature TH. The output remains active until the temperature drops below user defined temperature TL, allowing for any hysteresis necessary.

User defined temperature settings are stored in non–volatile memory, so parts may be programmed prior to insertion in a system. Temperature settings, and temperature readings are all communicated to/from the DS1621 over a simple 2–wire serial interface.

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DETAILED PIN DESCRIPTION Table 1

PIN	SYMBOL	DESCRIPTION
1	SDA	Data input/output pin for 2–wire serial communication port.
2	SCL	Clock input/output pin for 2–wire serial communication port.
3	T_{OUT}	Thermostat output. Active when temperature exceeds TH; will reset when temperature falls below TL.
4	GND	Ground pin.
5	A2	Address input pin.
6	A1	Address input pin.
7	A0	Address input pin.
8	V_{DD}	Supply voltage input power pin.

OPERATION

Measuring Temperature

A block diagram of the DS1621 is shown in Figure 1. The DS1621 measures temperatures through the use of an on–board proprietary temperature measurement technique. A block diagram of the temperature measurement circuitry is shown in Figure 2.

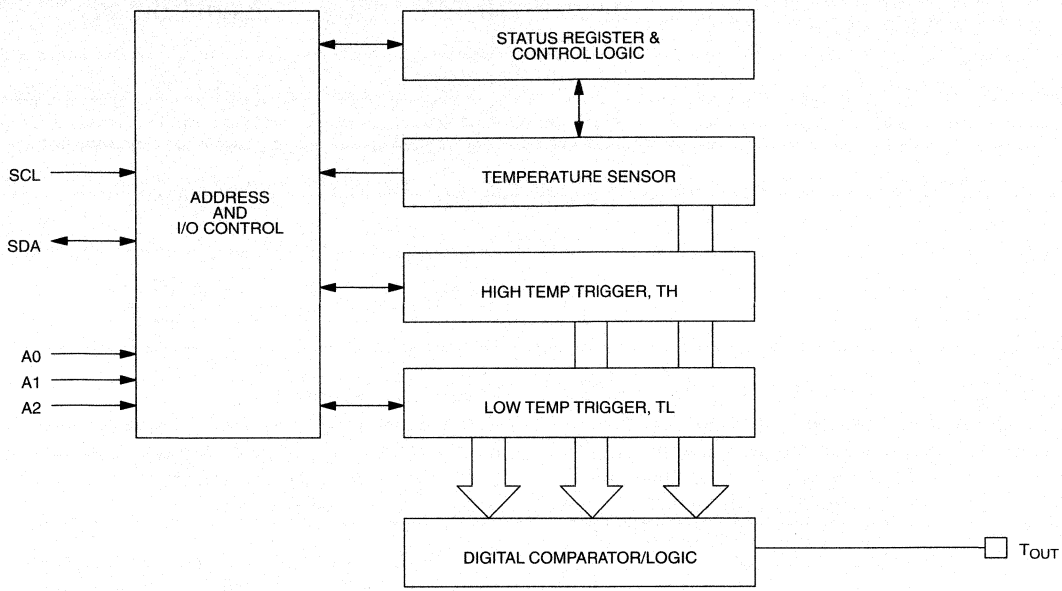
The DS1621 measures temperature by counting the number of clock cycles that an oscillator with a low temperature coefficient goes through during a gate period determined by a high temperature coefficient oscillator. The counter is preset with a base count that corresponds to –55°C. If the counter reaches zero before the gate period is over, the temperature register, which is also preset to the –55°C value, is incremented, indicating that the temperature is higher than –55°C.

At the same time, the counter is then preset with a value determined by the slope accumulator circuitry. This circuitry is needed to compensate for the parabolic behavior of the oscillators over temperature. The counter is then clocked again until it reaches zero. If the gate period is still not finished, then this process repeats.

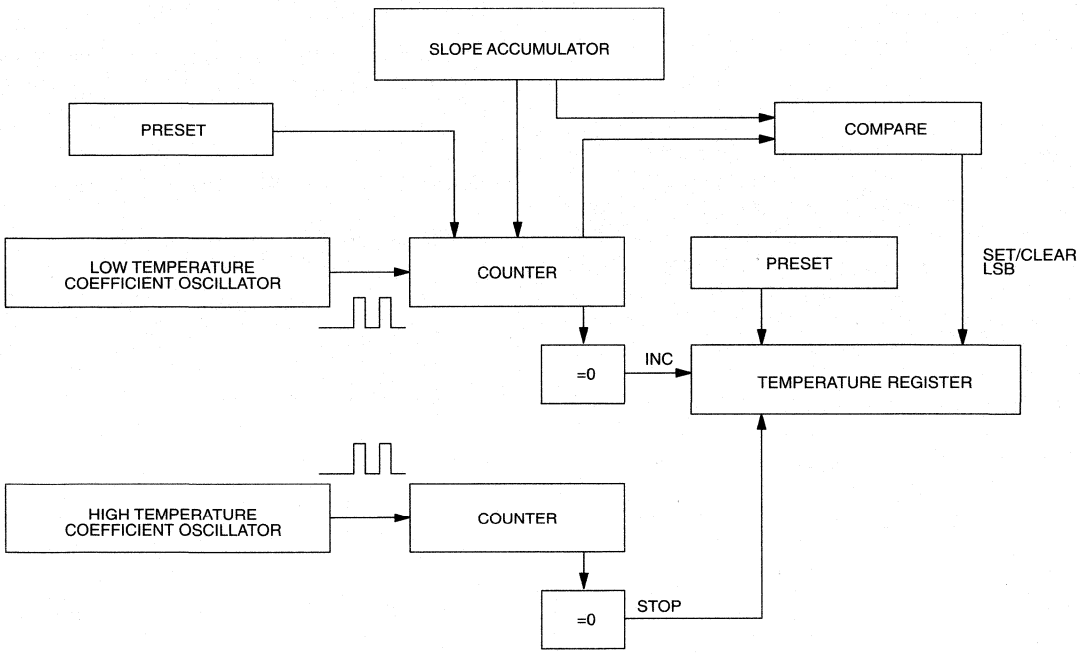
The slope accumulator is used to compensate for the nonlinear behavior of the oscillators over temperature, yielding a high resolution temperature measurement. This is done by changing the number of counts necessary for the counter to go through for each incremental degree in temperature. To obtain the desired resolution, therefore, both the value of the counter and the number of counts per degree C (the value of the slope accumulator) at a given temperature must be known.

This calculation is done inside the DS1621 to provide 0.5°C resolution. The temperature reading is provided in a 9–bit, two's complement reading by issuing the READ TEMPERATURE command. Table 2 describes the exact relationship of output data to measured temperature. The data is transmitted through the 2–wire serial interface, MSB first. The DS1621 can measure temperature over the range of –55°C to +125°C in 0.5°C increments. For Fahrenheit usage, a lookup table or conversion factor must be used.

DS1621 FUNCTIONAL BLOCK DIAGRAM Figure 1



TEMPERATURE MEASURING CIRCUITRY Figure 2



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TEMPERATURE/DATA RELATIONSHIPS Table 2

TEMPERATURE	DIGITAL OUTPUT (Binary)	DIGITAL OUTPUT (Hex)
+125°C	01111101 00000000	7B00h
+25°C	00011001 00000000	1900h
$+^1/_2$°C	0000000010000000	0080h
+0°C	0000000000000000	0000h
$-^1/_2$°C	11111111 10000000	FF80h
–25°C	11100111 00000000	E700h
–55°C	11001001 00000000	C900h

Since data is transmitted over the 2–wire bus MSB first, temperature data may be written to/read from the DS1621 as either a single byte (with temperature resolution of 1°C), or as two bytes, the second byte containing the value of the least significant (0.5°C)bit of the temperature reading, as shown in Table 1. Note that the remaining 7 bits of this byte are set to all 0's.

Note that temperature is represented in the DS1621 in terms of a $^1/_2$°C LSB, yielding the following 9–bit format:

MSB								LSB							
1	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0

T = –25°C

Higher resolutions may be obtained by reading the temperature, and truncating the 0.5°C bit (the LSB) from the read value. This value is TEMP_READ. The value left in the counter may then be read by issuing a READ COUNTER command. This value is the count remaining (COUNT_REMAIN) after the gate period has ceased. By loading the value of the slope accumulator into the count register (using the READ SLOPE command), this value may then be read, yielding the number of counts per degree C (COUNT_PER_C) at that temperature. The actual temperature may be then be calculated by the user using the following:

$$TEMPERATURE = TEMP\_READ - 0.25 + \frac{(COUNT\_PER\_C - COUNT\_REMAIN)}{COUNT\_PER\_C}$$

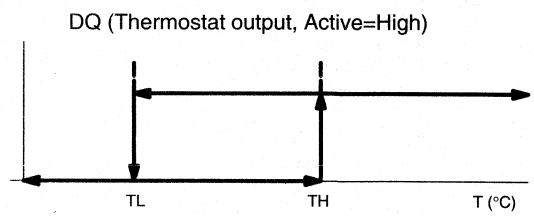
Thermostat Control

In its operating mode, the DS1621 functions as a thermostat with programmable hysteresis, as shown in Figure 3. The thermostat output updates as soon as a temperature conversion is complete.

When the DS1621's temperature meets or exceeds the value stored in the high temperature trip register (TH), the output becomes active, and will stay active until the temperature falls below the temperature stored in the low temperature trigger register (TL). In this way, any amount of hysteresis may be obtained.

The active state for the output is programmable by the user, so that an active state may either be a logic 1 (V_{DD}) or a logic 0 (0V).

THERMOSTAT OUTPUT OPERATION Figure 3



OPERATION AND CONTROL

The DS1621 must have temperature settings resident in the TH and TL registers for thermostatic operation. A configuration/status register is also used to determine the method of operation that the DS1621 will use in a particular application, as well as indicating the status of the temperature conversion operation.

The configuration register is defined as follows:

CONFIGURATION/STATUS REGISTER

DONE	THF	TLF	NVB	1	0	POL	1SHOT

where

DONE = Conversion Done bit. "1" = Conversion complete, "0" = conversion in progress.

THF = Temperature High Flag. This bit will be set to "1" when the temperature is greater than or equal to the value of TH. It will remain "1" until reset by writing 0 into this location or removing power from the device. This feature provides a method of determining if if the DS1621 has ever been subjected to temperatures above TH while power has been applied.

TLF = Temperature Low Flag. This bit will be set to "1" when the temperature is less than or equal to the value of TL. It will remain "1" until reset by writing 0 into this location or removing power from the device. This feature provides a method of determining if if the DS1621 has ever been subjected to temperatures below TL while power has been applied.

NVB = Nonvolatile memory busy flag. "1" = Write to an E^2 memory cell in progress, "0" = nonvolatile memory is not busy. A copy to E^2 may take up to 10 ms.

POL = Output Polarity Bit. "1" = active high, "0" = active low. This bit is nonvolatile.

1SHOT= One Shot Mode. If 1SHOT is "1", the DS1621 will perform one temperature conversion upon reception of the Start Convert T protocol. If 1SHOT is "0", the DS1621 will continuously perform temperature conversions. This bit is nonvolatile.

For typical thermostat operation, the DS1621 will operate in continuous mode. However, for applications where only one reading is needed at certain times, and to conserve power, the one–shot mode may be used. Note that the thermostat output (T_{OUT}) will remain in the state it was in after the last valid temperature conversion cycle when operating in one–shot mode.

2–WIRE SERIAL DATA BUS

The DS1621 supports a bi–directional two–wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a "master". The devices that are controlled by the master are "slaves". The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START an d STOP conditions. The DS1621 operates as a slave on the two–wire bus. Connections to the bus are made via the open–drain I/O lines SDA and SCL.

The following bus protocol has been defined (See Figure 4):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

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Each data transfer is initiated with a START condition and terminated with a STOP condition The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte–wise and each receiver acknowledges with a ninth bit.

Within the bus specifications a regular mode (100 KHz clock rate) and a fast mode (400 KHz clock rate) are defined. The DS1621 works in both modes.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

DATA TRANSFER ON 2–WIRE SERIAL BUS Figure 4

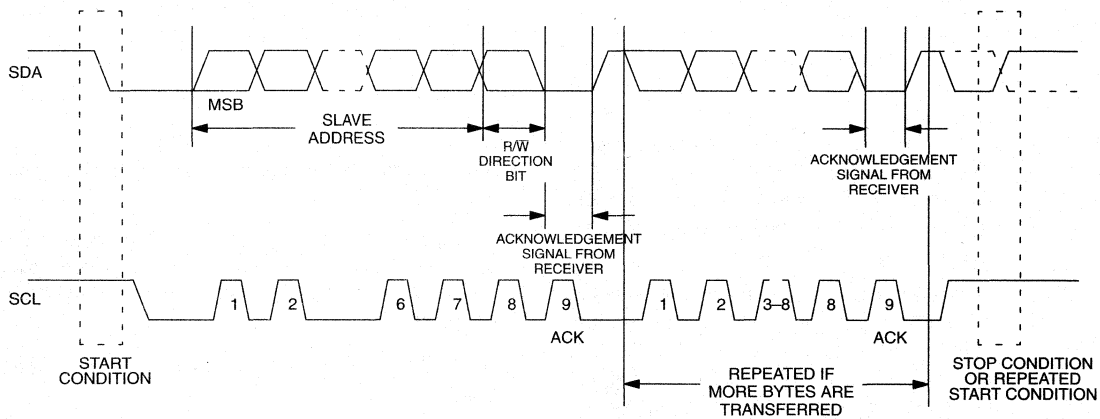


Figure 4 details how data transfer is accomplished on the two–wire bus. Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

1. **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.

2. **Data transfer from a slave transmitter to a master receiver.** The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a 'not acknowledge' is returned.

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

The DS1621 may operate in the following two modes:

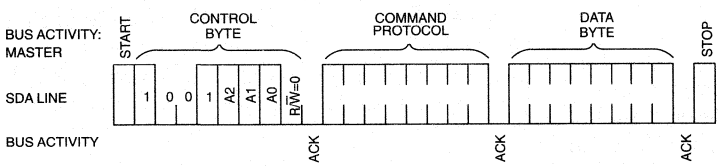
1. **Slave receiver mode:** Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.
2. **Slave transmitter mode:** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1621 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

SLAVE ADDRESS

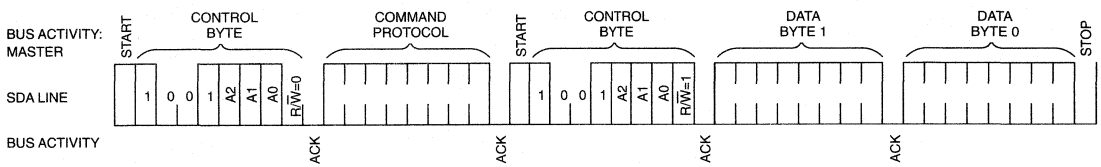
A control byte is the first byte received following the START condition from the master device. The control byte consists of a four bit control code; for the DS1621, this is set as 1001 binary for read and write operations. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used by the master device to select which of eight devices are to be accessed. These bits are in effect the three least significant bits of the slave address. The last bit of the control byte ($R/\overline{W}$) defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. Following the START condition, the DS1621 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving the 1001 code and appropriate device select bits, the slave device outputs an acknowledge signal on the SDA line.

2–WIRE SERIAL COMMUNICATION WITH DS1621 Figure 5

Write to DS1621



Read from DS1621



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COMMAND SET

Data and control information is read from and written to the DS1621 in the format shown in Figure 5. To write to the DS1621, the master will issue the slave address of the DS1621, and the R/$\overline{W}$ bit will be set to 0. After receiving an acknowledge, the bus master provides a command protocol. After receiving this protocol, the DS1621 will issue an acknowledge, and then the master may send data to the DS1621. If the DS1621 is to be read, the master must send the command protocol as before, and then issue a repeated START condition and the control byte again, this time with the R/$\overline{W}$ bit set to 1 to allow reading of the data from the DS1621. The command set for the DS1621 as shown in Table 3 is as follows:

Read Temperature [AAh]

This command reads the last temperature conversion result. The DS1621 will send two bytes, in the format described earlier, which are the contents of this register.

Access TH [A1h]

If R/$\overline{W}$ is 0, this command writes to the TH (HIGH TEMPERATURE) register. After issuing this command, the next two bytes written to the DS1621, in the same format as described for reading temperature, will set the high temperature threshold for operation of the T_{OUT} output. If R/$\overline{W}$ is 1, the value stored in this register is read back.

Access TL [A2h]

If R/$\overline{W}$ is 0, this command writes to the TL (LOW TEMPERATURE) register. After issuing this command, the next two bytes written to the DS1621, in the same format as described for reading temperature, will set the high temperature threshold for operation of the T_{OUT} output. If R/$\overline{W}$ is 1, the value stored in this register is read back.

Access Config [ACh]

If R/$\overline{W}$ is 0, this command writes to the configuration register. After issuing this command, the next data byte is the value to be written into the configuration register. If R/$\overline{W}$ is 1, the next data byte read is the value stored in the configuration register.

Read Counter [A8h]

This command reads the value of the counter byte. This command is valid only if R/$\overline{W}$ is 1.

Read Slope [A9h]

This command reads the value of the slope counter byte from the DS1621. This command is valid only if R/$\overline{W}$ is 1.

Start Convert T [EEh]

This command begins a temperature conversion. No further data is required. In one–shot mode, the temperature conversion will be performed and then the DS1621 will remain idle. In continuous mode, this command will initiate continuous conversions.

Stop Convert T [22h]

This command stops temperature conversion. No further data is required. This command may be used to halt a DS1621 in continuous conversion mode. After issuing this command, the current temperature measurement will be completed, and then the DS1621 will remain idle until a Start Convert T is issued to resume continuous operation.

DS1621 COMMAND SET Table 3

INSTRUCTION	DESCRIPTION	PROTOCOL	2–WIRE BUS DATA AFTER ISSUING PROTOCOL	NOTES
TEMPERATURE CONVERSION COMMANDS				
Read Temperature	Read last converted temperature value from temperature register.	AAh	<read 2 bytes data>	
Read Counter	Reads value of count remaining from counter.	A8h	<read data>	
Read Slope	Reads value of the slope accumulator.	A9h	<read data>	
Start Convert T	Initiates temperature conversion.	EEh	idle	1
Stop Convert T	Halts temperature conversion.	22h	idle	1
THERMOSTAT COMMANDS				
Access TH	Reads or writes high temperature limit value into TH register.	A1h	<write data>	2
Access TL	Reads or writes low temperature limit value into TL register.	A2h	<write data>	2
Access Config	Reads or writes configuration data to configuration register.	ACh	<write data>	2

NOTES:

1. In continuous conversion mode, a Stop Convert T command will halt continuous conversion. To restart, the Start Convert T command must be issued. In one–shot mode, a Start Convert T command must be issued for every temperature reading desired.
2. Writing to the E^2 typically requires 10ms at room temperature. After issuing a write command, no further writes should be requested for at least 10 ms.

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MEMORY FUNCTION EXAMPLE

Example: Bus master sets up DS1621 for continuous conversion and thermostatic function.

BUS MASTER MODE	DS1621 MODE	DATA (MSB FIRST)	COMMENTS
TX	RX	START	Bus Master initiates a START condition.
TX	RX	<address,0>	Bus Master sends DS1621 address; R/$\overline{W}$ = 0.
RX	TX	ACK	DS1621 generates acknowledge bit.
TX	RX	ACh	Bus Master sends Access Config command protocol.
RX	TX	ACK	DS1621 generates acknowledge bit.
TX	RX	02h	Bus Master sets up DS1621 for output polarity active high, continuous conversion.
RX	TX	ACK	DS1621 generates acknowledge bit.
TX	RX	START	Bus Master generates a repeated START condition.
TX	RX	<address,0>	Bus Master sends DS1621 address; R/$\overline{W}$ = 0.
RX	TX	ACK	DS1621 generates acknowledge bit.
TX	RX	A1h	Bus Master sends Access TH command.
RX	TX	ACK	DS1621 generates acknowledge bit.
TX	RX	28h	Bus Master sends first byte of data for TH limit of +40°C.
RX	TX	ACK	DS1621 generates acknowledge bit.
TX	RX	00h	Bus Master sends second byte of data for TH limit of +40°C.
RX	TX	ACK	DS1621 generates acknowledge bit.
TX	RX	START	Bus Master generates a repeated START condition.
TX	RX	<address,0>	Bus Master sends DS1621 address; R/$\overline{W}$ = 0.
RX	TX	ACK	DS1621 generates acknowledge bit.
TX	RX	A2h	Bus Master sends Access TL command.
RX	TX	ACK	DS1621 generates acknowledge bit.
TX	RX	0Ah	Bus Master sends first byte of data for TL limit of +10°C.
RX	TX	ACK	DS1621 generates acknowledge bit.
TX	RX	00h	Bus Master sends second byte of data for TL limit of +10°C.
RX	TX	ACK	DS1621 generates acknowledge bit.
TX	RX	START	Bus Master generates a repeated START condition.
TX	RX	<address,0>	Bus Master sends DS1621 address; R/$\overline{W}$ = 0.
RX	TX	ACK	DS1621 generates acknowledge bit.
TX	RX	EEh	Bus Master sends Start Convert T command protocol.
RX	TX	ACK	DS1621 generates acknowledge bit.
TX	RX	STOP	Bus Master initiates STOP condition.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to 7.0V
Operating Temperature	–55°C to +125°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD}	2.7		5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(–55°C to +125°C; V_{DD}=2.7V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Thermometer Error	T_{ERR}	0°C to 70°C	See Typical Curve		±1/2	°C	
Low Level Input Voltage	V_{IL}		–0.5		0.3 V_{DD}	V	
High Level Input Voltage	V_{IH}		0.7 V_{DD}		V_{DD}+0.5	V	
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	Fast Mode	0		50	ns	
Low Level Output Voltage	V_{OL1}	3 mA sink current	0		0.4	V	
	V_{OL2}	6 mA sink current	0		0.6	V	
Input Current each I/O Pin		$0.4<V_{I/O}<0.9V_{DD}$	–10		10	µA	2
I/O Capacitance	$C_{I/O}$				10	pF	
Active Supply Current	I_{CC}	Temperature Conversion E^2 Write Communication Only			1000 400 100	µA	3, 4
Standby Supply Current	I_{STBY}				1	µA	3, 4
Thermostat Output (T_{OUT}) Output Voltage	V_{OH}	1 mA source	2.4			V	
	V_{OL}	4 mA sink			0.4	V	

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AC ELECTRICAL CHARACTERISTICS

(–55°C to +125°C; V_{DD}=2.7V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Temperature Conversion Time	T_{TC}			1	2	s	
NV Write Cycle Time	t_{WR}	0°C to 70°C		10	50	ms	10
SCL Clock Frequency	f_{SCL}	Fast Mode Standard Mode	0 0		400 100	KHz	
Bus Free Time Between a STOP and START Condition	t_{BUF}	Fast Mode Standard Mode	1.3 4.7			µs	
Hold Time (Repeated) START Condition	$t_{HD:STA}$	Fast Mode Standard Mode	0.6 4.0			µs	5
Low Period of SCL Clock	t_{LOW}	Fast Mode Standard Mode	1.3 4.7			µs	
High Period of SCL Clock	t_{HIGH}	Fast Mode Standard Mode	0.6 4.0			µs	
Setup Time for a Repeated START Condition	$t_{SU:STA}$	Fast Mode Standard Mode	0.6 4.7			µs	
Data Hold Time	$t_{HD:DAT}$	Fast Mode Standard Mode	0 0		0.9	µs	6, 7
Data Setup Time	$t_{SU:DAT}$	Fast Mode Standard Mode	100 250			ns	8
Rise Time of both SDA and SCL Signals	t_R	Fast Mode Standard Mode	$20+0.1C_B$		300 1000	ns	9
Fall Time of both SDA and SCL Signals	t_F	Fast Mode Standard Mode	$20+0.1C_B$		300 300	ns	9
Setup time for STOP Condition	$t_{SU:STO}$	Fast Mode Standard Mode	0.6 4.0			µs	
Capacitive Load for each Bus Line	C_b				400	pF	

All values referred to V_{IH}=0.9 V_{DD} and V_{IL}=0.1 V_{DD}.

AC ELECTRICAL CHARACTERISTICS

(–55°C to +125°C; V_{DD}=2.7V to 5.5V)

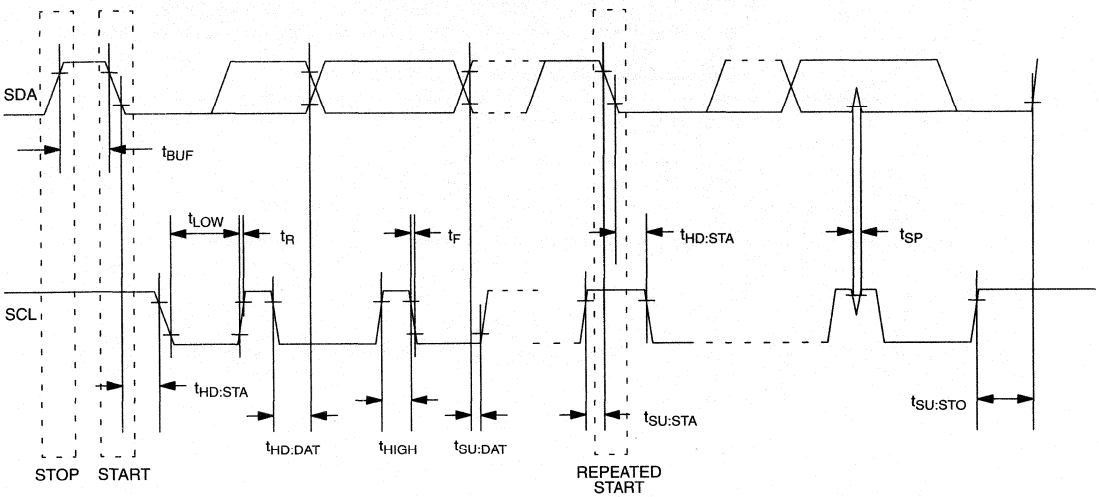
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_I		5		pF	

NOTES:

1. All voltages are referenced to ground.
2. I/O pins of fast mode devices must not obstruct the SDA and SCL lines if V_{DD} is switched off.
3. I_{CC} specified with T_{OUT} pin open.
4. I_{CC} specified with V_{CC} at 5.0V and SDA,SCL = 5.0V, 0°C to 70°C.

5. After this period, the first clock pulse is generated.
6. A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IH\ MIN}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
7. The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
8. A fast mode device can be used in a standard mode system, but the requirement $t_{SU:DAT}$ >250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{R\ MAX}+t_{SU:DAT}$ = 1000+250 = 1250 ns before the SCL line is released.
9. C_b – total capacitance of one bus line in pF.
10. Writing to the nonvolatile memory should only take place in the 0°C to +70°C temperature range.

TIMING DIAGRAM



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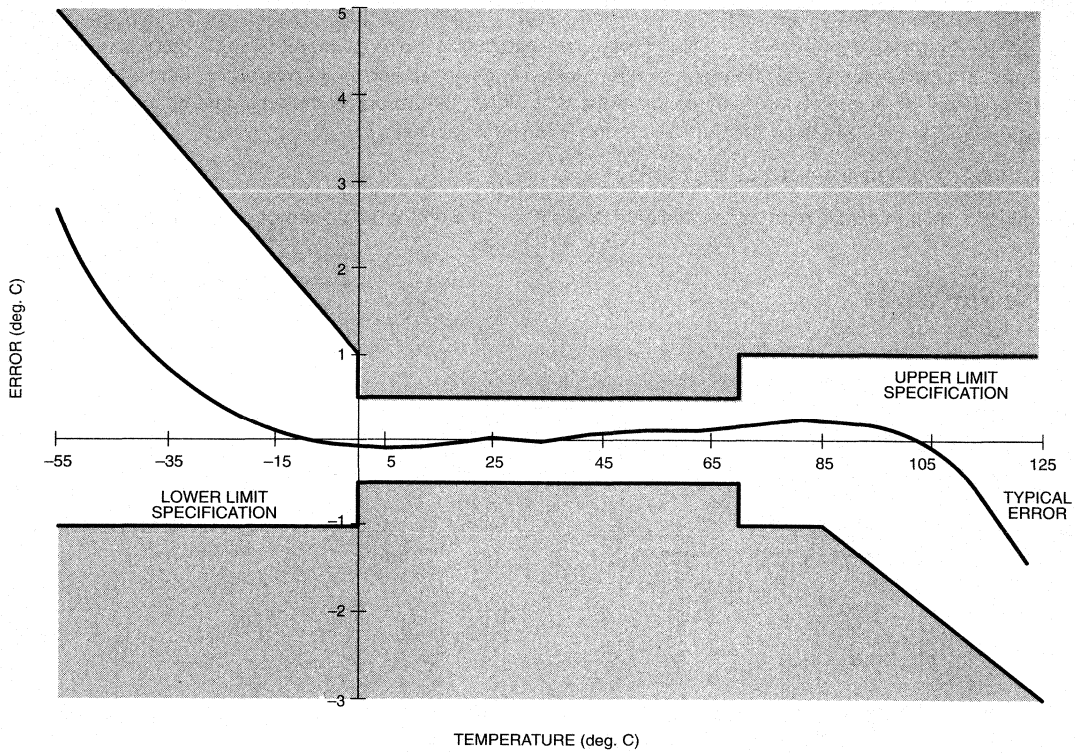
TYPICAL PERFORMANCE CURVE

DS1621 DIGITAL THERMOMETER AND THERMOSTAT
TEMPERATURE READING ERROR



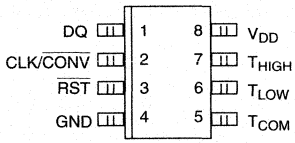
DALLAS SEMICONDUCTOR

DS1623
Digital Thermometer and Thermostat

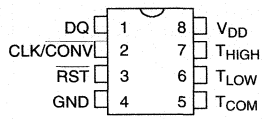
FEATURES

- Requires no external components
- Measures temperatures from –55°C to +125°C in 0.5°C increments. Fahrenheit equivalent is –67°F to 257°F in 0.9°F increments
- Temperature is read as a 9–bit value
- Converts temperature to digital word in 1 second
- Thermostatic settings are user–definable and non–volatile
- Data is read from/written via a 3–wire serial interface (CLK, DQ, $\overline{RST}$)
- Applications include thermostatic controls, industrial systems, consumer products, thermometers, or any thermally sensitive system
- 8–pin DIP or SOIC package

PIN ASSIGNMENT



DS1623S
8–PIN SOIC (208 MIL)
See Mech. Drawings Section



DS1623
8–PIN DIP
See Mech. Drawings Section

PIN DESCRIPTION

DQ	–	3–Wire Input/Output
CLK/$\overline{CONV}$	–	3–Wire Clock Input and Standalone Convert Input
$\overline{RST}$	–	3–Wire Reset Input
GND	–	Ground
T_{HIGH}	–	High Temperature Trigger
T_{LOW}	–	Low Temperature Trigger
T_{COM}	–	High/Low Combination Trigger
V_{DD}	–	Power Supply Voltage (+3.3V)

DESCRIPTION

The DS1623 Digital Thermometer and Thermostat provides 9–bit temperature readings which indicate the temperature of the device. With three thermal alarm outputs, the DS1623 can also act as a thermostat. T_{HIGH} is driven high if the DS1623's temperature is greater than or equal to a user–defined temperature TH. T_{LOW} is driven high if the DS1623's temperature is less than or equal to a user–defined temperature TL. T_{COM} is driven high when the temperature exceeds TH and stays high until the temperature falls below that of TL.

User–defined temperature settings are stored in non–volatile memory, so parts can be programmed prior to insertion in a system, as well as used in standalone applications without a CPU. Temperature settings and temperature readings are all communicated to/from the DS1623 over a simple 3–wire interface.

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060895 1/12

OPERATION–MEASURING TEMPERATURE

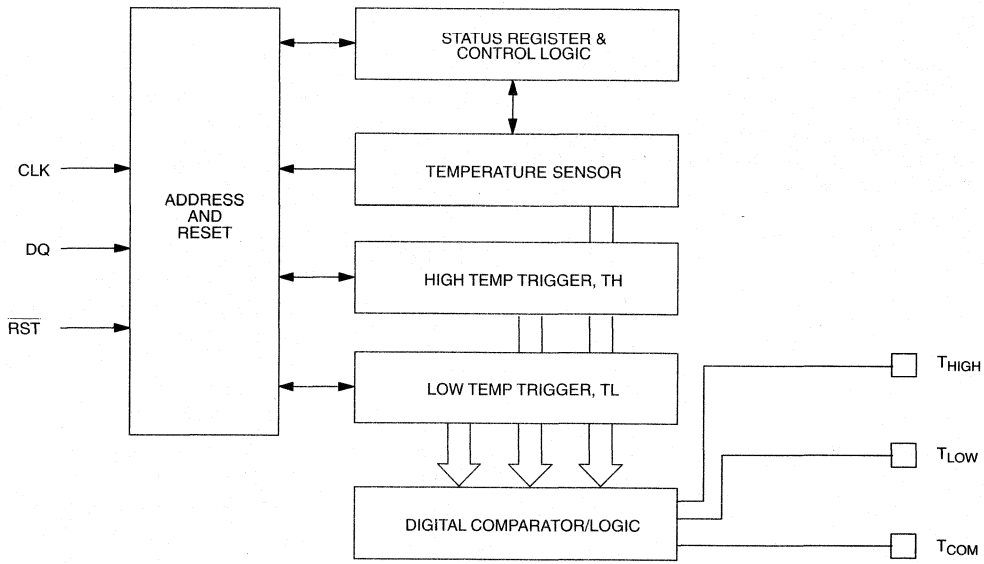
A block diagram of the DS1623 is shown in Figure 1. The DS1623 measures temperatures through the use of an on–board proprietary temperature measurement technique. A block diagram of the temperature measurement circuitry is shown in Figure 2.

The DS1623 measures temperature by counting the number of clock cycles that an oscillator with a low temperature coefficient goes through during a gate period determined by a high temperature coefficient oscillator. The counter is preset with a base count that corresponds to –55°C. If the counter reaches zero before the gate period is over, the temperature register, which is also preset to the –55°C value, is incremented, indicating that the temperature is higher than –55°C.

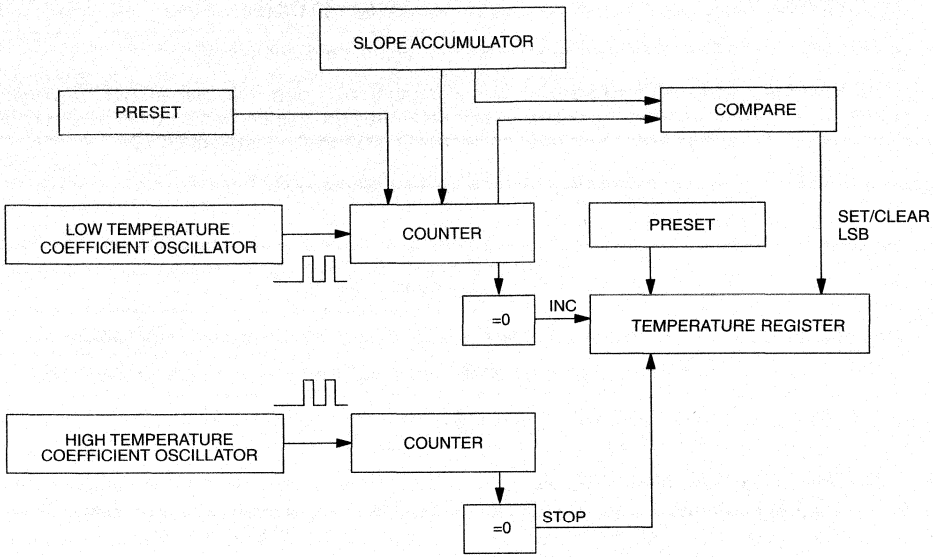
At the same time, the counter is then preset with a value determined by the slope accumulator circuitry. This circuitry is needed to compensate for the parabolic behavior of the oscillators over temperature. The counter is then clocked again until it reaches zero. If the gate period is still not finished, then this process repeats.

The slope accumulator is used to compensate for the nonlinear behavior of the oscillators over temperature, yielding a high resolution temperature measurement. This is done by changing the number of counts necessary for the counter to go through for each incremental degree in temperature. To obtain the desired resolution, therefore, both the value of the counter and the number of counts per degree C (the value of the slope accumulator) at a given temperature must be known.

DS1623 FUNCTIONAL BLOCK DIAGRAM Figure 1



TEMPERATURE MEASURING CIRCUITRY Figure 2



Internally, this calculation is doen inside the DS1623 to provide 0.5°C resolution. The temperature reading is provided in a 9–bit, two's complement reading by issuing a READ TEMPERATURE command. Table 1 describes the exact relationship of output data to measured temperature. The data is transmitted serially through the 3–wire serial interface, LSB first. The DS1623 can measure temperature over the range of –55°C to +125°C in 0.5°C increments. For Farenheit usage, a lookup table or conversion factor must be used.

TEMPERATURE/DATA RELATIONSHIPS Table 1

TEMP	DIGITAL OUTPUT (Binary)	DIGITAL OUTPUT (Hex)
+125°C	0 11111010	00FA
+25°C	0 00110010	0032h
+1/2°C	0 00000001	0001h
+0°C	0 00000000	0000h
–1/2°C	1 11111111	01FFh
–25°C	1 11001110	01CEh
–55°C	1 10010010	0192h

Since data is transmitted over the 3–wire bus LSB first, temperature data can be written to/read from the DS1623 as either a 9–bit word (taking $\overline{RST}$ low after the 9th (MSB) bit), or as two transfers of 8–bit words, with the most significant 7 bits being ignored or set to zero, as illustrated in Table 1. After the MSB, the DS1623 will output 0's.

Note that temperature is represented in the DS1623 in terms of a 1/2°C LSB, yielding the following 9–bit format:

MSB								LSB							
X	X	X	X	X	X	X	1	1	1	0	0	1	1	1	0

T = –25°C

Higher resolutions may be obtained by reading the temperature, and truncating the 0.5°C bit (the LSB) from the read value. This value is TEMP_READ. The value left in the counter may then be read by issuing a READ COUNTER command. This value is the count remaining (COUNT_REMAIN) after the gate period has ceased. By loading the value of the slope accumulator into the count register (using the READ SLOPE command), this value may then be read, yielding the number of counts per degree C (COUNT_PER_C) at that temperature. The actual temperature may be then be calculated by the user using the following:

$$TEMPERATURE = TEMP\_READ - 0.25 + \frac{(COUNT\_PER\_C - COUNT\_REMAIN)}{COUNT\_PER\_C}$$

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DETAILED PIN DESCRIPTION Table 2

PIN	SYMBOL	DESCRIPTION
1	DQ	**Data Input/Output pin** for 3–wire communication port.
2	CLK/$\overline{CONV}$	**Clock input pin** for 3–wire communication port. When the DS1623 is used in a standalone application with no 3–wire port, this pin can be used as a convert pin. Temperature conversion will begin on the falling edge of $\overline{CONV}$.
3	$\overline{RST}$	**Reset input pin** for 3–wire communication port.
4	GND	**Ground pin.**
5	T_{COM}	**High/Low Combination Trigger.** Goes high when temperature exceeds TH; will reset to low when temperature falls below TL.
6	T_{LOW}	**Low Temperature Trigger.** Goes high when temperature falls below TL.
7	T_{HIGH}	**High Temperature Trigger.** Goes high when temperature exceeds TH.
8	V_{DD}	**Supply Voltage.** 3.3V input power pin.

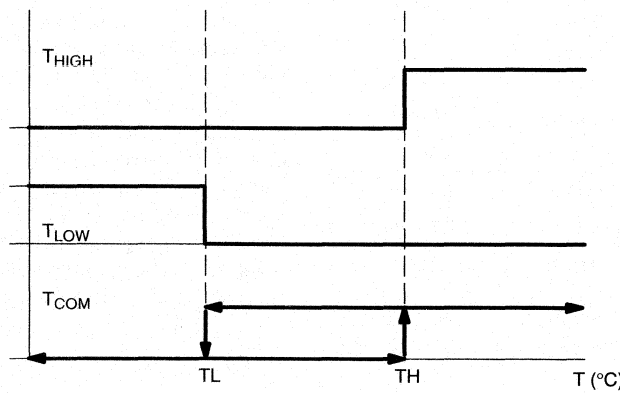
OPERATION–THERMOSTAT CONTROLS

Three thermally triggered outputs, T_{HIGH}, T_{LOW}, and T_{COM}, are provided to allow the DS1623 to be used as a thermostat, as shown in Figure 3. When the DS1623's temperature meets or exceeds the value stored in the high temperature trip register, the output T_{HIGH} becomes active (high) and remains active until the DS1623's measured temperature becomes less than the stored value in the high temperature register, TH. The T_{HIGH} output can be used to indicate that a high temperature tolerance boundary has been met or exceeded, or as part of a closed loop system can be used to activate a cooling system and to deactivate it when the system temperature returns to tolerance.

The T_{LOW} output functions similarly to the T_{HIGH} output. When the DS1623's measured temperature equals or falls below the value stored in the low temperature register, the T_{LOW} output becomes active. T_{LOW} remains active until the DS1623's temperature becomes greater than the value stored in the low temperature register, TL. The T_{LOW} output can be used to indicate that a low temperature tolerance boundary has been met or exceeded, or as part of a closed loop system, can be used to activate a heating system and to deactivate it when the system temperature returns to tolerance.

The T_{COM} output goes high when the measured temperature meets or exceeds TH, and will stay high until the temperature equals or falls below TL. In this way, any amount of hysteresis can be obtained.

THERMOSTAT OUTPUT OPERATION Figure 3



OPERATION AND CONTROL

The DS1623 must have temperature settings resident in the TH and TL registers for thermostatic operation. A configuration/status register is also used to determine the method of operation that the DS1623 will use in a particular application, as well as indicating the status of the temperature conversion operation. The configuration register is defined as follows:

CONFIGURATION/STATUS REGISTER

DONE	THF	TLF	NVB	1	0	CPU	1SHOT

where

DONE = Conversion Done bit. 1=conversion complete, 0=conversion in progress.

THF = Temperature High Flag. This bit will be set to 1 when the temperature is greater than or equal to the value of TH. It will remain 1 until reset by writing 0 into this location or by removing power from the device. This feature provides a method of determining if the DS1623 has ever been subjected to temperatures above TH while power has been applied.

TLF = Temperature Low Flag. This bit will be set to 1 when the temperature is less than or equal to the value of TL. It will remain 1 until reset by writing 0 into this location or by removing power from the device. This feature provides a method of determining if the DS1623 has ever been subjected to temperatures below TL while power has been applied.

NVB = Nonvolatile Memory Busy Flag. 1=write to an E^2 memory cell in progress. 0=nonvolatile memory is not busy. A copy to E^2 may take up to 10 ms.

CPU = CPU use bit. If CPU=0, the CLK/$\overline{\text{CONV}}$ pin acts as a conversion start control, when $\overline{\text{RST}}$ is low. If CPU is 1, the DS1623 will be used with a CPU communicating to it over the 3–wire port, and the operation of the CLK/$\overline{\text{CONV}}$ pin is as a normal clock in concert with DQ and $\overline{\text{RST}}$. This bit is stored in nonvolatile E^2 memory, capable of at least 50,000 writes.

1SHOT = One–Shot Mode. If 1SHOT is 1, the DS1623 will perform one temperature conversion upon reception of the Start Convert T protocol. If 1SHOT is 0, the DS1623 will continuously perform temperature conversion. This bit is stored in nonvolatile E^2 memory, capable of at least 50,000 writes.

For typical thermostat operation, the DS1623 will operate in continuous mode. However, for applications where only one reading is needed at certain times, and to conserve power, the one–shot mode may be used. Note that the thermostat outputs (T_{HIGH}, T_{LOW}, T_{COM}) will remain in the state they were in after the last valid temperature conversion cycle when operating in one–shot mode.

OPERATION IN STANDALONE MODE

In applications where the DS1623 is used as a simple thermostat, no CPU is required. Since the temperature limits are nonvolatile, the DS1623 can be programmed prior to insertion in the system. In order to facilitate operation without a CPU, the CLK/$\overline{\text{CONV}}$ pin (pin 2) can be used to initiate conversions. Note that the CPU bit must be set to 0 in the configuration register to use this mode of operation.

To use the CLK/$\overline{\text{CONV}}$ pin to initiate conversions, $\overline{\text{RST}}$ must be low and CLK/$\overline{\text{CONV}}$ must be high. If CLK/$\overline{\text{CONV}}$ is driven low and then brought high in less than 10 ms, one temperature conversion will be performed and then the DS1623 will return to an idle state. If CLK/$\overline{\text{CONV}}$ is driven low and remains low, continuous conversions will take place until CLK/$\overline{\text{CONV}}$ is brought high again. With the CPU bit set to 0, the CLK/$\overline{\text{CONV}}$ will override the 1–shot bit if it is equal to 1. This means that even if the part is set for one–shot mode, driving CLK/$\overline{\text{CONV}}$ low will initiate conversions.

3–WIRE COMMUNICATIONS

The 3–wire bus is comprised of three signals. These are the $\overline{\text{RST}}$ (reset) signal, the CLK (clock) signal, and the DQ (data) signal. All data transfers are initiated by driving the $\overline{\text{RST}}$ input high. Driving the $\overline{\text{RST}}$ input low terminates communication. (See Figures 4 and 5.) A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of a clock cycle. Data bits are output on the falling edge of the clock, and remain valid through the rising edge.

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When reading data from the DS1623, the DQ pin goes to a high impedance state while the clock is high. Taking $\overline{RST}$ low will terminate any communication and cause the DQ pin to go to a high impedance state.

Data over the 3–wire interface is communicated LSB first. The command set for the 3–wire interface as shown in Table 3 is as follows; only these protocols should be written to the DS1623, as writing other protocols to the device may result in permanent damage to the part.

Read Temperature [AAh]
This command reads the contents of the register which contains the last temperature conversion result. The next nine clock cycles will output the contents of this register.

Write TH [01h]
This command writes to the TH (HIGH TEMPERATURE) register. After issuing this command, the next nine clock cycles clock in the 9–bit temperature limit which will set the threshold for operation of the T_{HIGH} output.

Write TL [02h]
This command writes to the TL (LOW TEMPERATURE) register. After issuing this command, the next nine clock cycles clock in the 9–bit temperature limit which will set the threshold for operation of the T_{LOW} output.

Read TH [A1h]
This command reads the value of the TH (HIGH TEMPERATURE) register. After issuing this command, the next nine clock cycles clock out the 9–bit temperature limit which sets the threshold for operation of the T_{HIGH} output.

Read TL [A2h]
This command reads the value of the TL (LOW TEMPERATURE) register. After issuing this command, the next nine clock cycles clock out the 9–bit temperature limit which sets the threshold for operation of the T_{LOW} output.

Read Counter [A8h]
This command reads the value of the counter byte. The next nine clock cycles will output the contents of this register.

Read Slope [A9h]
This command reads the value of the slope counter byte from the DS1623. The next nine clock cycles will output the contents of this register.

Start Convert T [EEh]
This command begins a temperature conversion. No further data is required. In one–shot mode, the temperature conversion will be performed and then the DS1623 will remain idle. In continuous mode, this command will initiate continuous conversions.

Stop Convert T [22h]
This command stops temperature conversion. No further data is required. This command may be used to halt a DS1623 in continuous conversion mode. After issuing this command, the current temperature measurement will be completed, and then the DS1623 will remain idle until a Start Convert T is issued to resume continuous operation.

Write Config [0Ch]
This command writes to the configuration register. After issuing this command, the next eight clock cycles clock in the value of the configuration register.

Read Config [ACh]
This command reads the value in the configuration register. After issuing this command, the next eight clock cycles output the value of the configuration register.

DS1623 COMMAND SET Table 3

INSTRUCTION	DESCRIPTION	PROTOCOL	3–WIRE BUS DATA AFTER ISSUING PROTOCOL	NOTES
TEMPERATURE CONVERSION COMMANDS				
Read Temperature	Reads last converted temperature value from temperature register.	AAh	<read data>	
Read Counter	Reads value of count remaining from counter.	A8h	<read data>	
Read Slope	Reads value of the slope accumulator.	A9h	<read data>	
Start Convert T	Initiates temperature conversion.	EEh	idle	1
Stop Convert T	Halts temperature conversion.	22h	idle	1
THERMOSTAT COMMANDS				
Write TH	Writes high temperature limit value into TH register.	01h	<write data>	2
Write TL	Writes low temperature limit value into TL register.	02h	<write data>	2
Read TH	Reads stored value of high temperature limit from TH register.	A1h	<read data>	2
Read TL	Reads stored value of low temperature limit from TL register.	A2h	<read data>	2
Write Config	Writes configuration data to configuration register.	0Ch	<write data>	2
Read Config	Reads configuration data from configuration register.	ACh	<read data>	2

NOTES:

1. In continuous conversion mode, a Stop Convert T command will halt continuous conversion. To restart, the Start Convert T command must be issued. In one–shot mode, a Start Convert T command must be issued for every temperature reading desired.
2. Writing to the E^2 typically requires 10 ms at room temperature. After issuing a write command, no further writes should be requested for at least 10 ms.
3. Each instruction must be preceded by a reset.

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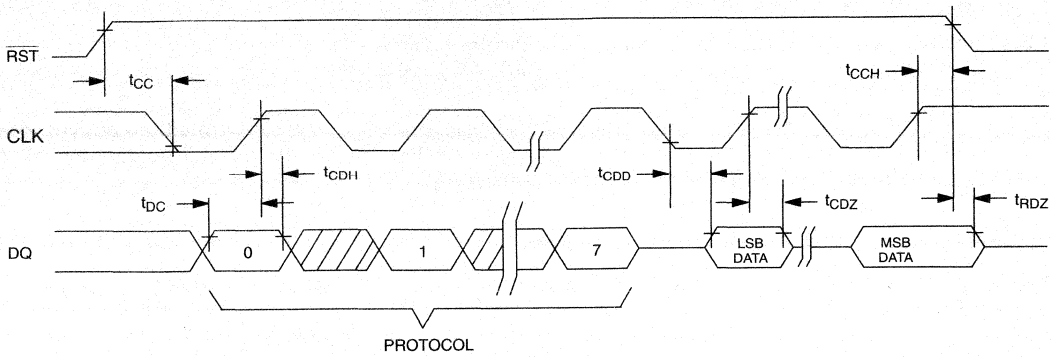
FUNCTION EXAMPLE

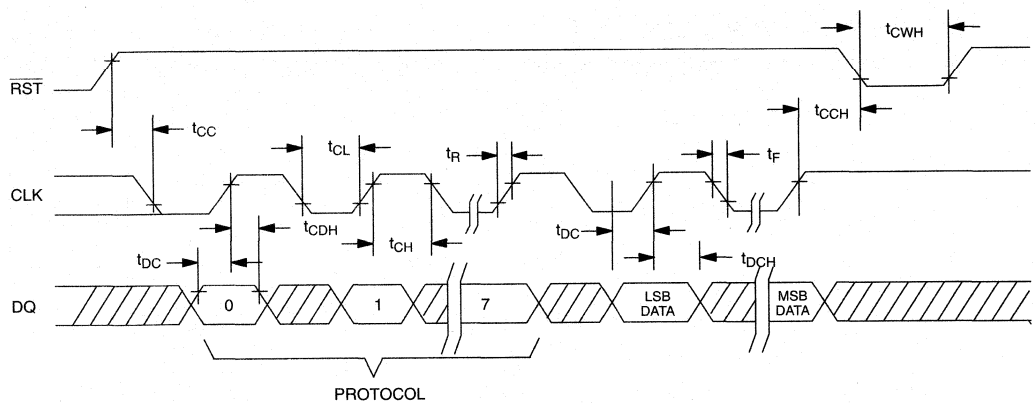
Example: CPU sets up DS1623 for continuous conversion and thermostatic function.

CPU MODE	DS1623 MODE (3–WIRE)	DATA (LSB FIRST)	COMMENTS
TX	RX	0Ch	CPU issues Write Config command.
TX	RX	00h	CPU sets DS1623 up for continuous conversion.
TX	RX	Toggle $\overline{RST}$	CPU issues Reset to DS1623.
TX	RX	01h	CPU issues Write TH command.
TX	RX	0050h	CPU sends data for TH limit of +40°C.
TX	RX	Toggle $\overline{RST}$	CPU issues Reset to DS1623.
TX	RX	02h	CPU issues Write TL command.
TX	RX	0014h	CPU sends data for TL limit of +10°C.
TX	RX	Toggle $\overline{RST}$	CPU issues Reset to DS1623.
TX	RX	A1h	CPU issues Read TH command.
RX	TX	0050h	DS1623 sends back stored value of TH for CPU to verify.
TX	RX	Toggle $\overline{RST}$	CPU issues Reset to DS1623.
TX	RX	A2h	CPU issues Read TL command.
RX	TX	0014h	DS1623 sends back stored value of TL for CPU to verify.
TX	RX	Toggle $\overline{RST}$	CPU issues Reset to DS1623.
TX	RX	EEh	CPU issues Start Convert T command.
TX	RX	Toggle $\overline{RST}$	CPU issues Reset to DS1623.

READ DATA TRANSFER Figure 4



WRITE DATA TRANSFER Figure 5



NOTE: t_{CL}, t_{CH}, t_R, and t_F apply to both read and write data transfer.

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	–55°C to +125°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

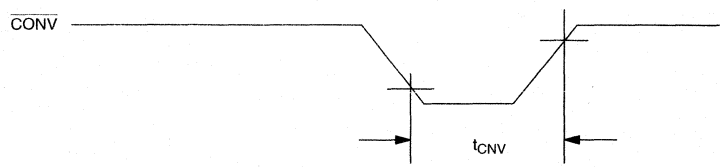
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply	V_{DD}	2.7		5.5	V	1
Logic 1	V_{IH}	2.0		V_{CC}+0.3	V	1
Logic 0	V_{IL}	–0.3		+0.6	V	1

DC ELECTRICAL CHARACTERISTICS

(–55°C to +125°C; V_{DD}=2.7V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	MAX	UNITS	NOTES
Thermometer Error	T_{ERR}	0°C to +70°C		±1/2	°C	10, 11
		–55°C to +0°C and 70°C to 125°C	See Typical Curve			
Logic 0 Output	V_{OL}			0.4	V	3
Logic 1 Output	V_{OH}		2.4		V	2
Input Resistance	R_I	$\overline{RST}$ to GND DQ,CLK to V_{DD}		2 2	MΩ MΩ	
Active Supply Current	I_{CC}	0°C to +70°C		1	mA	4, 5
Standby Supply Current	I_{STBY}	0°C to +70°C		1	µA	4, 5

SINGLE CONVERT TIMING DIAGRAM (STAND–ALONE MODE)



AC ELECTRICAL CHARACTERISTICS

(–55°C to +125°C; V_{DD}=2.7V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Temperature Conversion Time	T_{TC}		200	500	ms	
Data to CLK Setup	t_{DC}	35			ns	6
CLK to Data Hold	t_{CDH}	40			ns	6
CLK to Data Delay	t_{CDD}			100	ns	6, 7, 8
CLK Low Time	t_{CL}	325			ns	6
CLK High Time	t_{CH}	325			ns	6
CLK Frequency	f_{CLK}	DC		1.50	MHz	6
CLK Rise and Fall	t_R, t_F			500	ns	
$\overline{RST}$ to CLK Setup	t_{CC}	100			ns	6
CLK to $\overline{RST}$ Hold	t_{CCH}	40			ns	6
$\overline{RST}$ Inactive Time	t_{CWH}	125			ns	6, 9
CLK High to I/O High Z	t_{CDZ}			50	ns	6
$\overline{RST}$ Low to I/O High Z	t_{RDZ}			50	ns	6
Convert Pulse Width	t_{CNV}	250 ns		500 ms		
NV Write Cycle Time	t_{WR}		10	50	ms	12

AC ELECTRICAL CHARACTERISTICS

(–55°C to +125°C; V_{DD}=2.7V to 5.5V)

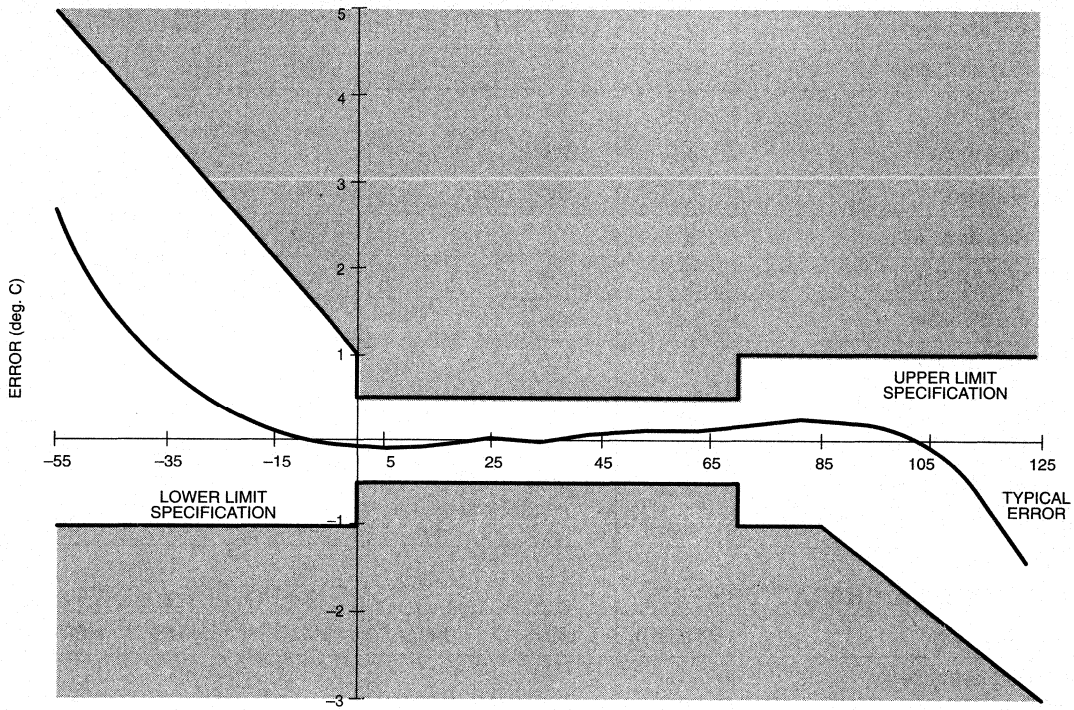
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_I		5		pF	
I/O Capacitance	$C_{I/O}$		10		pF	

NOTES:

1. All voltages are referenced to ground.
2. Logic one voltages are specified at a source current of 1 mA.
3. Logic zero voltages are specified at a sink current of 4 mA.
4. I_{CC} specified with DQ pin open and CLK pin at V_{DD}.
5. I_{CC} specified with V_{CC} at 3.3V and $\overline{RST}$=GND.
6. Measured at V_{IH} = 2.0V or V_{IL} = 0.6V.
7. Measured at V_{OH} = 2.4V or V_{OL} = 0.4V.
8. Load capacitance = 50 pF.
9. t_{CWH} must be 10 ms minimum following any write command that involves the E^2 memory.
10. See typical curve for specification limits outside 0°C to 70°C range.
11. Thermometer error specified from V_{CC}=2.7V to 5.5V)
12. Writing to the nonvolatile memory should only take place in the 0°C to +70°C temperature range.

TYPICAL PERFORMANCE CURVE

DS1623 DIGITAL THERMOMETER AND THERMOSTAT
TEMPERATURE READING ERROR



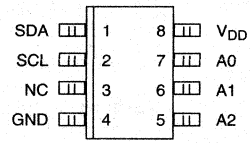
DALLAS SEMICONDUCTOR

DS1624
Digital Thermometer and Memory

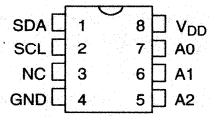
FEATURES

- Temperature measurements require no external components
- Measures temperatures from –55°C to +125°C in 0.03125°C increments. Fahrenheit equivalent is –67°F to 257°F in 0.05625°F increments
- Temperature is read as a 13–bit value (two byte transfer)
- Converts temperature to digital word in 200 ms, typical
- 256 bytes of E^2 memory on board for storing information such as frequency compensation coefficients
- Data is read/written via a 2–wire serial interface (open drain I/O lines)
- Applications include temperature–compensated crystal oscillators for test equipment and radio systems
- 8–pin DIP or SOIC package

PIN ASSIGNMENT



DS1624S
8–PIN SOIC (208 MIL)
See Mech. Drawings Section



DS1624
8–PIN DIP (300 MIL)
See Mech. Drawings Section

PIN DESCRIPTION

SDA	–	2–Wire Serial Data Input/Output
SCL	–	2–Wire Serial Clock
GND	–	Ground
A0	–	Chip Address Input
A1	–	Chip Address Input
A2	–	Chip Address Input
V_{DD}	–	Digital Power Supply (+3V– +5V)
NC	–	No Connection

DESCRIPTION

The DS1624 consists of a digital thermometer and 256 bytes of E^2 memory. The thermometer provides 13-bit temperature readings which indicate the temperature of the device. The E^2 memory allows a user to store frequency compensation coefficients for digital correction of crystal frequency due to temperature. Any other type of information may also reside in this user space.

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041095 1/15

DETAILED PIN DESCRIPTION Table 1

PIN	SYMBOL	DESCRIPTION
1	SDA	**Data input/output pin** for 2–wire serial communication port.
2	SCL	**Clock input/output pin** for 2–wire serial communication port.
3	NC	**No Connect**. No Internal Connection
4	GND	**Ground pin.**
5	A2	**Address input pin.**
6	A1	**Address input pin.**
7	A0	**Address input pin.**
8	V_{DD}	**Supply Voltage** 3V to 5V input power pin.

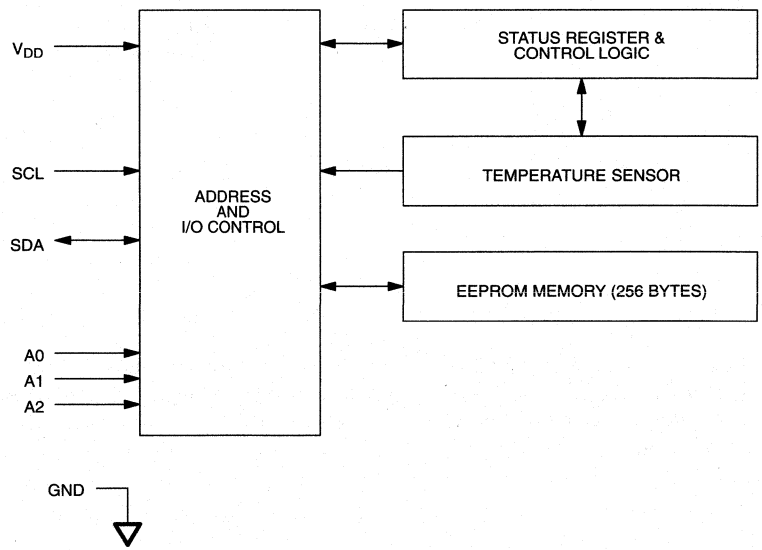
OVERVIEW

A block diagram of the DS1624 is shown in Figure 1. The DS1624 consists of two separate functional units: 1) a 256–byte nonvolatile E^2 memory, and 2) a direct–to–digital temperature sensor.

The nonvolatile memory is made up of 256 bytes of E^2 memory. This memory may be used to store any type of information the user wishes; for example, frequency compensation coefficients may be placed in this memory to allow for compensation of measured frequency depending upon the temperature at which the measurement is made. These memory locations are accessed through the 2–wire serial bus.

The direct to digital temperature sensor allows the DS1624 to measure the ambient temperature and report the temperature value in a 13–bit word, with 0.03125°C resolution. The temperature sensor and its related registers are accessed through the 2–wire serial interface.

DS1624 FUNCTIONAL BLOCK DIAGRAM Figure 1



2–WIRE SERIAL DATA BUS

The DS1624 supports a bi–directional two–wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a "master". The devices that are controlled by the master are "slaves". The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START an d STOP conditions. The DS1624 operates as a slave on the two–wire bus. Connections to the bus are made via the open–drain I/O lines SDA and SCL. The following bus protocol has been defined (See Figure 2):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte–wise and each receiver acknowledges with a ninth bit.

Within the bus specifications a regular mode (100 KHz clock rate) and a fast mode (400 KHz clock rate) are defined. The DS1624 works in both modes.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

DATA TRANSFER ON 2–WIRE SERIAL BUS Figure 2

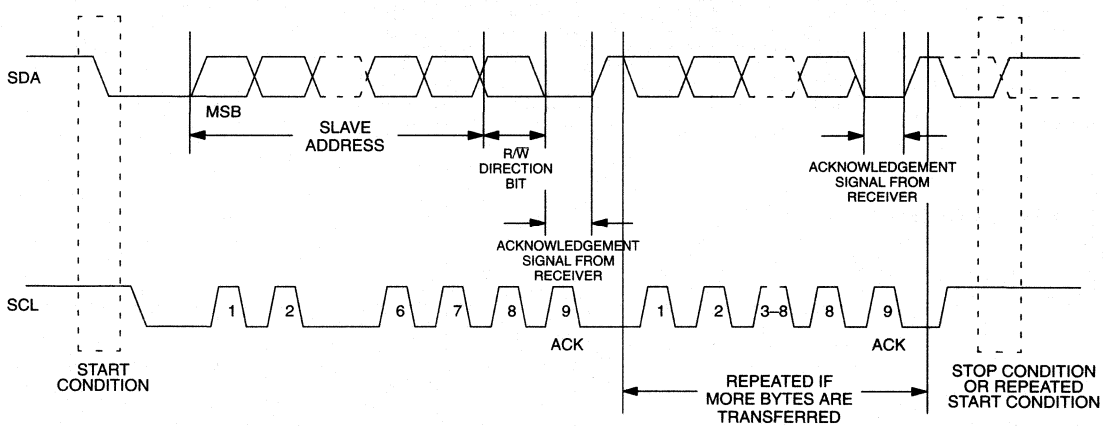


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Figure 2 details how data transfer is accomplished on the two–wire bus. Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

1. **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.
2. **Data transfer from a slave transmitter to a master receiver.** The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a 'not acknowledge' is returned.

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

The DS1624 may operate in the following two modes:

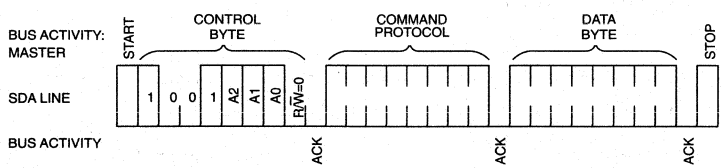
1. **Slave receiver mode:** Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.
2. **Slave transmitter mode:** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1624 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

SLAVE ADDRESS

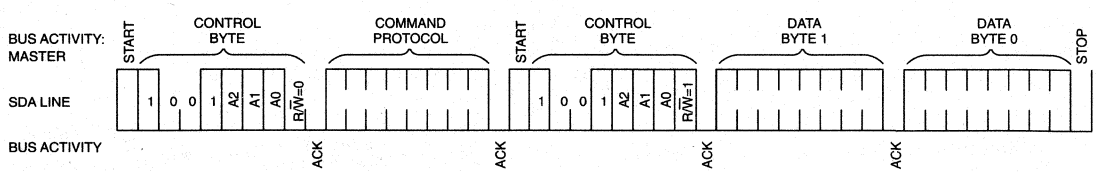
A control byte is the first byte received following the START condition from the master device. The control byte consists of a four bit control code; for the DS1624, this is set as 1001 binary for read and write operations. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used by the master device to select which of eight devices are to be accessed. These bits are in effect the three least significant bits of the slave address. The last bit of the control byte (R/$\overline{W}$) defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. Following the START condition, the DS1624 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving the 1001 code and appropriate device select bits, the slave device outputs an acknowledge signal on the SDA line.

2–WIRE SERIAL COMMUNICATION WITH DS1624 Figure 3

Write to DS1624



Read from DS1624



OPERATION–MEASURING TEMPERATURE

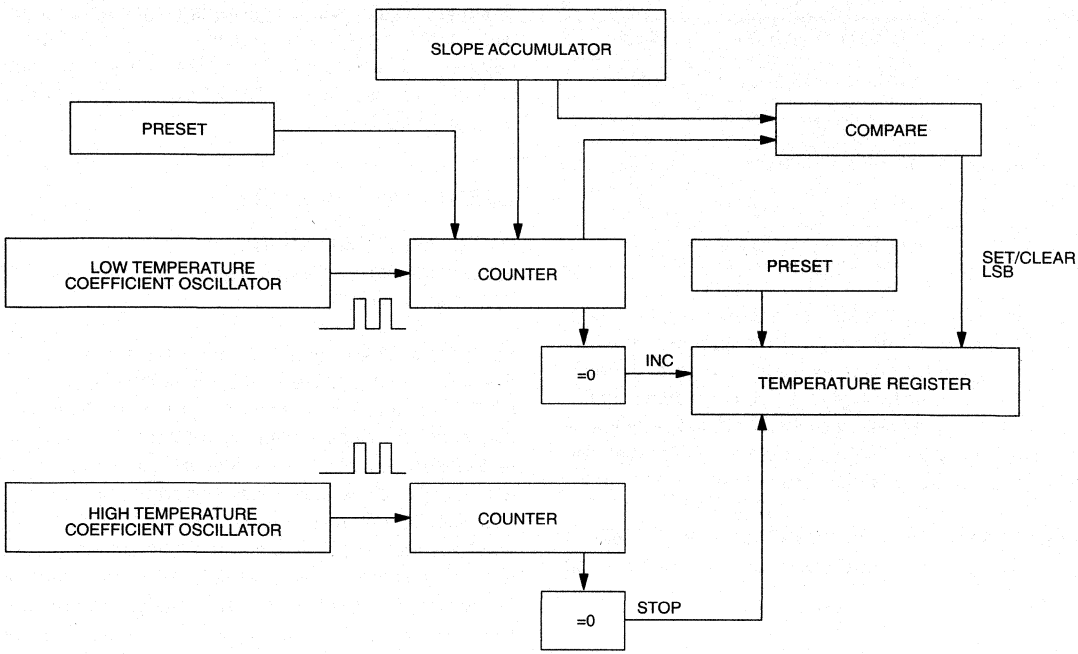
A block diagram of the DS1624 is shown in Figure 1.The DS1624 measures temperatures through the use of an on–board proprietary temperature measurement technique. A block diagram of the temperature measurement circuitry is shown in Figure 4.

The DS1624 measures temperature by counting the number of clock cycles that an oscillator with a low temperature coefficient goes through during a gate period determined by a high temperature coefficient oscillator. The counter is preset with a base count that corresponds to –55°C. If the counter reaches zero before the gate period is over, the temperature register, which is also preset to the –55°C value, is incremented, indicating that the temperature is higher than –55°C.

At the same time, the counter is then preset with a value determined by the slope accumulator circuitry. This circuitry is needed to compensate for the parabolic behavior of the oscillators over temperature. The counter is then clocked again until it reaches zero. If the gate period is still not finished, then this process repeats.

The slope accumulator is used to compensate for the nonlinear behavior of the oscillators over temperature, yielding a high resolution temperature measurement. This is done by changing the number of counts necessary for the counter to go through for each incremental degree in temperature. To obtain the desired resolution, therefore, both the value of the counter and the number of counts per degree C (the value of the slope accumulator) at a given temperature must be known.

TEMPERATURE MEASURING CIRCUITRY Figure 4



10

Internally, this calculation is performed by the DS1624 to provide 0.03125°C resolution. The temperature reading is provided in a 13–bit, two's complement reading by issuing READ TEMPERATURE command. Table 2 describes the exact relationship of output data to measured temperature. The data is transmitted serially through the 2–wire serial interface, MSB first. The DS1624 can measure temperature over the range of –55°C to +125°C in 0.03125°C increments. For Fahrenheit usage, a lookup table or conversion factor must be used.

TEMPERATURE/DATA RELATIONSHIPS

Table 2

TEMP	DIGITAL OUTPUT (Binary)	DIGITAL OUTPUT (Hex)
+125°C	01111101 00000000	7B00h
+25.0625°C	00011001 00010000	1910h
+1/2°C	00000000 10000000	0080h
+0°C	00000000 00000000	0070h
–1/2°C	11111111 10000000	FF80h
–25.0625°C	11100110 11110000	E6F0h
–55°C	11001001 00000000	C900h

Since data is transmitted over the 2–wire bus MSB first, temperature data may be written to/read from the DS1624 as either a single byte (with temperature resolution of 1°C), or as two bytes, the second byte containing the value of the 5 least significant bits of the temperature reading, as shown in Table 1. Note that the remaining three bits of this byte are set to all 0's.

Note that temperature is represented in the DS1624 in terms of a 0.03125°C LSB, yielding the following 13–bit format:

MSB LSB

0	0	0	1	1	0	0	1	0	0	0	1	0	0	0	0

= –25.0625°C

OPERATION AND CONTROL

A configuration/status register is used to determine the method of operation that the DS1624 will use in a particular application, as well as indicating the status of the temperature conversion operation.

The configuration register is defined as follows:

CONFIGURATION/STATUS REGISTER

DONE	1	0	0	1	0	1	1SHOT

where

DONE= Conversion Done bit. "1" = Conversion complete, "0" = conversion in progress.

1SHOT= One Shot Mode. If 1SHOT is "1", the DS1624 will perform one temperature conversion upon reception of the Start Convert T protocol. If 1SHOT is "0", the DS1624 will continuously perform temperature conversions. This bit is nonvolatile.

Since the configuration register is implemented in E^2, writes to the register require 10 ms to complete. After issuing a command to write to the configuration register, no further accesses to the DS1624 should be made for at least 10 ms.

OPERATION – MEMORY

BYTE PROGRAM MODE

In this mode, the master sends addresses and one data byte to the DS1624.

Following a START condition, the device code (4–bit), the slave address (3 bit), and the R/$\overline{W}$ bit, which is logic LOW, are placed onto the bus by the master. The master then sends the Access Memory protocol. This indicates to the addressed DS1624 that a byte with a word address will follow after it has generated an acknowledge bit. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the DS1624. After receiving the acknowledge of the DS1624, the master device transmits the data word to be written into the addressed memory location. The DS1624 acknowledges again and the master generates a STOP condition. This initiates the internal programming cycle of the DS1624. A repeated START condition, instead of a STOP condition, will abort the programming operation.

During the programming cycle, the DS1624 will not acknowledge any further accesses to the device until the programming cycle is complete (approximately 10 ms.)

PAGE PROGRAM MODE

To program the DS1624, the master sends addresses and data to the DS1624 which is the slave. This is done by supplying a START condition followed by the 4–bit device code, the 3–bit slave address, and the R/$\overline{W}$ bit which is defined as a logic LOW for a write. The master then sends the Access Memory protocol. This indicates to the addressed slave that a word address will follow so the slave outputs the acknowledge pulse to the master during the ninth clock pulse. When the word address is received by the DS1624, it is placed in the address pointer defining which memory location is to be written. The DS1624 will generate an acknowledge after every 8–bits received and store them consecutively in an 8–byte RAM until a STOP condition is detected which initiates the internal programming cycle.

A repeated START condition, instead of a STOP condition, will abort the programming operation.During the programming cycle, the DS1624 will not acknowledge any further accesses to the device until the programming cycle is complete (approximately 10 ms).

If more than 8 bytes are transmitted by the master, the DS1624 will roll over and overwrite the data beginning with the first received byte. This does not affect erase/write cycles of the EEPROM array and is accomplished as a result of only allowing the address register's bottom 3 bits to increment while the upper 5 bits remain unchanged.

If the master generates a STOP condition after transmitting the first data word, byte programming mode is entered.

READ MODE

In this mode, the master is reading data from the DS1624 E^2 memory. The master first provides the slave address to the device, with R/$\overline{W}$ set to 0. The master then sends the Access Memory protocol, and, after receiving an acknowledge, then provides the word address, which is the address of the memory location at which it wishes to begin reading. Note that while this is a read operation, the address pointer must first be written. During this period the DS1624 generates acknowledge bits as defined in the appropriate section.

The master now generates another START condition and transmits the slave address again, except this time the R/$\overline{W}$ bit is set to 1, to put the DS1624 in read mode. After the DS1624 generates the acknowledge bit, it then outputs the data from the addressed location on the SDA pin, increments the address pointer and, if it receives an acknowledge from the master, will transmit the next consecutive byte. This autoincrement sequence is only aborted when the master sends a STOP condition instead of an acknowledge. When the address pointer reaches the end of the 256–byte memory space (address FFh), it will increment from the end of the memory back to the first location of the memory (address 00h).

COMMAND SET

Data and control information is read from and written to the DS1624 in the format shown in Figure 3. To write to the DS1624, the master will issue the slave address of the DS1624, and the R/$\overline{W}$ bit will be set to 0. After receiving an acknowledge, the bus master provides a command protocol. After receiving this protocol, the DS1624 will issue an acknowledge, and then the master may send data to the DS1624. If the DS1624 is to be read, the master must send the command protocol as before, and then issue a repeated START condition and the control byte again, this time with the R/$\overline{W}$ bit set to 1 to allow reading of the data from the DS1624. The command set for the DS1624 as shown in Table 3 is as follows:

Access Memory [17h]

This command instructs the DS1624 to access its E^2 memory. After issuing this command, the next data byte is the value of the word address to be accessed. See OPERATION–MEMORY section for detailed explanations of the use of this protocol and data format following it.

Access Config [ACh]

If R/$\overline{W}$ is 0, this command writes to the configuration register. After issuing this command, the next data byte is value to be written into the configuration register. If R/$\overline{W}$ is 1, the next data byte read is the value store d in the configuration register.

Read Temperature [AAh]

This command reads the last temperature conversion result. The DS1624 will send two bytes, in the format described earlier, which are the contents of this register.

Start Convert T [EEh]

This command begins a temperature conversion. No further data is required. In one–shot mode, the temperature conversion will be performed and then the DS1624 will remain idle. In continuous mode, this command will initiate continuous conversions.

Stop Convert T [22h]

This command stops temperature conversion. No further data is required. This command may be used to halt a DS1624 in continuous conversion mode. After issuing this command, the current temperature measurement will be completed, and then the DS1624 will remain idle until a Start Convert T is issued to resume continuous operation.

DS1624 COMMAND SET Table 3

INSTRUCTION	DESCRIPTION	PROTOCOL	2–WIRE BUS DATA AFTER ISSUING PROTOCOL	NOTES
TEMPERATURE CONVERSION COMMANDS				
Read Temperature	Read last converted temperature value from temperature register.	AAh	<read 2 bytes data>	
Start Convert T	Initiates temperature conversion.	EEh	idle	1
Stop Convert T	Halts temperature conversion.	22h	idle	1
MEMORY COMMANDS				
Access Memory	Reads or writes to 256–byte EEPROM memory.	17h	<write data>	2
Access Config	Reads or writes configuration data to configuration register.	ACh	<write data>	2

NOTES:

1. In continuous conversion mode, a Stop Convert T command will halt continuous conversion. To restart, the Start Convert T command must be issued. In one–shot mode, a Start Convert T command must be issued for every temperature reading desired.
2. Writing to the E^2 typically requires 10 ms at room temperature. After issuing a write command, no further reads or writes should be requested for at least 10 ms.

   During the programming cycle, the DS1624 will not acknowledge any further accesses to the device until the programming cycle is complete (approximately 10 ms).

MEMORY FUNCTION EXAMPLE

BUS MASTER MODE	DS1624 MODE	DATA (MSB FIRST)	COMMENTS	NOTES
{Command protocol for configuration register} {Start here}				
TX	RX	START	Bus Master Initiates a Start condition	
TX	RX	<cadr,0>	Bus Master sends DS1624 address; R/$\overline{W}$=0;	
RX	TX	ACK	DS1624 generates acknowledge bit.	
TX	RX	ACh	Bus Master sends Access Config command protocol	
RX	TX	ACK	DS1624 generates acknowledge bit.	1
TX	RX	00h	Bus Master sets up DS1624 for continuous conversion	
RX	TX	ACK	DS1624 generates acknowledge bit.	2
{Command protocol for Start Convert T} {Start here}				
TX	RX	START	Bus Master initiates a Start condition	
TX	RX	<cadr,0>	Bus Master sends DS1624 address; R/$\overline{W}$=0;	
RX	TX	ACK	DS1624 generates acknowledge bit.	
TX	RX	EEh	Bus Master sends Start Convert T command protocol	
RX	TX	ACK	DS1624 generates acknowledge bit.	1
TX	RX	STOP	Bus Master initiates the STOP condition	
{Command protocol for reading the Temperature} {Start here}				
TX	RX	START	Bus Master initiates a Start condition	
TX	RX	<cadr, 0>	Bus Master sends DS1624 address; R/$\overline{W}$=0;	
RX	TX	ACK	DS1624 generates acknowledge bit.	
TX	RX	AAh	Bus Master sends Read Temp command protocol	
RX	TX	ACK	DS1624 generates acknowledge bit.	1
TX	RX	START	Bus Master initiates a Start condition	
TX	RX	<cadr,1>	Bus Master sends DS1624 address: R/$\overline{W}$=1;	
RX	TX	ACK	DS1624 generates acknowledge bit.	
RX	TX	<data>	DS1624 sends the MSB byte of Temperature.	
TX	RX	ACK	Bus Master generates acknowledge bit.	
RX	TX	<data>	DS1624 sends the LSB byte of Temperature.	
TX	RX	STOP	Bus Master Initiates the STOP condition.	
{Command protocol for writing to EEPROM} {Start here}				

BUS MASTER MODE	DS1624 MODE	DATA (MSB FIRST)	COMMENTS	NOTES
TX	RX	START	Bus Master initiates a Start condition	
TX	RX	<cadr,0>	Bus Master sends DS1624 address; R/$\overline{W}$=0;	
RX	TX	ACK	DS1624 generates acknowledge bit.	
TX	RX	17h	Bus Master sends Access Memory command protocol	
RX	TX	ACK	DS1624 generates acknowledge bit.	1
TX	RX	<madr>	Bus Master sends the starting memory address.	
RX	TX	ACK	DS1624 generates acknowledge bit.	
TX	RX	<data>	Bus Master sends the first byte of data.	
RX	TX	ACK	DS1624 generates acknowledge bit.	
TX	RX	<data>	Bus Master sends the second byte of data.	
RX	TX	ACK	DS1624 generates acknowledge bit.	
.	.	.	.	
.	.	.	.	
.	.	.	.	
.	.	.	.	
TX	RX	<data>	Bus Master sends the n-th byte of data.	3
RX	TX	ACK	DS1624 generates acknowledge bit.	
TX	RX	STOP	Bus Master initiates the STOP condition.	4
{Command protocol for reading from EEPROM} {Start here}				
TX	RX	START	Bus Master initiates a Start condition	
TX	RX	<cadr,0>	Bus Master sends DS1624 address; R/$\overline{W}$=0;	
RX	TX	ACK	DS1624 generates acknowledge bit.	
TX	RX	17h	Bus Master sends Access Memory command protocol	
RX	TX	ACK	DS1624 generates acknowledge bit.	1
TX	RX	<madr>	Bus Master sends the starting memory address.	
RX	TX	ACK	DS1624 generates acknowledge bit.	
TX	RX	START	Bus Master initiates a Start condition	
TX	RX	<cadr,1>	Bus Master sends DS1624 address: R/$\overline{W}$=1;	
RX	TX	ACK	DS1624 generates acknowledge bit.	
RX	TX	<data>	DS1624 sends the first byte of data.	
TX	RX	ACK	Bus Master generates acknowledge bit.	

BUS MASTER MODE	DS1624 MODE	DATA (MSB FIRST)	COMMENTS	NOTES
RX	TX	<data>	DS1624 sends the second byte of data.	
TX	RX	ACK	Bus Master generates acknowledge bit.	
•	•	•	•	
•	•	•	•	
•	•	•	•	
•	•	•	•	
RX	TX	<data>	DS1624 sends the n-th byte of data.	5
TX	RX	STOP	Bus Master initiates the STOP condition.	

NOTES:

1. If this protocol follows a write and the DS1624 does not acknowledge here, restart the protocol at the Start here. If it does acknowledge, continue on.
2. Wait for write to complete (10 ms typ. 50 ms max). If DS1624 does not acknowledge the command protocol immediately following a configure register or write mem protocol, the DS1624 has not finished writing. Restart the new command protocol until the DS1624 acknowledges.
3. If n is greater than 8, the last eight bytes are the only bytes saved in memory. If the starting address is 00 and the incoming data is 00 11 22 33 44 55 66 77 88 99, the result will be mem00=88 mem01=99 mem02=22 mem03=33 mem04=44 mem05=55 mem06=66 mem07=77. The data wraps around and overwrites itself.
4. The STOP condition causes the DS1624 to initiate the write to EEPROM sequence. If a START condition comes instead of the STOP condition, the write is aborted. The data is not saved.
5. For reading, the address is incremented. If the starting address is 04h and 30 bytes of data are read out, 21h is the final address read.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	–55°C to +125°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD}	2.7	5.0	5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(–55°C to +125°C; V_{DD}=2.7V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Thermometer Error	T_{ERR}	0°C to 70°C –55°C to +0°C and +70°C to +125°C	See Typical Curve		±1/2	°C	11
Low Level Input Voltage	V_{IL}		–0.5		$0.3V_{DD}$	V	
High Level Input Voltage	V_{IH}		$0.7V_{DD}$		V_{DD}+0.5	V	
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	Fast Mode	0		50	ns	
Low Level Output Voltage	V_{OL1}	3 mA sink current	0		0.4	V	
	V_{OL2}	6 mA sink current	0		0.6	V	
Input Current each I/O Pin		$0.4<V_{I/O}<0.9V_{DD}$	–10		10	µA	2
I/O Capacitance	$C_{I/O}$				10	pF	
Active Supply Current	I_{CC}	Temperature Conversion			1000		
		E^2 Write			400	µA	3, 4
		Communication Only			100		
Standby Supply Current	I_{STBY}			1	3	µA	3, 4

AC ELECTRICAL CHARACTERISTICS

(–55°C to +125°C; V_{DD}=2.7V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Temperature Conversion Time	T_{TC}			200	500	ms	
NV Write Cycle Time	t_{WR}	0°C to 70°C		10	50	ms	10
SCL Clock Frequency	f_{SCL}	Fast Mode Standard Mode	0 0		400 100	KHz	
Bus Free Time Between a STOP and START Condition	t_{BUF}	Fast Mode Standard Mode	1.3 4.7			µs	
Hold Time (Repeated) START Condition	$t_{HD:STA}$	Fast Mode Standard Mode	0.6 4.0			µs	5
Low Period of SCL Clock	t_{LOW}	Fast Mode Standard Mode	1.3 4.7			µs	
High Period of SCL Clock	t_{HIGH}	Fast Mode Standard Mode	0.6 4.0			µs	
Setup Time for a Repeated START Condition	$t_{SU:STA}$	Fast Mode Standard Mode	0.6 4.7			µs	
Data Hold Time	$t_{HD:DAT}$	Fast Mode Standard Mode	0 0		0.9	µs	6, 7
Data Setup Time	$t_{SU:DAT}$	Fast Mode Standard Mode	100 250			ns	8
Rise Time of both SDA and SCL Signals	t_R	Fast Mode Standard Mode	$20+0.1C_B$		300 1000	ns	9
Fall Time of both SDA and SCL Signals	t_F	Fast Mode Standard Mode	$20+0.1C_B$		300 300	ns	9
Setup time for STOP Condition	$t_{SU:STO}$	Fast Mode Standard Mode	0.6 4.0			µs	
Capacitive Load for each Bus Line	C_b				400	pF	

All values referred to V_{IH}=0.9 V_{DD} and V_{IL}=0.1 V_{DD}.

AC ELECTRICAL CHARACTERISTICS

(–55°C to +125°C; V_{DD}=2.7V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_I		5		pF	

NOTES:

1. All voltages are referenced to ground.
2. I/O pins of fast mode devices must not obstruct the SDA and SCL lines if V_{DD} is switched off.
3. I_{CC} specified with SDA pin open.
4. I_{CC} specified with V_{CC} at 5.0V and SDA, SCL = 5.0V, 0°C to +70°C.

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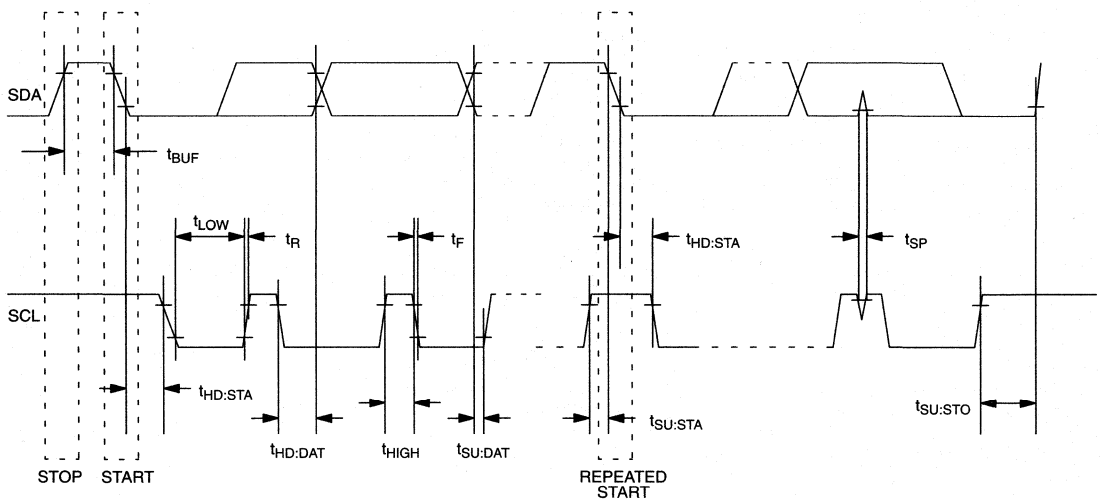
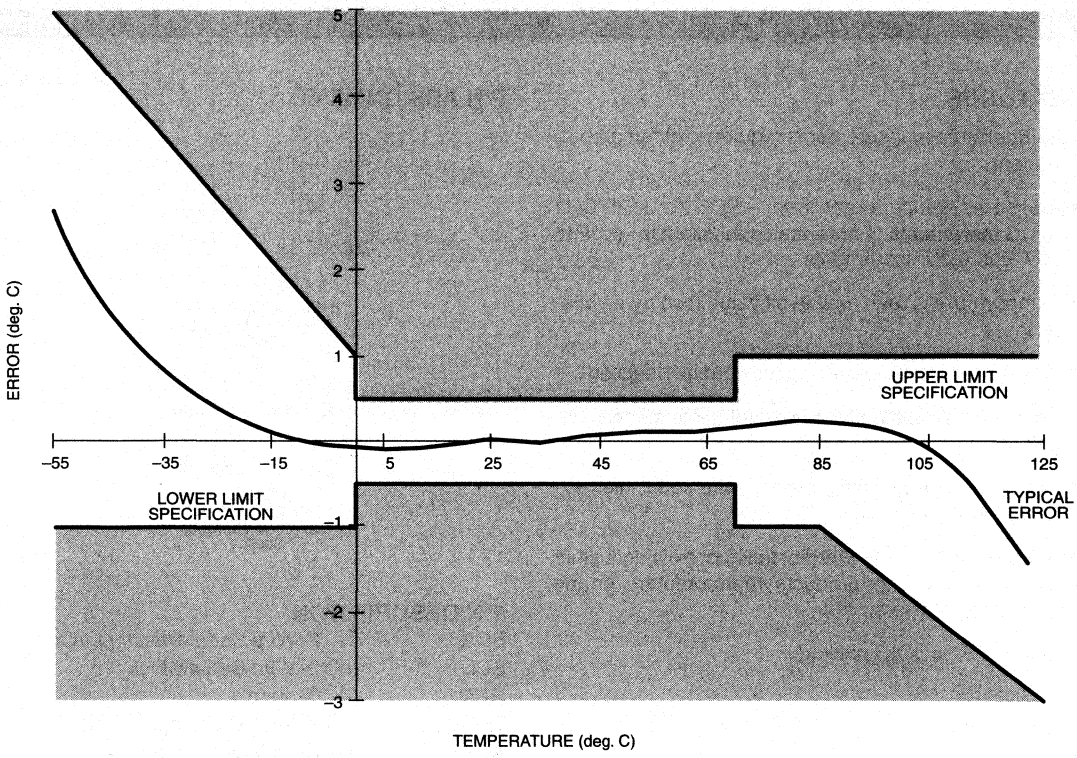
5. After this period, the first clock pulse is generated.
6. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH\ MIN}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
7. The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
8. A fast mode device can be used in a standard mode system, but the requirement $t_{SU:DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{R\ MAX}+t_{SU:DAT} = 1000+250 = 1250$ ns before the SCL line is released.
9. C_b – total capacitance of one bus line in pF.
10. Writing to the nonvolatile memory should only take place in the 0°C to +70°C temperature range.
11. See Typical Curve for specification limits outside the 0°C to 70°C temperature range.

TIMING DIAGRAMS



TYPICAL PERFORMANCE CURVE

DS1624 DIGITAL THERMOMETER AND THERMOSTAT
TEMPERATURE READING ERROR



10

ADVANCED INFORMATION

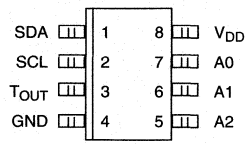
DALLAS SEMICONDUCTOR

DS1625
Digital Thermometer and Thermostat

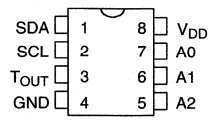
FEATURES

- Temperature measurements require no external components
- Measures temperatures from –55°C to +125°C in 0.5°C increments. Fahrenheit equivalent is –67°F to 257°F in 0.9°F increments
- Temperature is read as a 9–bit value (two byte transfer)
- Converts temperature to digital word in 1 second
- Thermostatic settings are user definable and nonvolatile
- Data is read from/written via a 2–wire serial interface (open drain I/O lines)
- Applications include thermostatic controls, industrial systems, consumer products, thermometers, or any thermal sensitive system.
- 8–pin DIP or SOIC package

PIN ASSIGNMENT



DS1625S
8–PIN SOIC (208 MIL)
See Mech. Drawings Section



DS1625
8–PIN DIP (300 MIL)
See Mech. Drawings Section

PIN DESCRIPTION

SDA	–	2–Wire Serial Data Input/Output
SCL	–	2–Wire Serial Clock
GND	–	Ground
T_{OUT}	–	Thermostat Output Signal
A0	–	Chip Address Input
A1	–	Chip Address Input
A2	–	Chip Address Input
V_{DD}	–	Power Supply Voltage (+5V)

DESCRIPTION

The DS1625 digital thermometer and thermostat provides 9 bit temperature readings which indicate the temperature of the device. The thermal alarm output, $T_{OUT,}$ is active when the temperature of the device exceeds a user–defined temperature TH. The output remains active until the temperature drops below user defined temperature TL, allowing for any hysteresis necessary.

User defined temperature settings are stored in non–volatile memory, so parts may be programmed prior to insertion in a system. Temperature settings, and temperature readings are all communicated to/from the DS1625 over a simple 2–wire serial interface.

DETAILED PIN DESCRIPTION Table 1

PIN	SYMBOL	DESCRIPTION
1	SDA	Data input/output pin for 2–wire serial communication port.
2	SCL	Clock input/output pin for 2–wire serial communication port.
3	T_{OUT}	Thermostat output. Active when temperature exceeds TH; will reset when temperature falls below TL.
4	GND	Ground pin.
5	A2	Address input pin.
6	A1	Address input pin.
7	A0	Address input pin.
8	V_{DD}	Supply voltage 5V input power pin.

OPERATION

Measuring Temperature

A block diagram of the DS1625 is shown in Figure 1. The DS1625 measures temperatures through the use of an on–board proprietary temperature measurement technique. A block diagram of the temperature measurement circuitry is shown in Figure 2.

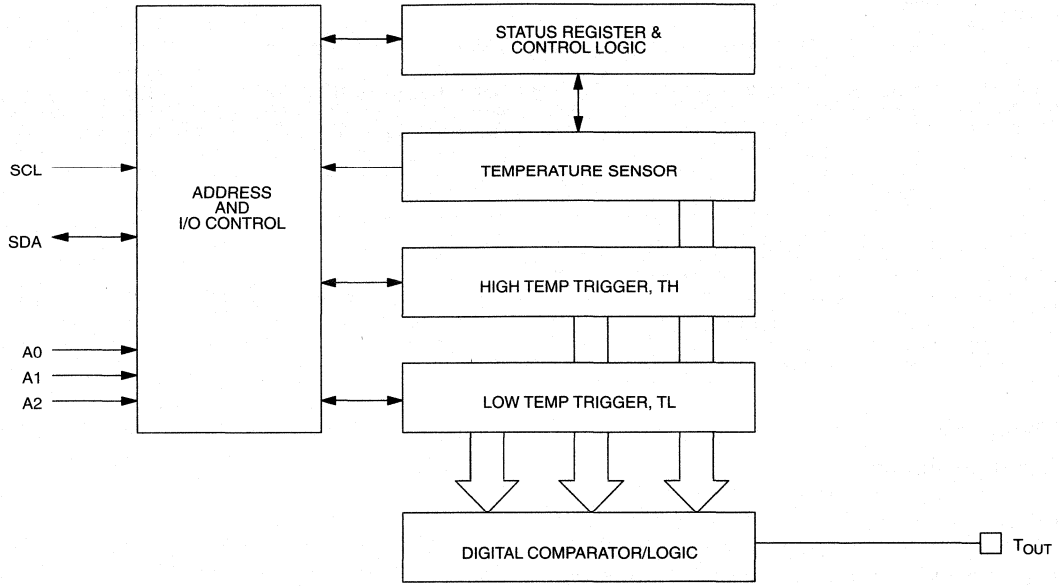
The DS1625 measures temperature by counting the number of clock cycles that an oscillator with a low temperature coefficient goes through during a gate period determined by a high temperature coefficient oscillator. The counter is preset with a base count that corresponds to –55°C. If the counter reaches zero before the gate period is over, the temperature register, which is also preset to the –55°C value, is incremented, indicating that the temperature is higher than –55°C.

At the same time, the counter is then preset with a value determined by the slope accumulator circuitry. This circuitry is needed to compensate for the parabolic behavior of the oscillators over temperature. The counter is then clocked again until it reaches zero. If the gate period is still not finished, then this process repeats.

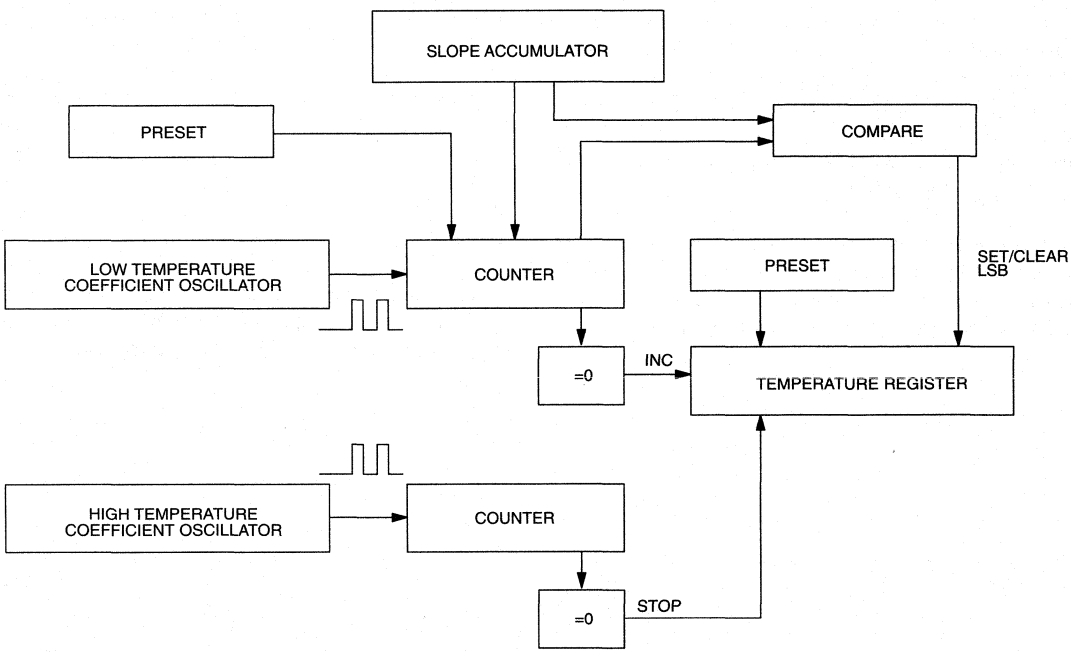
The slope accumulator is used to compensate for the nonlinear behavior of the oscillators over temperature, yielding a high resolution temperature measurement. This is done by changing the number of counts necessary for the counter to go through for each incremental degree in temperature. To obtain the desired resolution, therefore, both the value of the counter and the number of counts per degree C (the value of the slope accumulator) at a given temperature must be known.

This calculation is done inside the DS1625 to provide 0.5°C resolution. The temperature reading is provided in a 9–bit, two's complement reading by issuing the READ TEMPERATURE command. Table 2 describes the exact relationship of output data to measured temperature. The data is transmitted serially through the 2–wire serial interface, MSB first. The DS1625 can measure temperature over the range of –55°C to +125°C in 0.5°C increments. For Fahrenheit usage, a lookup table or conversion factor must be used.

DS1625 FUNCTIONAL BLOCK DIAGRAM Figure 1



TEMPERATURE MEASURING CIRCUITRY Figure 2



TEMPERATURE/DATA RELATIONSHIPS Table 2

TEMPERATURE	DIGITAL OUTPUT (Binary)	DIGITAL OUTPUT (Hex)
+125°C	01111101 00000000	7B00h
+25°C	00011001 00000000	1900h
$+^1/_2$°C	0000000010000000	0080h
+0°C	0000000000000000	007Fh
$-^1/_2$°C	11111111 10000000	FF80h
–25°C	11100111 00000000	E700h
–55°C	11001001 00000000	C900h

Since data is transmitted over the 2–wire bus MSB first, temperature data may be read from the DS1625 as either a single byte (with temperature resolution of 1°C), or as two bytes, the second byte containing the value of the least significant (0.5°C)bit of the temperature reading, as shown in Table 1. Note that the remaining 7 bits of this byte are set to all 0's.

Note that temperature is represented in the DS1625 in terms of a $^1/_2$°C LSB, yielding the following 9–bit format:

MSB								LSB							
1	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0

T = –25°C

Higher resolutions may be obtained by reading the temperature, and truncating the 0.5°C bit (the LSB) from the read value. This value is TEMP_READ. The value left in the counter may then be read by issuing a READ COUNTER command. This value is the count remaining (COUNT_REMAIN) after the gate period has ceased. By loading the value of the slope accumulator into the count register (using the READ SLOPE command), this value may then be read, yielding the number of counts per degree C (COUNT_PER_C) at that temperature. The actual temperature may be then be calculated by the user using the following:

$$\text{TEMPERATURE} = \text{TEMP\_READ} - 0.25 + \frac{(\text{COUNT\_PER\_C} - \text{COUNT\_REMAIN})}{\text{COUNT\_PER\_C}}$$

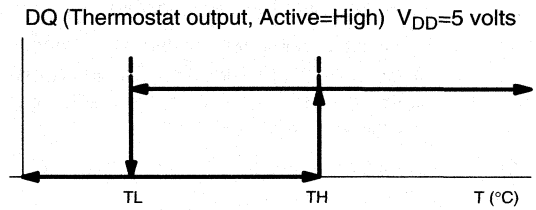
Thermostat Control

In its operating mode, the DS1625 functions as a thermostat with programmable hysteresis, as shown in Figure 3. The thermostat output updates as soon as a temperature conversion is complete.

When the DS1625's temperature meets or exceeds the value stored in the high temperature trip register (TH), the output becomes active, and will stay active until the temperature falls below the temperature stored in the low temperature trigger register (TL). In this way, any amount of hysteresis may be obtained.

The active state for the output is programmable by the user, so that an active state may either be a logic 1 (+5V) or a logic 0 (0V).

THERMOSTAT OUTPUT OPERATION Figure 3



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OPERATION AND CONTROL

The DS1625 must have temperature settings resident in the TH and TL registers for thermostatic operation. A configuration/status register is also used to determine the method of operation that the DS1625 will use in a particular application, as well as indicating the status of the temperature conversion operation.

The configuration register is defined as follows:

CONFIGURATION/STATUS REGISTER

DONE	THF	TLF	NVB	1	0	POL	1SHOT

where

DONE = Conversion Done bit. "1" = Conversion complete, "0" = conversion in progress.

THF = Temperature High Flag. This bit will be set to "1" when the temperature is greater than or equal to the value of TH. It will remain "1" until reset by writing 0 into this location or removing power from the device. This feature provides a method of determining if if the DS1625 has ever been subjected to temperatures above TH while power has been applied.

TLF = Temperature Low Flag. This bit will be set to "1" when the temperature is less than or equal to the value of TL. It will remain "1" until reset by writing 0 into this location or removing power from the device. This feature provides a method of determining if if the DS1625 has ever been subjected to temperatures below TL while power has been applied.

NVB = Nonvolatile memory busy flag. "1" = Write to an E^2 memory cell in progress, "0" = nonvolatile memory is not busy. A copy to E^2 may take up to 10 ms.

POL = Output Polarity Bit. "1" = active high, "0" = active low. This bit is nonvolatile.

1SHOT= One Shot Mode. If 1SHOT is "1", the DS1625 will perform one temperature conversion upon reception of the Start Convert T protocol. If 1SHOT is "0", the DS1625 will continuously perform temperature conversions. This bit is nonvolatile.

For typical thermostat operation, the DS1625 will operate in continuous mode. However, for applications where only one reading is needed at certain times, and to conserve power, the one–shot mode may be used. Note that the thermostat output (T_{OUT}) will remain in the state it was in after the last valid temperature conversion cycle when operating in one–shot mode.

2–WIRE SERIAL DATA BUS

The DS1625 supports a bi–directional two–wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a "master". The devices that are controlled by the master are "slaves". The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START an d STOP conditions. The DS1625 operates as a slave on the two–wire bus. Connections to the bus are made via the open–drain I/O lines SDA and SCL.

The following bus protocol has been defined (See Figure 3):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte–wise and each receiver acknowledges with a ninth bit.

Within the bus specifications a regular mode (100 KHz clock rate) and a fast mode (400 KHz clock rate) are defined. The DS1625 works in both modes.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

DATA TRANSFER ON 2–WIRE SERIAL BUS Figure 4

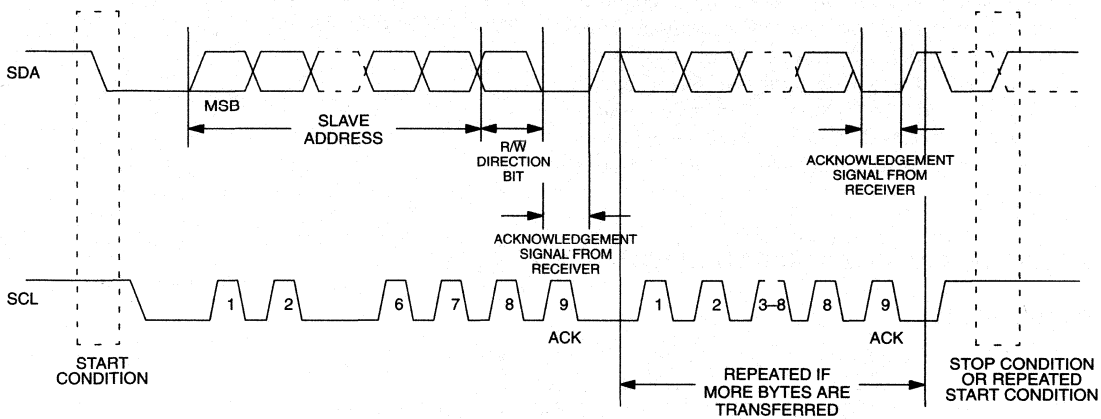

Figure 4 details how data transfer is accomplished on the two–wire bus. Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

1. **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.
2. **Data transfer from a slave transmitter to a master receiver.** The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the salve to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a 'not acknowledge' is returned.

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The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

The DS1625 may operate in the following two modes:

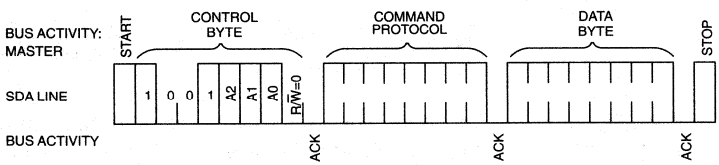
1. **Slave receiver mode:** Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.
2. **Slave transmitter mode:** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1625 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

SLAVE ADDRESS

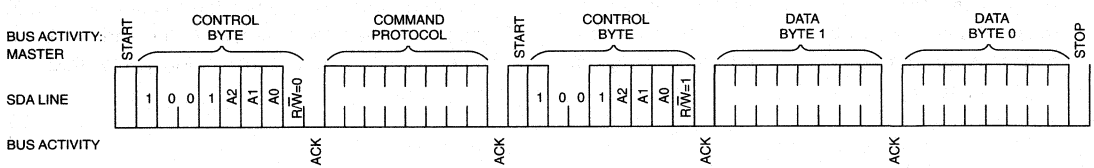
A control byte is the first byte received following the START condition from the master device. The control byte consists of a four bit control code; for the DS1625, this is set as 1001 binary for read and write operations. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used by the master device to select which of eight devices are to be accessed. These bits are in effect the three least significant bits of the slave address. The last bit of the control byte (R/$\overline{W}$) defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. Following the START condition, the DS1625 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving the 1001 code and appropriate device select bits, the slave device outputs an acknowledge signal on the SDA line.

2–WIRE SERIAL COMMUNICATION WITH DS1625 Figure 5

Write to DS1625



Read from DS1625



COMMAND SET

Data and control information is read from and written to the DS1625 in the format shown in Figure 4. To write to the DS1625, the master will issue the slave address of the DS1625, and the R/$\overline{W}$ bit will be set to 0. After receiving an acknowledge, the bus master provides a command protocol. After receiving this protocol, the DS1625 will issue an acknowledge, and then the master may send data to the DS1625. If the DS1625 is to be read, the master must send the command protocol as before, and then issue a repeated START condition and the control byte again, this time with the R/$\overline{W}$ bit set to 1 to allow reading of the data from the DS1625. The command set for the DS1625 as shown in Table 3 is as follows:

Read Temperature [AAh]

This command reads the last temperature conversion result. The DS1625 will send two bytes, in the format described earlier, which are the contents of this register.

Access TH [A1h]

If R/$\overline{W}$ is 0, this command writes to the TH (HIGH TEMPERATURE) register. After issuing this command, the next two bytes written to the DS1625, in the same format as described for reading temperature, will set the high temperature threshold for operation of the T_{OUT} output. If R/$\overline{W}$ is 1, the value stored in this register is read back.

Access TL [A2h]

If R/$\overline{W}$ is 0, this command writes to the TL (LOW TEMPERATURE) register. After issuing this command, the next two bytes written to the DS1625, in the same format as described for reading temperature, will set the high temperature threshold for operation of the TOUT output. If R/$\overline{W}$ is 1, the value stored in this register is read back.

Access Config [ACh]

If R/$\overline{W}$ is 0, this command writes to the configuration register. After issuing this command, the next data byte is the value to be written into the configuration register. If R/$\overline{W}$ is 1, the next data byte read is the value stored in the configuration register.

Start Convert T [EEh]

This command begins a temperature conversion. No further data is required. In one–shot mode, the temperature conversion will be performed and then the DS1625 will remain idle. In continuous mode, this command will initiate continuous conversions.

Stop Convert T [22h]

This command stops temperature conversion. No further data is required. This command may be used to halt a DS1625 in continuous conversion mode. After issuing this command, the current temperature measurement will be completed, and then the DS1625 will remain idle until a Start Convert T is issued to resume continuous operation.

DS1625 COMMAND SET Table 3

INSTRUCTION	DESCRIPTION	PROTOCOL	2–WIRE BUS DATA AFTER ISSUING PROTOCOL	NOTES
TEMPERATURE CONVERSION COMMANDS				
Read Temperature	Read last converted temperature value from temperature register.	AAh	<read 2 bytes data>	
Start Convert T	Initiates temperature conversion.	EEh	idle	1
Stop Convert T	Halts temperature conversion.	22h	idle	1
THERMOSTAT COMMANDS				
Access TH	Reads or writes high temperature limit value into TH register.	A1h	<write 2 bytes data>	2
Access TL	Reads or writes low temperature limit value into TL register.	A2h	<write 2 bytes data>	2
Access Config	Reads or writes configuration data to configuration register.	ACh	<write data>	2

NOTES:

1. In continuous conversion mode, a Stop Convert T command will halt continuous conversion. To restart, the Start Convert T command must be issued. In one–shot mode, a Start Convert T command must be issued for every temperature reading desired.
2. Writing to the E^2 typically requires 10ms at room temperature. After issuing a write command, no further writes should be requested for at least 10 ms.

MEMORY FUNCTION EXAMPLE

Example: Bus master sets up DS1625 for continuous conversion and thermostatic function.

BUS MASTER MODE	DS1625 MODE	DATA (MSB FIRST)	COMMENTS
TX	RX	START	Bus Master initiates a START condition.
TX	RX	<address,0>	Bus Master sends DS1625 address; R/$\overline{W}$ = 0.
RX	TX	ACK	DS1625 generates acknowledge bit.
TX	RX	ACh	Bus Master sends Access Config command protocol.
RX	TX	ACK	DS1625 generates acknowledge bit.
TX	RX	02h	Bus Master sets up DS1625 for output polarity active high, continuous conversion.
RX	TX	ACK	DS1625 generates acknowledge bit.
TX	RX	START	Bus Master generates a repeated START condition.
TX	RX	<address,0>	Bus Master sends DS1625 address; R/$\overline{W}$ = 0.
RX	TX	ACK	DS1625 generates acknowledge bit.
TX	RX	A1h	Bus Master sends Access TH command.
RX	TX	ACK	DS1625 generates acknowledge bit.
TX	RX	28h	Bus Master sends first byte of data for TH limit of +40°C.
RX	TX	ACK	DS1625 generates acknowledge bit.
TX	RX	00h	Bus Master sends second byte of data for TH limit of +40°C.
RX	TX	ACK	DS1625 generates acknowledge bit.
TX	RX	START	Bus Master generates a repeated START condition.
TX	RX	<address,0>	Bus Master sends DS1625 address; R/$\overline{W}$ = 0.
RX	TX	ACK	DS1625 generates acknowledge bit.
TX	RX	A2h	Bus Master sends Access TL command.
RX	TX	ACK	DS1625 generates acknowledge bit.
TX	RX	0Ah	Bus Master sends first byte of data for TL limit of +10°C.
RX	TX	ACK	DS1625 generates acknowledge bit.
TX	RX	00h	Bus Master sends second byte of data for TL limit of +10°C.
RX	TX	ACK	DS1625 generates acknowledge bit.
TX	RX	START	Bus Master generates a repeated START condition.
TX	RX	<address,0>	Bus Master sends DS1625 address; R/$\overline{W}$ = 0.
RX	TX	ACK	DS1625 generates acknowledge bit.
TX	RX	EEh	Bus Master sends Start Convert T command protocol.
RX	TX	ACK	DS1625 generates acknowledge bit.
TX	RX	STOP	Bus Master initiates STOP condition.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	–55°C to +125°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD}	4.5	5.0	5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(–55°C to +125°C; V_{DD}=4.5V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Thermometer Error	T_{ERR}	0°C to 70°C –40°C to +0°C and 70°C to 85°C –55°C to –40°C and 85°C to 125°C			±1/2 ±1 ±2	°C °C °C	
Low Level Input Voltage	V_{IL}		–0.5		1.5	V	
High Level Input Voltage	V_{IH}		3.0		V_{DD}+0.5	V	
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	Fast Mode	0		50	ns	
Low Level Output Voltage	V_{OL1}	3 mA sink current	0		0.4	V	
	V_{OL2}	6 mA sink current	0		0.6	V	
Input Current each I/O Pin		$0.4<V_{I/O}<0.9V_{DD}$	–10		10	µA	2
I/O Capacitance	$C_{I/O}$				10	pF	
Active Supply Current	I_{CC}	Temperature Conversion E^2 Write Communication Only			1000 400 100	µA	3, 4
Standby Supply Current	I_{STBY}				1	µA	3, 4

AC ELECTRICAL CHARACTERISTICS

(–55°C to +125°C; V_{DD}=4.5V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP.	MAX	UNITS	NOTES
Temperature Conversion Time	T_{TC}			1	2	s	
NV Write Cycle Time	t_{WR}	0°C to 70°C		10	50	ms	10
SCL Clock Frequency	f_{SCL}	Fast Mode Standard Mode	0 0		400 100	KHz	
Bus Free Time Between a STOP and START Condition	t_{BUF}	Fast Mode Standard Mode	1.3 4.7			µs	
Hold Time (Repeated) START Condition	$t_{HD:STA}$	Fast Mode Standard Mode	0.6 4.0			µs	5
Low Period of SCL Clock	t_{LOW}	Fast Mode Standard Mode	1.3 4.7			µs	
High Period of SCL Clock	t_{HIGH}	Fast Mode Standard Mode	0.6 4.0			µs	
Setup Time for a Repeated START Condition	$t_{SU:STA}$	Fast Mode Standard Mode	0.6 4.7			µs	
Data Hold Time	$t_{HD:DAT}$	Fast Mode Standard Mode	0 0		0.9	µs	6, 7
Data Setup Time	$t_{SU:DAT}$	Fast Mode Standard Mode	100 250			ns	8
Rise Time of both SDA and SCL Signals	t_R	Fast Mode Standard Mode	$20+0.1C_B$		300 1000	ns	9
Fall Time of both SDA and SCL Signals	t_F	Fast Mode Standard Mode	$20+0.1C_B$		300 300	ns	9
Setup time for STOP Condition	$t_{SU:STO}$	Fast Mode Standard Mode	0.6 4.0			µs	
Capacitive Load for each Bus Line	C_b				400	pF	

All values referred to the V_{IHMIN} and V_{ILMAX} levels.

AC ELECTRICAL CHARACTERISTICS

(–55°C to +125°C; V_{DD}=4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_I		5		pF	

NOTES:

1. All voltages are referenced to ground.
2. I/O pins of fast mode devices must not obstruct the SDA and SCL lines if V_{DD} is switched off.
3. I_{CC} specified with DQ pin open.
4. I_{CC} specified with V_{CC} at 5.0V and SDA,SCL = 5.0V, 0°C to 70°C.

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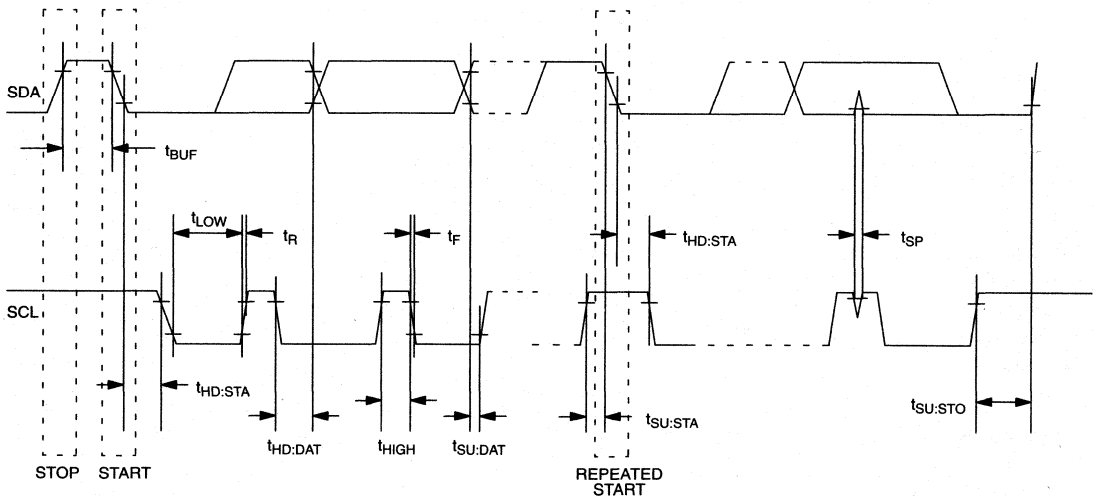
5. After this period, the first clock pulse is generated.
6. A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IH\ MIN}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
7. The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
8. A fast mode device can be used in a standard mode system, but the requirement $t_{SU:DAT}$ >250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{R\ MAX}+t_{SU:DAT}$ = 1000+250 = 1250 ns before the SCL line is released.
9. C_b – total capacitance of one bus line in pF.
10. Writing to the nonvolatile memory should only take place in the 0°C to +70°C temperature range.

TIMING DIAGRAM



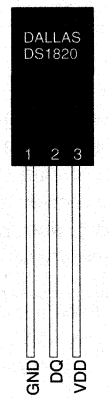
DALLAS SEMICONDUCTOR

DS1820
1–Wire™ Digital Thermometer

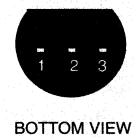
FEATURES

- Unique 1–Wire interface requires only one port pin for communication
- Multidrop capability simplifies distributed temperature sensing applications
- Requires no external components
- Can be powered from data line
- Zero standby power required
- Measures temperatures from –55°C to +125°C in 0.5°C increments. Fahrenheit equivalent is –67°F to 257°F in 0.9°F increments
- Temperature is read as a 9–bit digital value.
- Converts temperature to digital word in 200 ms (typ.)
- User–definable, nonvolatile temperature alarm settings
- Alarm search command identifies and addresses devices whose temperature is outside of programmed limits (temperature alarm condition)
- Applications include thermostatic controls, industrial systems, consumer products, thermometers, or any thermally sensitive system

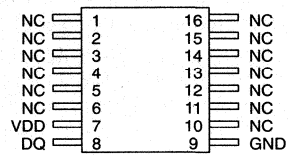
PIN ASSIGNMENT



DS1820
PR35 PACKAGE
See Mech. Drawings Section



BOTTOM VIEW



DS1820S
16-PIN SSOP
See Mech. Drawings Section

PIN DESCRIPTION

GND	–	Ground
DQ	–	Data In/Out
V_{DD}	–	Optional V_{DD}
NC	–	No Connect

DESCRIPTION

The DS1820 Digital Thermometer provides 9–bit temperature readings which indicate the temperature of the device.

Information is sent to/from the DS1820 over a 1–Wire interface, so that only one wire (and ground) needs to be connected from a central microprocessor to a DS1820. Power for reading, writing, and performing temperature conversions can be derived from the data line itself with no need for an external power source.

Because each DS1820 contains a unique silicon serial number, multiple DS1820s can exist on the same 1–Wire bus. This allows for placing temperature sensors in many different places. Applications where this feature is useful include HVAC environmental controls, sensing temperatures inside buildings, equipment or machinery, and in process monitoring and control.

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DETAILED PIN DESCRIPTION

PIN 16–PIN SSOP	PIN PR35	SYMBOL	DESCRIPTION
9	1	GND	**Ground.**
8	2	DQ	**Data Input/Output pin** for 1–Wire operation: Open drain. (See "Parasite Power" section.)
7	3	V_{DD}	**Optional V_{DD} pin**. See "Parasite Power" section for details of connection.

DS1820S (16–pin SSOP): All pins not specified in this table are not to be connected.

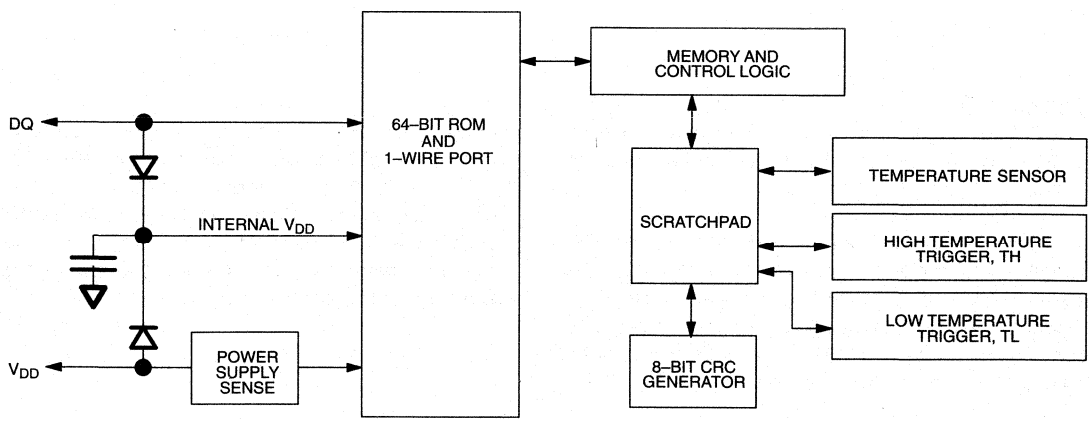
OVERVIEW

The block diagram of Figure 1 shows the major components of the DS1820. The DS1820 has three main data components: 1) 64–bit lasered ROM, 2) temperature sensor, and 3) nonvolatile temperature alarm triggers TH and TL. The device derives its power from the 1–Wire communication line by storing energy on an internal capacitor during periods of time when the signal line is high and continues to operate off this power source during the low times of the 1–Wire line until it returns high to replenish the parasite (capacitor) supply. As an alternative, the DS1820 may also be powered from an external 5V supply.

Communication to the DS1820 is via a 1–Wire port. With the 1–Wire port, the memory and control functions will not be available before the ROM function protocol has been established. The master must first provide one of five ROM function commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM, or 5) Alarm Search. These commands operate on the 64–bit lasered ROM portion of each device and can single out a specific device if many are present on the 1–Wire line as well as indicate to the bus master how many and what types of devices are present. After a ROM function sequence has been successfully executed, the memory and control functions are accessible and the master may then provide any one of the six memory and control function commands.

One control function command instructs the DS1820 to perform a temperature measurement. The result of this measurement will be placed in the DS1820's scratchpad memory, and may be read by issuing a memory function command which reads the contents of the scratchpad memory. The temperature alarm triggers TH and TL consist of one byte EEPROM each. If the alarm search command is not applied to the DS1820, these registers may be used as general purpose user memory. Writing TH and TL is done using a memory function command. Read access to these registers is through the scratchpad. All data is read and written least significant bit first.

DS1820 BLOCK DIAGRAM Figure 1



PARASITE POWER

The block diagram (Figure 1) shows the parasite powered circuitry. This circuitry "steals" power whenever the I/O or V_{DD} pins are high. I/O will provide sufficient power as long as the specified timing and voltage requirements are met (see the section titled "1–Wire Bus System"). The advantages of parasite power are two–fold: 1) by parasiting off this pin, no local power source is needed for remote sensing of temperature, and 2) the ROM may be read in absence of normal power.

In order for the DS1820 to be able to perform accurate temperature conversions, sufficient power must be provided over the I/O line when a temperature conversion is taking place. Since the operating current of the DS1820 is up to 1 mA, the I/O line will not have sufficient drive due to the 5K pullup resistor. This problem is particularly acute if several DS1820's are on the same I/O and attempting to convert simultaneously.

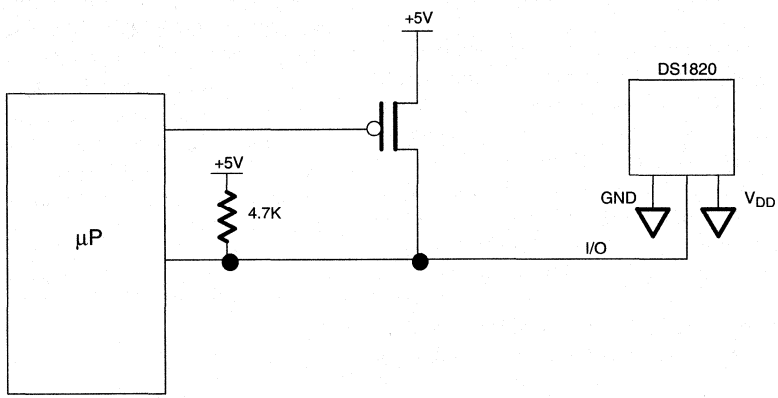
There are two ways to assure that the DS1820 has sufficient supply current during its active conversion cycle. The first is to provide a strong pullup on the I/O line whenever temperature conversions or copies to the E^2 memory are taking place. This may be accomplished by using a MOSFET to pull the I/O line directly to the power supply as shown in Figure 2. The I/O line must be switched over to the strong pullup within 10µs maximum after issuing any protocol that involves copying to the E^2 memory or initiates temperature conversions. When using the parasite power mode, the V_{DD} pin must be tied to ground.

Another method of supplying current to the DS1820 is through the use of an external power supply tied to the V_{DD} pin, as shown in Figure 3. The advantage to this is that the strong pullup is not required on the I/O line, and the bus master need not be tied up holding that line high during temperature conversions. This allows other data traffic on the 1–Wire bus during the conversion time. In addition, any number of DS1820's may be placed on the 1–Wire bus, and if they all use external power, they may all simultaneously perform temperature conversions by issuing the Skip ROM command and then issuing the Convert T command. Note that as long as the external power supply is active, the GND pin may not be floating.

The use of parasite power is not recommended above 100°C, since it may not be able to sustain communications given the higher leakage currents the DS1820 exhibits at these temperatures. For applications in which such temperatures are likely, it is strongly recommended that V_{DD} be applied to the DS1820.

For situations where the bus master does not know whether the DS1820's on the bus are parasite powered or supplied with external V_{DD}, a provision is made in the DS1820 to signal the power supply scheme used. The bus master can determine if any DS1820's are on the bus which require the strong pullup by sending a Skip ROM protocol, then issuing the read power supply command. After this command is issued, the master then issues read time slots. The DS1820 will send back "0" on the 1–Wire bus if it is parasite powered; it will send back a "1" if it is powered from the V_{DD} pin. If the master receives a "0", it knows that it must supply the strong pull–up on the I/O line during temperature conversions. See "Memory Command Functions" section for more detail on this command protocol.

STRONG PULL–UP FOR SUPPLYING DS1820 DURING TEMPERATURE CONVERSION Figure 2



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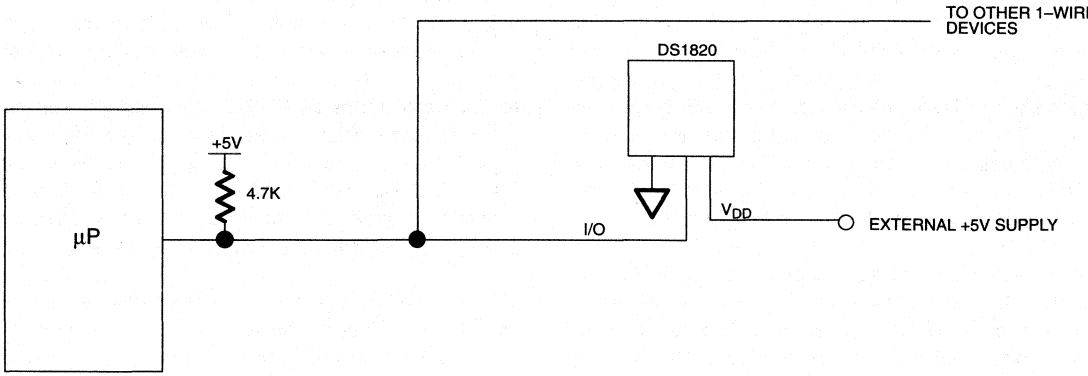
USING V_{DD} TO SUPPLY TEMPERATURE CONVERSION CURRENT Figure 3



OPERATION – MEASURING TEMPERATURE

The DS1820 measures temperatures through the use of an on–board proprietary temperature measurement technique. A block diagram of the temperature measurement circuitry is shown in Figure 4.

The DS1820 measures temperature by counting the number of clock cycles that an oscillator with a low temperature coefficient goes through during a gate period determined by a high temperature coefficient oscillator. The counter is preset with a base count that corresponds to –55°C. If the counter reaches zero before the gate period is over, the temperature register, which is also preset to the –55°C value, is incremented, indicating that the temperature is higher than –55°C.

At the same time, the counter is then preset with a value determined by the slope accumulator circuitry. This circuitry is needed to compensate for the parabolic behavior of the oscillators over temperature. The counter is then clocked again until it reaches zero. If the gate period is still not finished, then this process repeats.

The slope accumulator is used to compensate for the non–linear behavior of the oscillators over temperature, yielding a high resolution temperature measurement. This is done by changing the number of counts necessary for the counter to go through for each incremental degree in temperature. To obtain the desired resolution, therefore, both the value of the counter and the number of counts per degree C (the value of the slope accumulator) at a given temperature must be known.

Internally, this calculation is done inside the DS1820 to provide 0.5°C resolution. The temperature reading is provided in a 16–bit, sign–extended two's complement reading. Table 1 describes the exact relationship of output data to measured temperature. The data is transmitted serially over the 1–Wire interface. The DS1820 can measure temperature over the range of –55°C to +125°C in 0.5°C increments. For Fahrenheit usage, a lookup table or conversion factor must be used.

Note that temperature is represented in the DS1820 in terms of a $^1/_2$°C LSB, yielding the following 9–bit format:

MSB								LSB
1	1	1	0	0	1	1	1	0

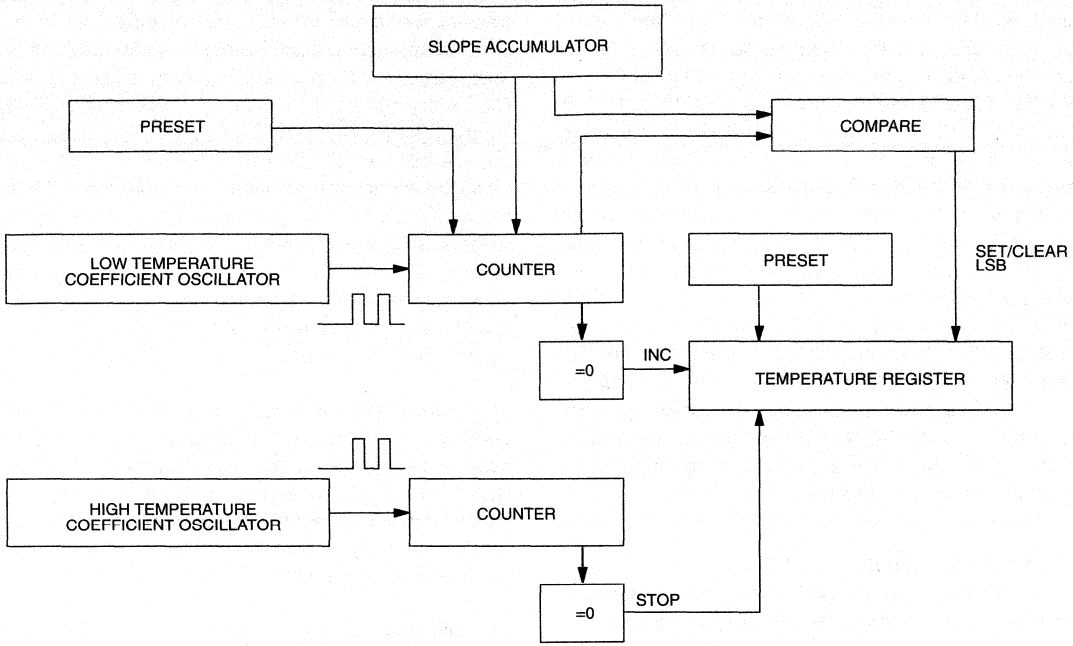
= –25°C

The most significant (sign) bit is duplicated into all of the bits in the upper MSB of the two–byte temperature register in memory. This "sign–extension" yields the 16–bit temperature readings as shown in Table 1.

Higher resolutions may be obtained by the following procedure. First, read the temperature, and truncate the 0.5°C bit (the LSB) from the read value. This value is TEMP_READ. The value left in the counter may then be read. This value is the count remaining (COUNT_REMAIN) after the gate period has ceased. The last value needed is the number of counts per degree C (COUNT_PER_C) at that temperature. The actual temperature may be then be calculated by the user using the following:

$$\text{TEMPERATURE} = \text{TEMP\_READ} - 0.25 + \frac{(\text{COUNT\_PER\_C} - \text{COUNT\_REMAIN})}{\text{COUNT\_PER\_C}}$$

TEMPERATURE MEASURING CIRCUITRY Figure 4



TEMPERATURE/DATA RELATIONSHIPS Table 1

TEMPERATURE	DIGITAL OUTPUT (Binary)	DIGITAL OUTPUT (Hex)
+125°C	00000000 11111010	00FA
+25°C	00000000 00110010	0032h
$+^1/_2$°C	00000000 00000001	0001h
+0°C	00000000 00000000	0000h
$-^1/_2$°C	11111111 11111111	FFFFh
–25°C	11111111 11001110	FFCEh
–55°C	11111111 10010010	FF92h

OPERATION – ALARM SIGNALLING

After the DS1820 has performed a temperature conversion, the temperature value is compared to the trigger values stored in TH and TL. Since these registers are 8 bit only, the 0.5°C bit is ignored for comparison. The most significant bit of TH or TL directly corresponds to the sign bit of the 16–bit temperature register. If the result of a temperature measurement is higher than TH or lower than TL, an alarm flag inside the device is set. This flag is updated with every temperature measurement. As long as the alarm flag is set, the DS1820 will respond to the alarm search command. This allows many DS1820s to be connected in parallel doing simultaneous temperature measurements. If somewhere the temperature exceeds the limits, the alarming device(s) can be identified and read immediately without having to read non–alarming devices.

64–BIT LASERED ROM

Each DS1820 contains a unique ROM code that is 64 bits long. The first eight bits are a 1–Wire family code (DS1820 code is 10h). The next 48 bits are a unique serial number. The last eight bits are a CRC of the first 56 bits. (See Figure 5.) The 64–bit ROM and ROM Function Control section allow the DS1820 to operate as a 1–Wire device and follow the 1–Wire protocol detailed in the section "1–Wire Bus System". The functions required to control sections of the DS1820 are not accessible until the ROM function protocol has been satisfied. This protocol is described in the ROM function protocol flowchart (Figure 6). The 1–Wire bus master must first provide one of five ROM function commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM, or 5) Alarm Search. After a ROM functions sequence has been successfully executed, the functions specific to the DS1820 are accessible and the bus master may then provide and one of the six memory and control function commands.

CRC GENERATION

The DS1820 has an 8–bit CRC stored in the most significant byte of the 64–bit ROM. The bus master can compute a CRC value from the first 56 bits of the 64–bit ROM and compare it to the value stored within the DS1820 to determine if the ROM data has been received error–free by the bus master. The equivalent polynomial function of this CRC is:

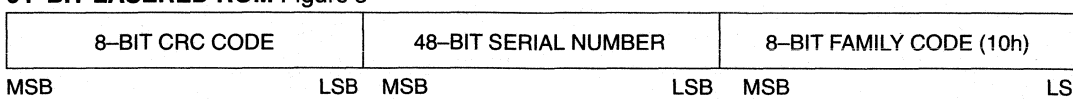
$$CRC = X^8 + X^5 + X^4 + 1$$

The DS1820 also generates an 8–bit CRC value using the same polynomial function shown above and provides this value to the bus master to validate the transfer of data bytes. In each case where a CRC is used for data transfer validation, the bus master must calculate a CRC value using the polynomial function given above and compare the calculated value to either the 8–bit CRC value stored in the 64–bit ROM portion of the DS1820 (for ROM reads) or the 8–bit CRC value computed within the DS1820 (which is read as a ninth byte when the scratchpad is read). The comparison of CRC values and decision to continue with an operation are determined entirely by the bus master. There is no circuitry inside the DS1820 that prevents a command sequence from proceeding if the CRC stored in or calculated by the DS1820 does not match the value generated by the bus master.

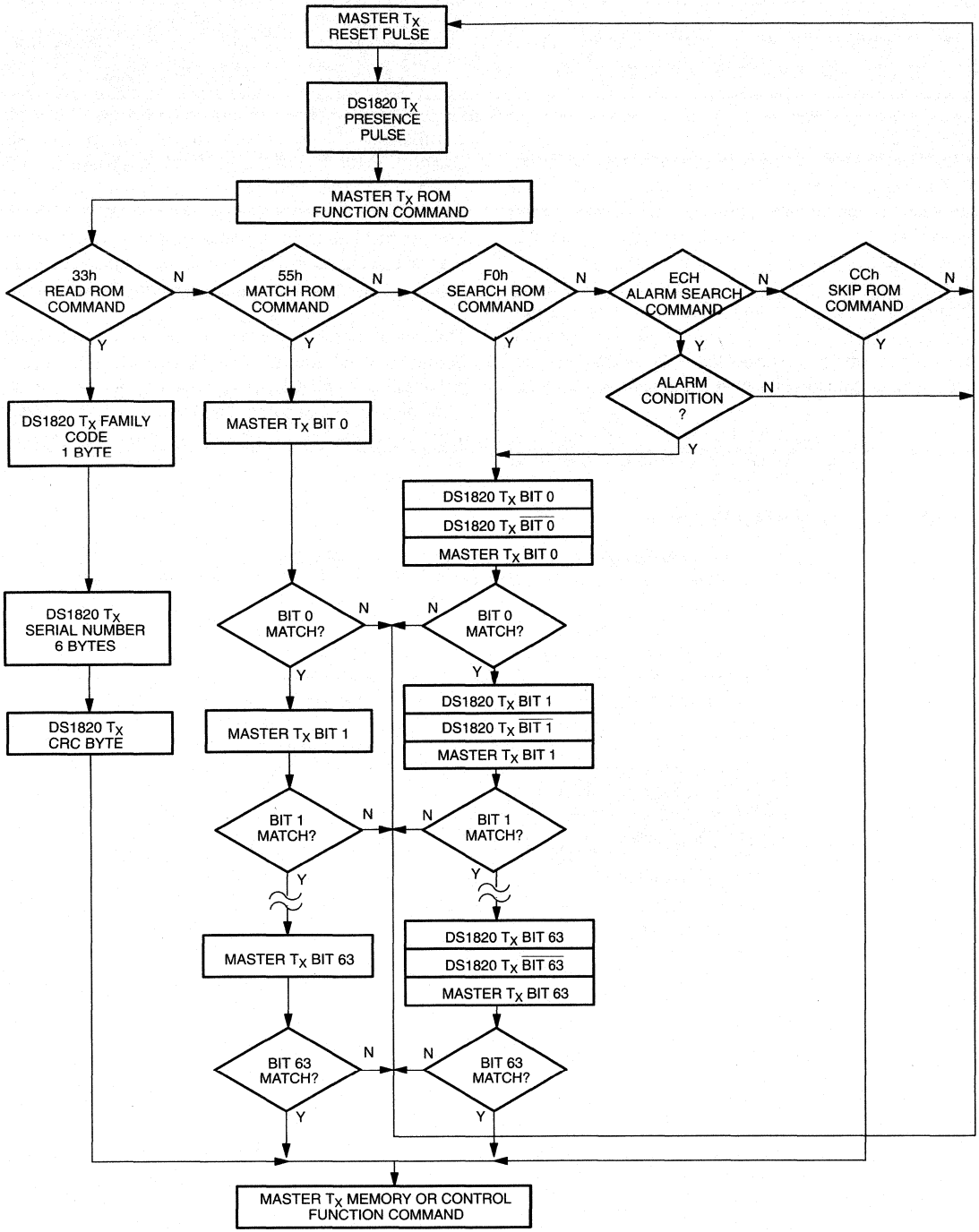
The 1–Wire CRC can be generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 7. Additional information about the Dallas 1–Wire Cyclic Redundancy Check is available in an application note entitled "Understanding and Using Cyclic Redundancy Checks with Dallas Semiconductor Touch Memory Products".

The shift register bits are initialized to zero. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the eight bits of CRC should return the shift register to all zeros.

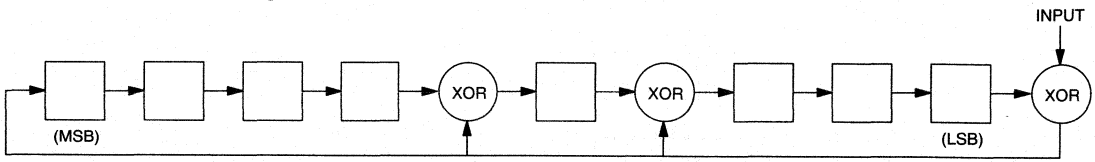
64–BIT LASERED ROM Figure 5



ROM FUNCTIONS FLOW CHART Figure 6



1–WIRE CRC CODE Figure 7



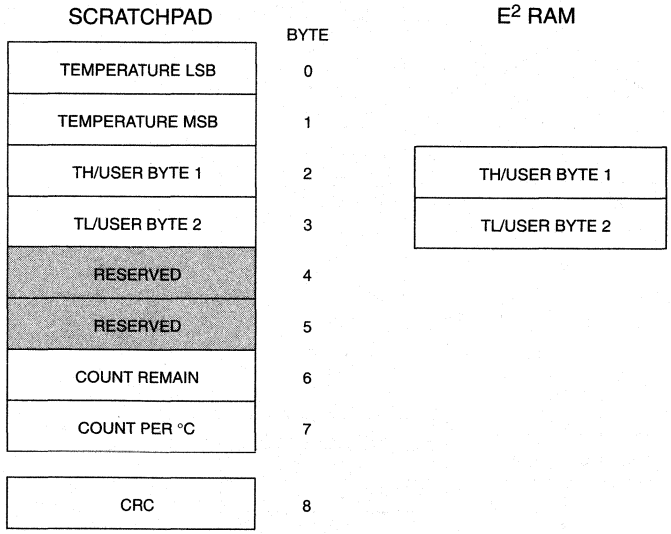
MEMORY

The DS1820's memory is organized as shown in Figure 8. The memory consists of a scratchpad RAM and a nonvolatile, electrically erasable (E^2) RAM, which stores the high and low temperature triggers TH and TL. The scratchpad helps insure data integrity when communicating over the 1–Wire bus. Data is first written to the scratchpad where it can be read back. After the data has been verified, a copy scratchpad command will transfer the data to the nonvolatile (E^2) RAM. This process insures data integrity when modifying the memory.

The scratchpad is organized as eight bytes of memory. The first two bytes contain the measured temperature information. The third and fourth bytes are volatile copies of TH and TL and are refreshed with every power–on reset. The next two bytes are not used; upon reading back, however, they will appear as all logic 1's. The seventh and eighth bytes are count registers, which may be used in obtaining higher temperature resolution (see "Operation–measuring Temperature" section).

There is a ninth byte which may be read with a Read Scratchpad command. This byte contains a cyclic redundancy check (CRC) byte which is the CRC over all of the eight previous bytes. This CRC is implemented in the fashion described in the section titled "CRC Generation".

DS1820 MEMORY MAP Figure 8



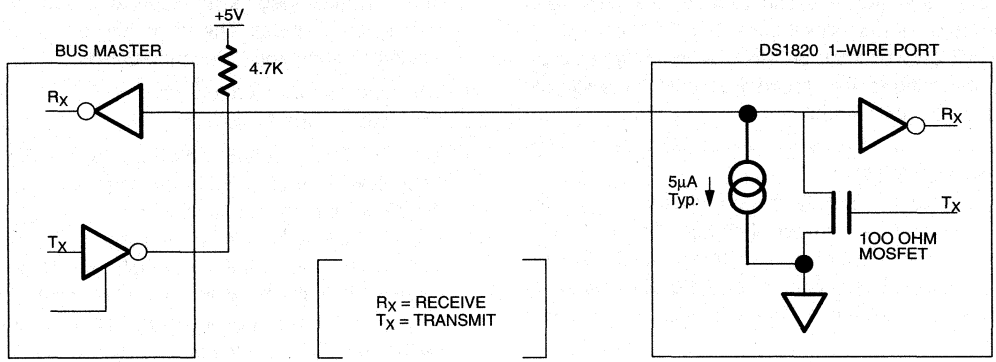
1–WIRE BUS SYSTEM

The 1–Wire bus is a system which has a single bus master and one or more slaves. The DS1820 behaves as a slave. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1–Wire signaling (signal types and timing).

HARDWARE CONFIGURATION

The 1–Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1–Wire bus must have open drain or 3–state outputs. The 1–Wire port of the DS1820 (I/O pin) is open drain with an internal circuit equivalent to that shown in Figure 9. A multidrop bus consists of a 1–Wire bus with multiple slaves attached. The 1–Wire bus requires a pullup resistor of approximately 5KΩ.

HARDWARE CONFIGURATION Figure 9



The idle state for the 1–Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 480 µs, all components on the bus will be reset.

TRANSACTION SEQUENCE

The protocol for accessing the DS1820 via the 1–Wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1–Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the DS1820 is on the bus and is ready to operate. For more details, see the "1–Wire Signaling" section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the five ROM function commands. All ROM function commands are eight bits long. A list of these commands follows (refer to flowchart in Figure 6):

Read ROM [33h]

This command allows the bus master to read the DS1820's 8–bit family code, unique 48–bit serial number, and 8–bit CRC. This command can only be used if there is a single DS1820 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired AND result).

10

Match ROM [55h]

The match ROM command, followed by a 64–bit ROM sequence, allows the bus master to address a specific DS1820 on a multidrop bus. Only the DS1820 that exactly matches the 64–bit ROM sequence will respond to the following memory function command. All slaves that do not match the 64–bit ROM sequence will wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

Skip ROM [CCh]

This command can save time in a single drop bus system by allowing the bus master to access the memory functions without providing the 64–bit ROM code. If more than one slave is present on the bus and a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pulldowns will produce a wired AND result).

Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1–Wire bus or their 64–bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64–bit ROM codes of all slave devices on the bus.

Alarm Search [ECh]

The flowchart of this command is identical to the Search ROM command. However, the DS1820 will respond to this command only if an alarm condition has been encountered at the last temperature measurement. An alarm condition is defined as a temperature higher than TH or lower than TL. The alarm condition remains set as long as the DS1820 is powered up, or until another temperature measurement reveals a non–alarming value. For alarming, the trigger values stored in EEPROM are taken into account. If an alarm condition exists and the TH or TL settings are changed, another temperature conversion should be done to validate any alarm conditions.

Example of a ROM Search

The ROM search process is the repetition of a simple 3–step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, 3–step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes.

The following example of the ROM search process assumes four different devices are connected to the same 1–Wire bus. The ROM data of the four devices is as shown:

ROM1	00110101...
ROM2	10101010...
ROM3	11110101...
ROM4	00010001...

The search process is as follows:

1. The bus master begins the initialization sequence by issuing a reset pulse. The slave devices respond by issuing simultaneous presence pulses.
2. The bus master will then issue the Search ROM command on the 1–Wire bus.
3. The bus master reads a bit from the 1–Wire bus. Each device will respond by placing the value of the first bit of their respective ROM data onto the 1–Wire bus. ROM1 and ROM4 will place a 0 onto the 1–Wire bus, i.e., pull it low. ROM2 and ROM3 will place a 1 onto the 1–Wire bus by allowing the line to stay high. The result is the logical AND of all devices on the line, therefore the bus master sees a 0. The bus master reads another bit. Since the Search ROM data command is being executed, all of the devices on the 1–Wire bus respond to this second read by placing the complement of the first bit of their respective ROM data onto the 1–Wire bus. ROM1 and ROM4 will place a 1 onto the 1–Wire, allowing the line to stay high. ROM2 and ROM3 will place a 0 onto the 1–Wire, thus it will be pulled low. The bus master again observes a 0 for the complement of the first ROM data bit. The bus master has determined that there are some devices on the 1–Wire bus that have a 0 in the first position and others that have a 1.

   The data obtained from the two reads of the 3–step routine have the following interpretations:

   00 There are still devices attached which have conflicting bits in this position.

   01 All devices still coupled have a 0 bit in this bit position.

   10 All devices still coupled have a 1 bit in this bit position.

11 There are no devices attached to the 1–Wire bus.

4. The bus master writes a 0. This deselects ROM2 and ROM3 for the remainder of this search pass, leaving only ROM1 and ROM4 connected to the 1–Wire bus.
5. The bus master performs two more reads and receives a 0 bit followed by a 1 bit. This indicates that all devices still coupled to the bus have 0's as their second ROM data bit.
6. The bus master then writes a 0 to keep both ROM1 and ROM4 coupled.
7. The bus master executes two reads and receives two 0 bits. This indicates that both 1 bits and 0 bits exist as the third bit of the ROM data of the attached devices.
8. The bus master writes a 0 bit. This deselects ROM1 leaving ROM4 as the only device still connected.
9. The bus master reads the remainder of the ROM bits for ROM4 and continues to access the part if desired. This completes the first pass and uniquely identifies one part on the 1–Wire bus.
10. The bus master starts a new ROM search sequence by repeating steps 1 through 7.
11. The bus master writes a 1 bit. This decouples ROM4, leaving only ROM1 still coupled.
12. The bus master reads the remainder of the ROM bits for ROM1 and communicates to the underlying logic if desired. This completes the second ROM search pass, in which another of the ROMs was found.
13. The bus master starts a new ROM search by repeating steps 1 through 3.
14. The bus master writes a 1 bit. This deselects ROM1 and ROM4 for the remainder of this search pass, leaving only ROM2 and ROM3 coupled to the system.
15. The bus master executes two read time slots and receives two zeros.
16. The bus master writes a 0 bit. This decouples ROM3, and leaving only ROM2.
17. The bus master reads the remainder of the ROM bits for ROM2 and communicates to the underlying logic if desired. This completes the third ROM search pass, in which another of the ROMs was found.
18. The bus master starts a new ROM search by repeating steps 13 through 15.
19. The bus master writes a 1 bit. This decouples ROM2, leaving only ROM3.
20. The bus master reads the remainder of the ROM bits for ROM3 and communicates to the underlying logic if desired. This completes the fourth ROM search pass, in which another of the ROMs was found.

Note the following:

The bus master learns the unique ID number (ROM data pattern) of one 1–Wire device on each ROM Search operation. The time required to derive the part's unique ROM code is:

$$960\ \mu s + (8 + 3 \times 64)\ 61\ \mu s = 13.16\ ms$$

The bus master is therefore capable of identifying 75 different 1–Wire devices per second.

I/O SIGNALING

The DS1820 requires strict protocols to insure data integrity. The protocol consists of several types of signaling on one line: reset pulse, presence pulse, write 0, write 1, read 0, and read 1. All of these signals, with the exception of the presence pulse, are initiated by the bus master.

The initialization sequence required to begin any communication with the DS1820 is shown in Figure 11. A reset pulse followed by a presence pulse indicates the DS1820 is ready to send or receive data given the correct ROM command and memory function command.

The bus master transmits (TX) a reset pulse (a low signal for a minimum of 480 µs). The bus master then releases the line and goes into a receive mode (RX). The 1–Wire bus is pulled to a high state via the 5K pull–up resistor . After detecting the rising edge on the I/O pin, the DS1820 waits 15–60 µs and then transmits the presence pulse (a low signal for 60–240 µs).

MEMORY COMMAND FUNCTIONS

The following command protocols are summarized in Table 2, and by the flowchart of Figure 10.

Write Scratchpad [4Eh]

This command writes to the scratchpad of the DS1820, starting at address 2. The next two bytes written will be saved in scratchpad memory, at address locations 2 and 3. Writing may be terminated at any point by issuing a reset.

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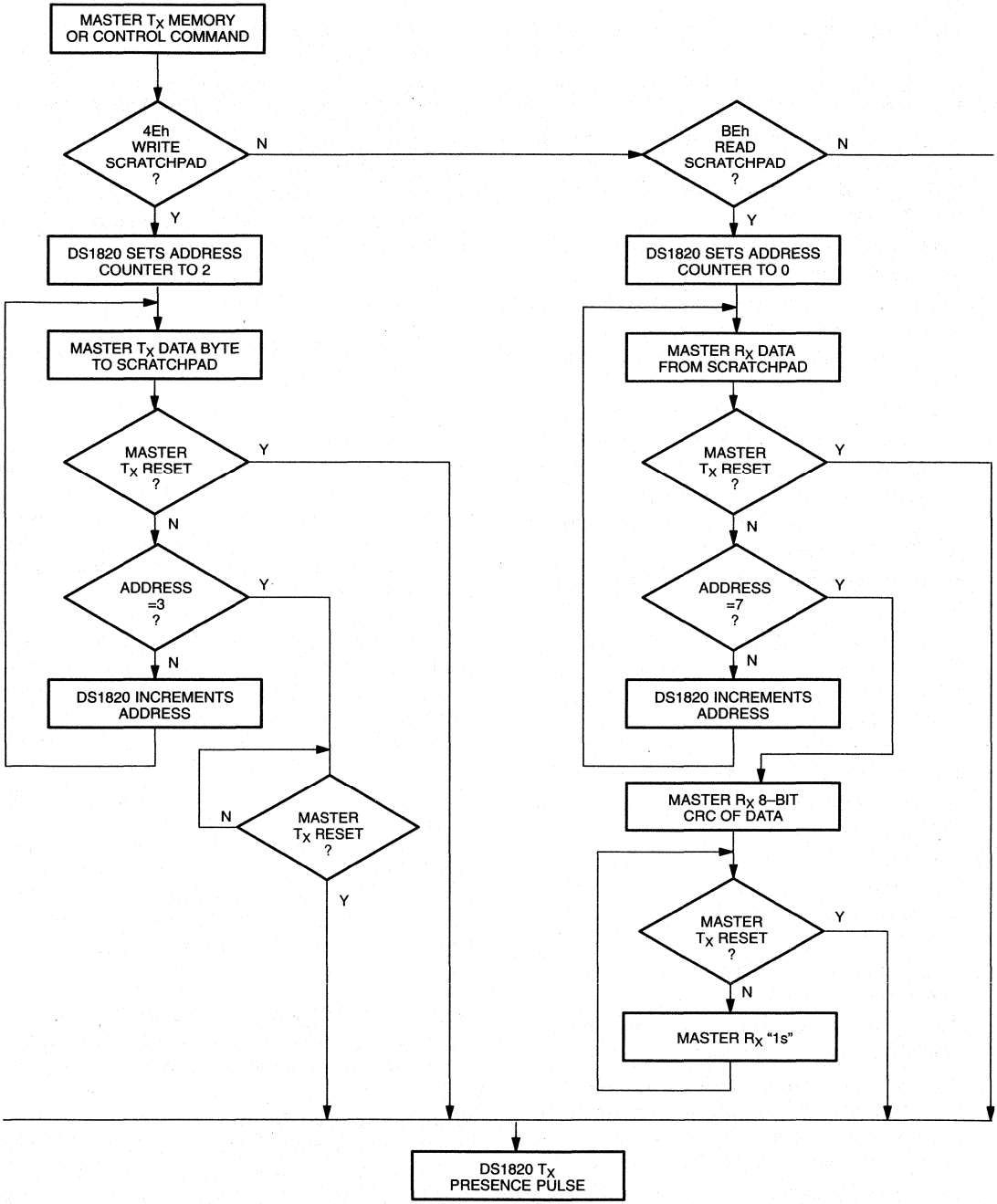
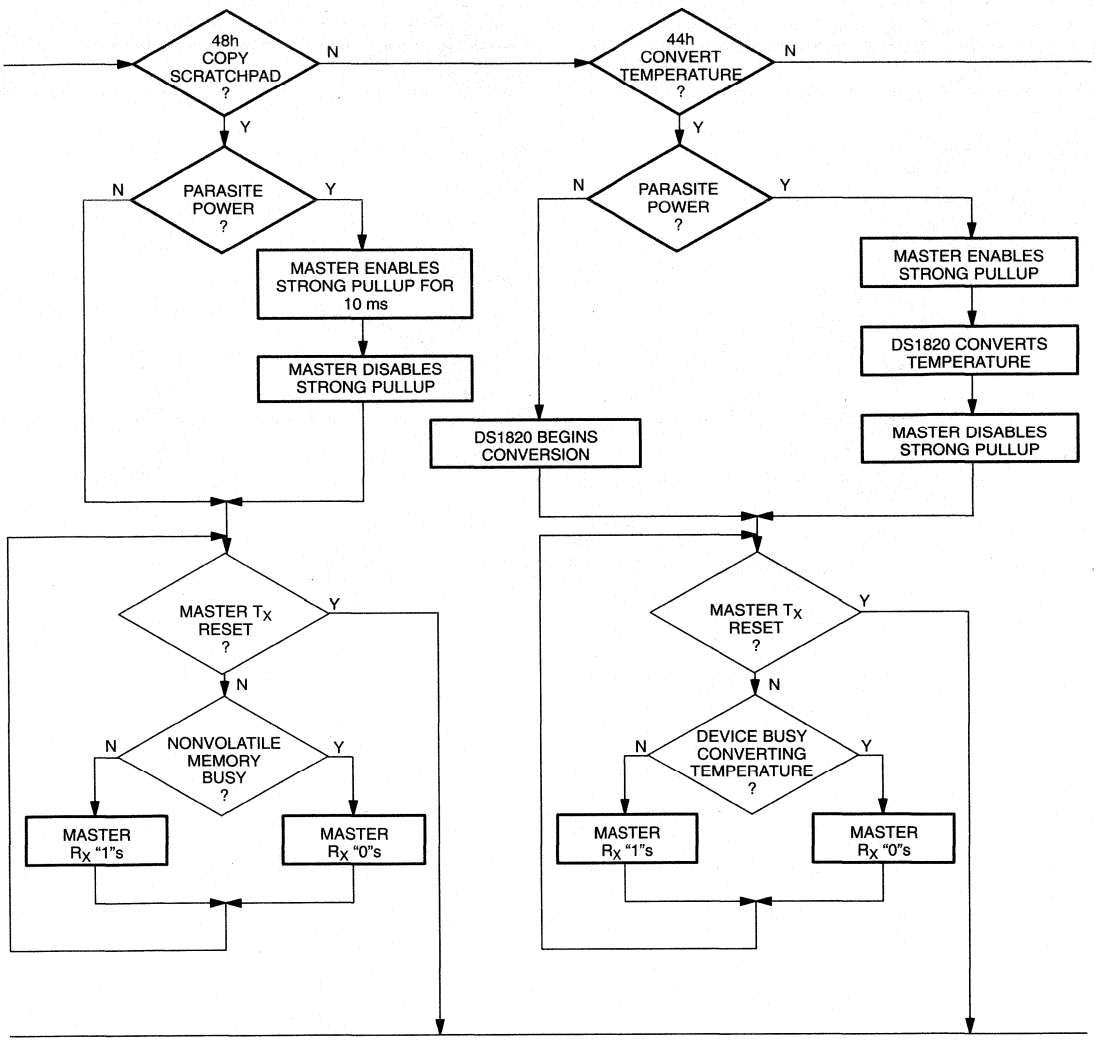
MEMORY FUNCTIONS FLOW CHART Figure 10



MEMORY FUNCTIONS FLOW CHART Figure 10 (cont'd)



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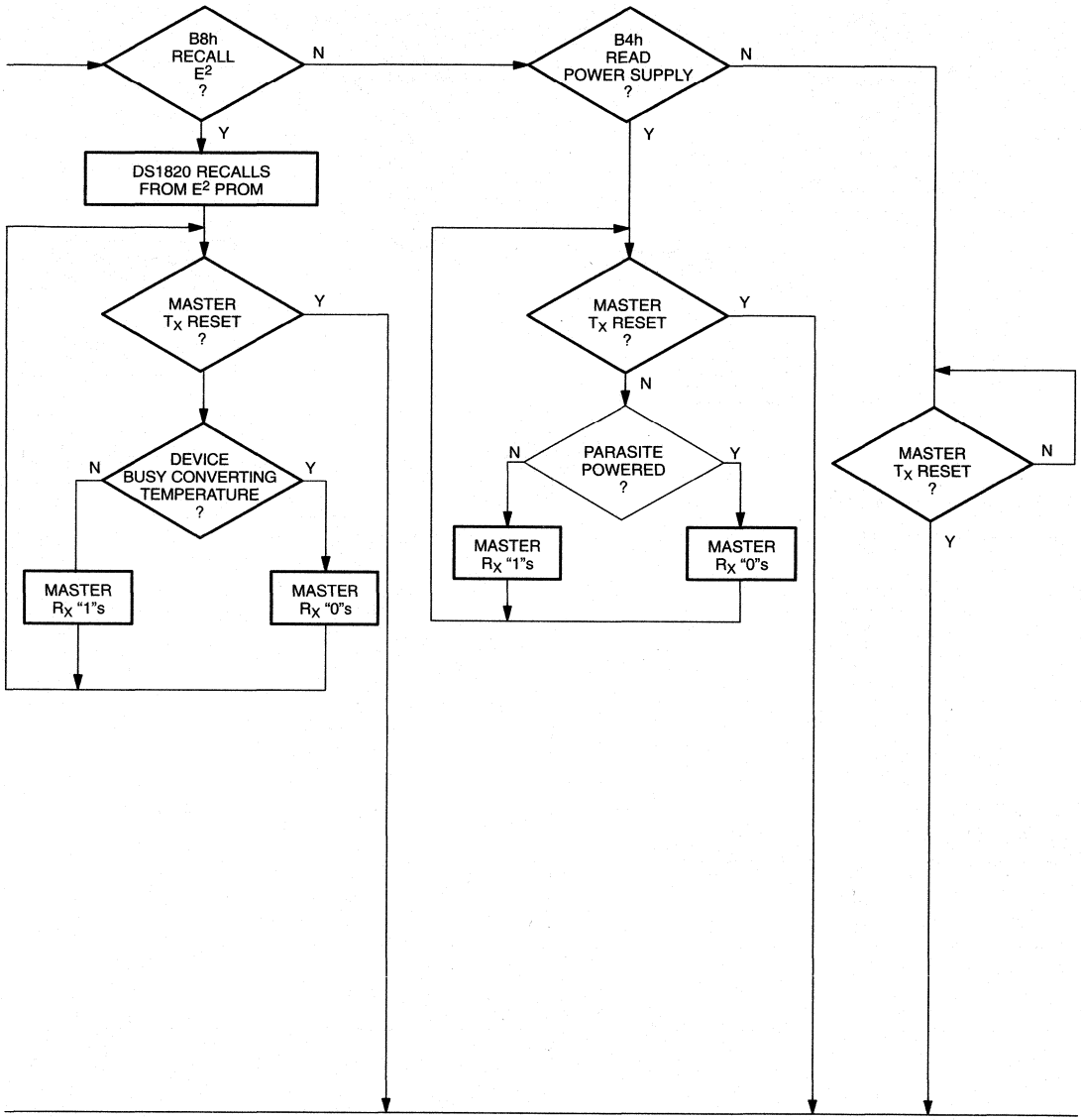
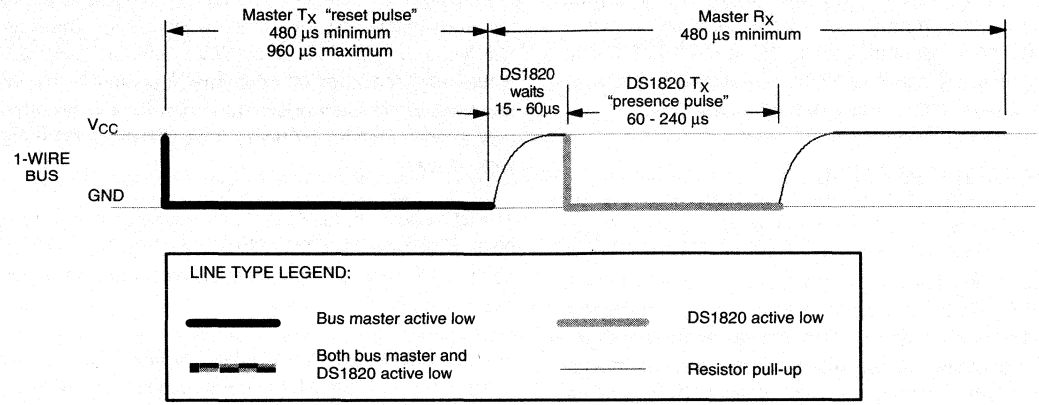
MEMORY FUNCTIONS FLOW CHART Figure 10 (cont'd)



INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 11



DS1820 COMMAND SET Table 2

INSTRUCTION	DESCRIPTION	PROTOCOL	1–WIRE BUS AFTER ISSUING PROTOCOL	NOTES
TEMPERATURE CONVERSION COMMANDS				
Convert T	Initiates temperature conversion.	44h	<read temperature busy status>	1
MEMORY COMMANDS				
Read Scratchpad	Reads bytes from scratchpad and reads CRC byte.	BEh	<read data up to 9 bytes>	
Write Scratchpad	Writes bytes into scratchpad at addresses 2 and 3 (TH and TL temperature triggers).	4Eh	<write data into 2 bytes at addr. 2 and addr. 3>	
Copy Scratchpad	Copies scratchpad into nonvolatile memory (addresses 2 and 3 only).	48h	<read copy status>	2
Recall E^2	Recalls values stored in nonvolatile memory into scratchpad (temperature triggers).	B8h	<read temperature busy status>	
Read Power Supply	Signals the mode of DS1820 power supply to the master.	B4h	<read supply status>	

NOTE:

1. Temperature conversion takes up to 500 ms. After receiving the Convert T protocol, if the part does not receive power from the V_{DD} pin, the I/O line for the DS1820 must be held high for at least 500 ms to provide power during the conversion process. As such, no other activity may take place on the 1–Wire bus for at least this period after a Convert T command has been issued.
2. After receiving the Copy Scratchpad protocol, if the part does not receive power from the V_{DD} pin, the I/O line for the DS1820 must be held high for at least 10 ms to provide power during the copy process. As such, no other activity may take place on the 1–Wire bus for at least this period after a Copy Scratchpad command has been issued.

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Read Scratchpad [BEh]
This command reads the contents of the scratchpad. Reading will commence at byte 0, and will continue through the scratchpad until the 9th (byte 8, CRC) byte is read. If not all locations are to be read, the master may issue a reset to terminate reading at any time.

Copy Scratchpad [48h]
This command copies the scratchpad into the E^2 memory of the DS1820, storing the temperature trigger bytes in nonvolatile memory. If the bus master issues read time slots following this command, the DS1820 will output "0" on the bus as long as it is busy copying the scratchpad to E^2; it will return a "1" when the copy process is complete. If parasite powered, the bus master has to enable a strong pullup for at least 10 ms immediately after issuing this command.

Convert T [44h]
This command begins a temperature conversion. No further data is required. The temperature conversion will be performed and then the DS1820 will remain idle. If the bus master issues read time slots following this command, the DS1820 will output "0" on the bus as long as it is busy making a temperature conversion; it will return a "1" when the temperature conversion is complete. If parasite powered, the bus master has to enable a strong pullup for 500 ms immediately after issuing this command.

Recall E2 [B8h]
This command recalls the temperature trigger values stored in E^2 to the scratchpad. This recall operation happens automatically upon power–up to the DS1820 as well, so valid data is available in the scratchpad as soon as the device has power applied. With every read data time slot issued after this command has been sent, the device will output its temperature converter busy flag "0"=busy, "1"=ready.

Read Power Supply [B4h]
With every read data time slot issued after this command has been sent to the DS1820, the device will signal its power mode: "0"=parasite power, "1"=external power supply provided.

READ/WRITE TIME SLOTS
DS1820 data is read and written through the use of time slots to manipulate bits and a command word to specify the transaction.

Write Time Slots
A write time slot is initiated when the host pulls the data line from a high logic level to a low logic level. There are two types of write time slots: Write One time slots and Write Zero time slots. All write time slots must be a minimum of 60 microseconds in duration with a minimum of a one microsecond recovery time between individual write cycles.

The DS1820 samples the I/O line in a window of 15 µs to 60 µs after the I/O line falls. If the line is high, a Write One occurs. If the line is low, a Write Zero occurs (see Figure 12).

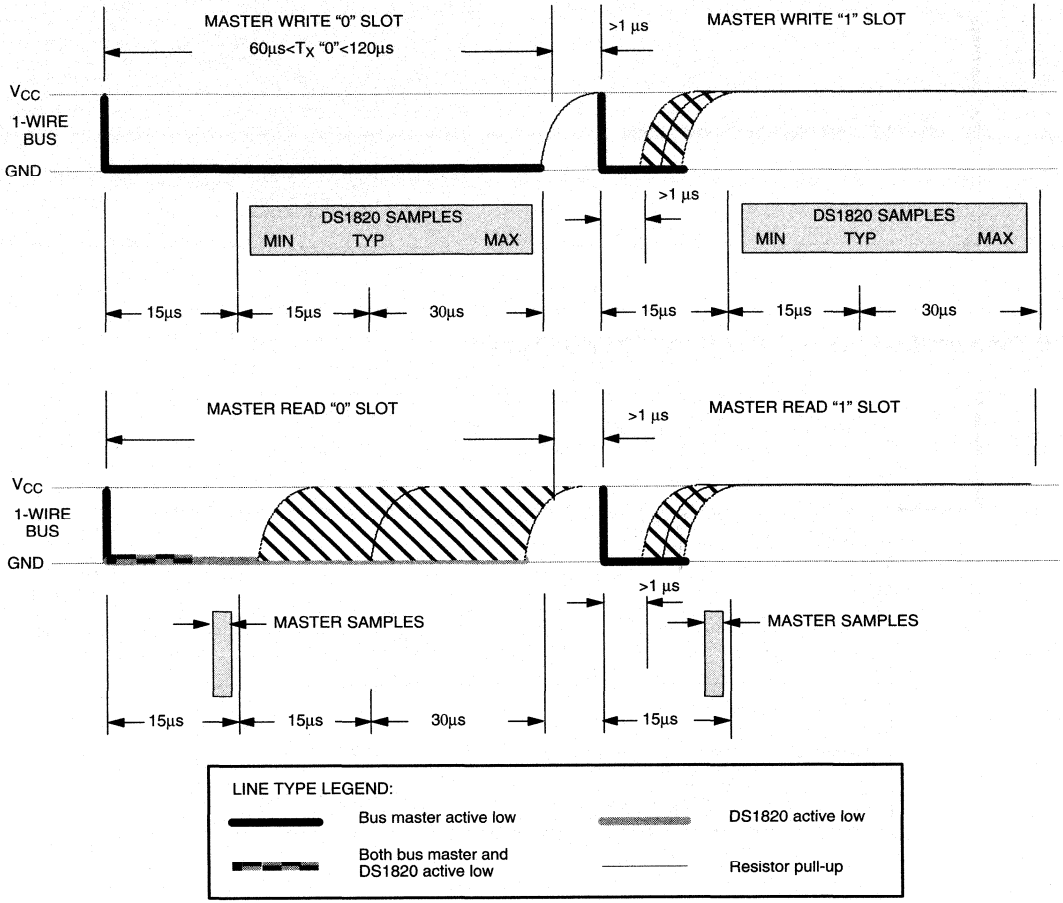
For the host to generate a Write One time slot, the data line must be pulled to a logic low level and then released, allowing the data line to pull up to a high level within 15 microseconds after the start of the write time slot.

For the host to generate a Write Zero time slot, the data line must be pulled to a logic low level and remain low for 60 µs.

Read Time Slots
The host generates read time slots when data is to be read from the DS1820. A read time slot is initiated when the host pulls the data line from a logic high level to logic low level. The data line must remain at a low logic level for a minimum of one microsecond; output data from the DS1820 is valid for 15 microseconds after the falling edge of the read time slot. The host therefore must stop driving the I/O pin low in order to read its state 15 microseconds from the start of the read slot (see Figure 12). By the end of the read time slot, the I/O pin will pull back high via the external pull–up resistor. All read time slots must be a minimum of 60 microseconds in duration with a minimum of a one microsecond recovery time between individual read slots.

Figure 13 shows that the sum of T_{INIT}, T_{RC}, and T_{SAMPLE} must be less than 15 µs. Figure 14 shows that system timing margin is maximized by keeping T_{INIT} and T_{RC} as small as possible and by locating the master sample time towards the end of the 15 µs period.

READ/WRITE TIMING DIAGRAM Figure 12



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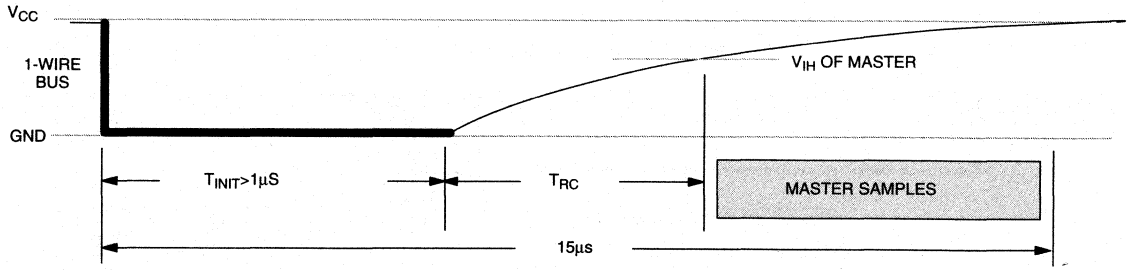
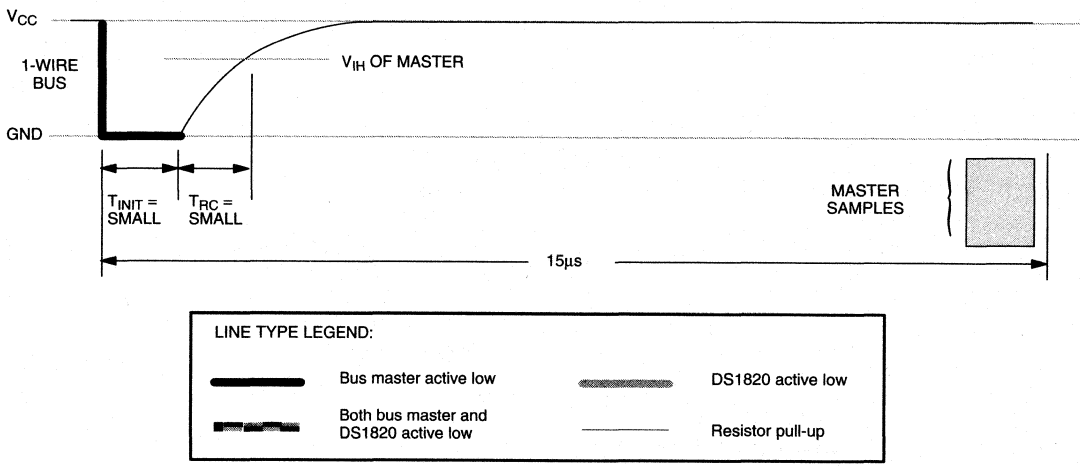
DETAILED MASTER READ "1" TIMING Figure 13



RECOMMENDED MASTER READ "1" TIMING Figure 14



MEMORY FUNCTION EXAMPLE Table 3
Example: Bus Master initiates temperature conversion, then reads temperature (parasite power assumed).

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480–960 µs)
RX	Presence	Presence pulse.
TX	55h	Issue "Match ROM" command.
TX	<64–bit ROM code>	Issue address for DS1820.
TX	44h	Issue "Convert T" command.
TX	<I/O LINE HIGH>	I/O line is held high for at least 500 ms by bus master to allow conversion to complete.
TX	Reset	Reset pulse.
RX	Presence	Presence pulse.
TX	55h	Issue "Match ROM" command.
TX	<64–bit ROM code>	Issue address for DS1820.
TX	BEh	Issue "Read Scratchpad" command.
RX	<9 data bytes>	Read entire scratchpad plus CRC; the master now recalculates the CRC of the eight data bytes received from the scratchpad, compares the CRC calculated and the CRC read. If they match, the master continues; if not, this read operation is repeated.
TX	Reset	Reset Pulse
RX	Presence	Presence pulse, done.

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MEMORY FUNCTION EXAMPLE Table 4

Example: Bus Master writes memory (parasite power and only one DS1820 assumed).

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse.
RX	Presence	Presence pulse.
TX	CCh	Skip ROM command.
TX	4Eh	Write Scratchpad command.
TX	<2 data bytes>	Writes two bytes to scratchpad (TH and TL).
TX	Reset	Reset pulse.
RX	Presence	Presence pulse.
TX	CCh	Skip ROM command.
TX	BEh	Read Scratchpad command.
RX	<9 data bytes>	Read entire scratchpad plus CRC. The master now recalculates the CRC of the eight data bytes received from the scratchpad, compares the CRC and the two other bytes read back from the scratchpad. If data match, the master continues; if not, repeat the sequence.
TX	Reset	Reset pulse.
RX	Presence	Presence pulse.
TX	CCh	Skip ROM command.
TX	48h	Copy Scratchpad command; after issuing this command, the master must wait 6 ms for copy operation to complete.
TX	Reset	Reset pulse.
RX	Presence	Presence pulse, done.

MEMORY FUNCTION EXAMPLE Table 5
Example: Temperature conversion and interpolation (external power supply and only one DS1820 assumed).

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	CCh	Skip ROM command.
TX	44h	Convert T command.
RX	<1 data byte>	Read busy flag eight times. The master continues reading one byte (or bit) after another until the data is FFh (all bits 1).
TX	Reset	Reset pulse.
RX	Presence	Presence pulse.
TX	CCh	Skip ROM command.
TX	BEh	Read Scratchpad command.
RX	<9 data bytes>	Read entire scratchpad plus CRC. The master now recalculates the CRC of the eight data bytes received from the scratchpad and compares both CRCs. If the CRCs match, the data is valid. The master saves the temperature value and stores the contents of the count register and count per °C register as COUNT_REMAIN and COUNT_PER_C, respectively
TX	Reset	Reset pulse.
RX	Presence	Presence pulse, done
–	–	CPU calculates temperature as described in the data sheet for higher resolution.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	–55°C to +125°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD}	I/O Functions	2.8	5.0	5.5	V	1, 2
		$\pm 1/2$°C Accurate Temperature Conversions	4.3		5.5		
Data Pin	I/O		–0.5		5.5	V	2
Logic 1	V_{IH}		2.0		V_{CC}+0.3	V	2, 3
Logic 0	V_{IL}		–0.3		+0.8	V	2, 4

DC ELECTRICAL CHARACTERISTICS

(–55°C to +125°C; V_{DD}=3.6V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Thermometer Error	t_{ERR}	0°C to +70°C			$\pm 1/2$	°C	
		–55°C to 0°C and +70°C to +125°C		See Typical Curve			9
Input Logic High	V_{IH}		2.2		5.5	V	2, 3
Input Logic Low	V_{IL}		–0.3		+0.8	V	2, 4
Sink Current	I_L	$V_{I/O}$=0.4V	–4.0			mA	2
Standby Current	I_Q			200	250	nA	8
Active Current	I_{DD}			1	1.5	mA	5, 6
Input Load Current	I_L			5		µA	7

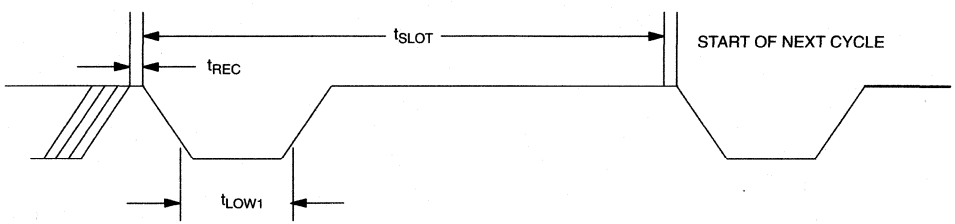
AC ELECTRICAL CHARACTERISTICS: 1–WIRE INTERFACE (–55°C to +125°C; V_{DD}=3.6V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Temperature Conversion Time	t_{CONV}		200	500	ms	
Time Slot	t_{SLOT}	60		120	µs	
Recovery Time	t_{REC}	1			µs	
Write 0 Low Time	r_{LOW0}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Read Data Valid	t_{RDV}			15	µs	
Reset Time High	t_{RSTH}	480			µs	
Reset Time Low	t_{RSTL}	480		4800	µs	
Presence Detect High	t_{PDHIGH}	15		60	µs	
Presence Detect Low	t_{PDLOW}	60		240	µs	
Capacitance	$C_{IN/OUT}$			25	pF	

NOTES:

1. Temperature conversion will work with ±2°C accuracy down to V_{DD} = 3.4V.
2. All voltages are referenced to ground.
3. Logic one voltages are specified at a source current of 1 mA.
4. Logic zero voltages are specified at a sink current of 4 mA.
5. I_{DD} specified with V_{CC} at 5.0V
6. Active current refers to either temperature conversion or writing to the E^2 memory. Writing to E^2 memory consumes approximately 200 µA for up to 10 ms.
7. Input load is to ground.
8. Standby current specified up to 70°C. Standby current typically is 5 µA at 125°C.
9. See Typical Curve for specification limits outside the 0°C to 70°C range.

1–WIRE WRITE ONE TIME SLOT



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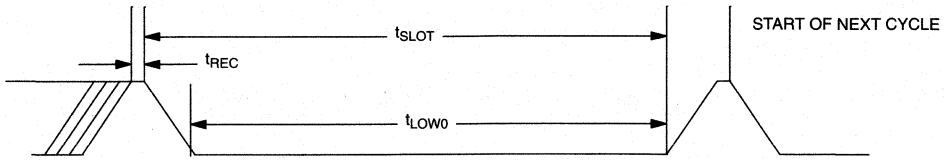
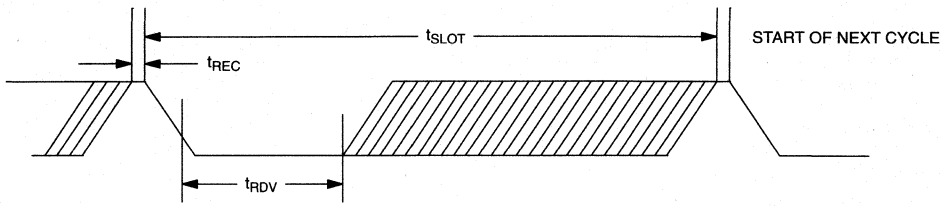
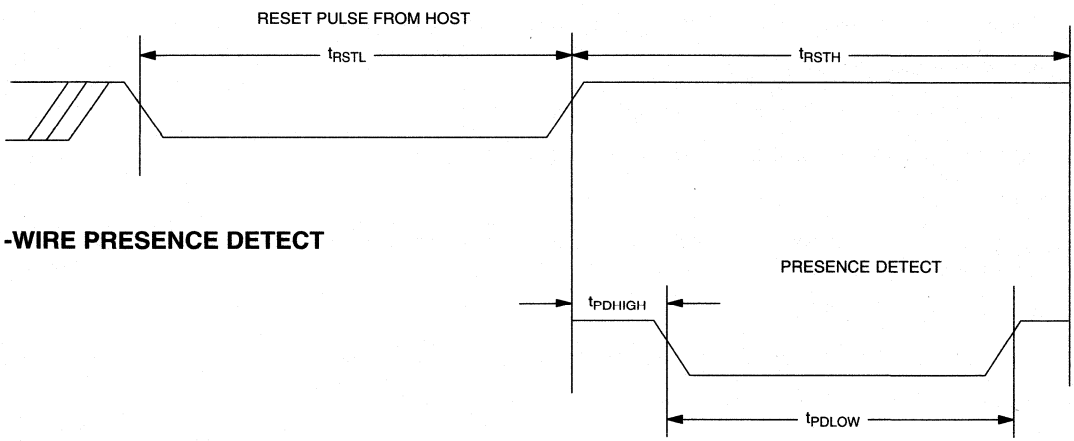
1–WIRE WRITE ZERO TIME SLOT



1-WIRE READ ZERO TIME SLOT



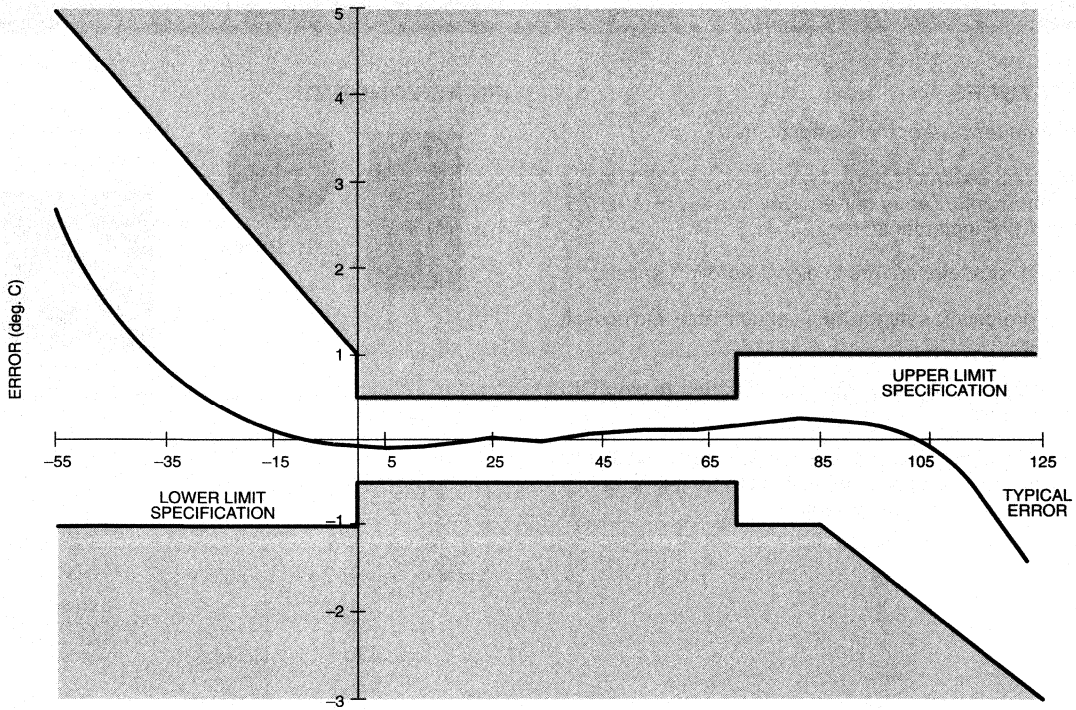
1-WIRE RESET PULSE



1-WIRE PRESENCE DETECT

TYPICAL PERFORMANCE CURVE

DS1820 DIGITAL TERMOMETER AND THERMOSTAT
TEMPERATURE READING ERROR



10

PRELIMINARY

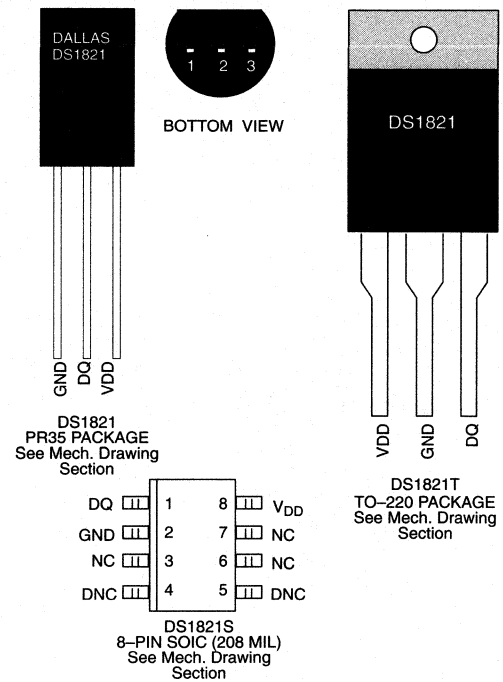
DALLAS SEMICONDUCTOR

DS1821
Programmable Digital Thermostat

FEATURES

- Requires no external components
- Measures temperatures from –55°C to +125°C in 1°C increments. Fahrenheit equivalent is –67°F to +257°F in 1.8°F increments
- Converts temperature to digital word in 1 second
- Thermostatic settings are user definable and nonvolatile
- Available in 3–pin PR35, TO–220, and 8–pin SOIC packages
- Applications include thermostatic controls, industrial systems, consumer products, thermometers, or any thermally sensitive system

PIN ASSIGNMENT



DS1821
PR35 PACKAGE
See Mech. Drawing Section

DS1821T
TO–220 PACKAGE
See Mech. Drawing Section

DS1821S
8–PIN SOIC (208 MIL)
See Mech. Drawing Section

PIN DESCRIPTION

GND	–	Ground
DQ	–	Data In/Out
V_{DD}	–	Power Supply Voltage +5V
NC	–	No Connect
DNC	–	Do Not Connect

DESCRIPTION

The DS1821 Programmable Digital Thermostat provides a thermal alarm logic output when the temperature of the device exceeds a user–defined temperature TH. The output remains active until the temperature drops below user defined temperature TL, allowing for any hysteresis necessary.

User–defined temperature settings are stored in non–volatile memory, so parts can be programmed prior to insertion in a system. Communication to/from the DS1821 is accomplished through the DQ pin in a programming mode; this same pin is used in operation as the thermostat output.

DETAILED PIN DESCRIPTION

PIN PR35	PIN TO–220	PIN 8–PIN SOIC	SYMBOL	DESCRIPTION
1	2/TAB	2	GND	**Ground.**
2	3	1	DQ	**Data input/output pin** for one–wire programming operation; **Thermostat output pin** in normal operation.
3	1	8	V_{DD}	**V_{DD}** pin. +5V nominal.

DS1821S (8–pin SOIC): All pins not specified in this table are not to be connected.

OVERVIEW

The block diagram of Figure 1 shows the major components of the DS1821. The DS1821 has two operating modes: one–wire and thermostat.

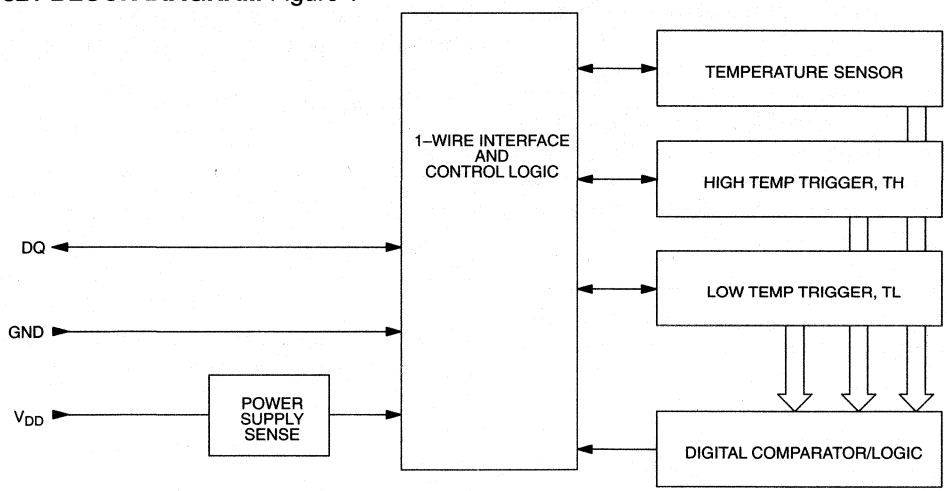
The part arrives from the factory in one–wire mode. In this mode, the DQ pin of the DS1821 is configured as a one–wire communication port which would be connected to a microprocessor. The microprocessor will write data into the high and low temperature trigger registers, TH and TL, respectively, to set up the temperature limits for thermostat operation. In this mode, the result of the last temperature measurement made by the DS1821 may also be read directly by the microprocessor.

Once temperature limits have been set and thermometer operation has been verified, the user may convert the DS1821 from a temperature sensor into a thermostat by writing to a bit in the status register. The part will then be configured for thermostat operation; this will also become the default power–up state for the device on the subsequent power up.

In thermostat mode, the DQ line becomes the thermostat output. This open drain output will go to its active state (programmable on/off) when the temperature of the DS1821 goes above the limit set in the TH register, and will remain active until the temperature goes below the limit programmed into the TL register.

If the user wishes to establish communications with the DS1821 once it has been placed in thermostat mode (for example, to change temperature trip point limits), this may be done by dropping V_{DD} while holding the DQ line high, then clocking the DQ line 16 times. The part will then be placed into one–wire mode, and will allow the I/O functions of the device to operate, and reads from or writes to the memory are possible. This does not change the power up state of the device, unless the user writes the configuration bit to do so.

DS1821 BLOCK DIAGRAM Figure 1



OPERATION

Temperature Measurement

The DS1821 measures temperatures through the use of an on–board proprietary temperature measurement technique. The temperature reading is provided in an 8–bit, two's complement reading. Table 1 describes the exact relationship of output data to measured temperature. The data is transmitted serially over the 1–wire interface. The DS1821 can measure temperature over the range of –55°C to +125°C in 1°C increments. For Fahrenheit usage, a lookup table or conversion factor must be used.

TEMPERATURE/DATA RELATIONSHIPS Table 1

TEMPERATURE	DIGITAL OUTPUT (Binary)	DIGITAL OUTPUT (Hex)
+125°C	01111101	7Dh
+25°C	00011001	19h
0°C	00000000	00h
–1°C	11111111	FFh
–25°C	11100111	E7h
–55°C	11001001	C9h

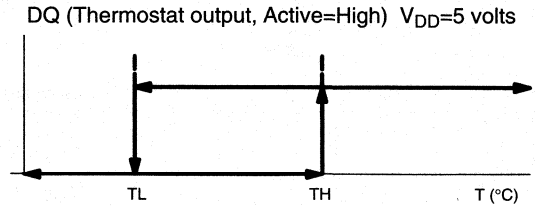
Thermostat Controls

In its thermostat mode, the DS1821 functions as a thermostat with programmable hysteresis, as shown in Figure 2. Temperature conversions begin as soon as V_{DD} is applied to the device, and are continually made, so that the thermostat output updates as soon as a temperature conversion is complete. This is approximately once every second.

When the DS1821's temperature meets or exceeds the value stored in the high temperature trip register (TH), the output becomes active, and will stay active until the temperature falls below the temperature stored in the low temperature trigger register (TL). In this way, any amount of hysteresis may be obtained.

The active state for the output is programmable by the user, so that an active state may either be a logic 1 (+5V, output transistor off) or a logic 0 (0V, output transistor on).

THERMOSTAT OUTPUT OPERATION Figure 2



PROGRAMMING THE DS1821

To program the DS1821, it must be placed in one–wire mode. This mode is active when the device arrives from the factory. Once the part has been programmed, and if the user has set the power–up state to thermostat mode, one–wire mode may only be achieved by bringing the V_{DD} pin low while holding the DQ line high, then clocking the DQ line 16 times.

The DS1821 has four internal registers that may be accessed through the DQ pin when the device is in one–wire mode. These registers are the high temperature trigger (TH), low temperature trigger (TL), the actual measured temperature result, and the status register. The TH,TL, and status registers are all nonvolatile.

The DS1821 must have temperature settings resident in the TH and TL registers for thermostatic operation. The temperature result register and the thermostat limit registers (TH and TL) hold an eight bit number in the two's complement format described in Table 1.

A status register is also present, indicating the status of the thermostatic control, and allowing configuration of the output polarity as either active high or active low, and establishes the power–up state of the device.

The status register is defined as follows:

where,

DONE	1	NVB	THF	TLF	T/$\overline{R}$	POL	1SHOT

DONE = Conversion Done bit. "1" = Conversion complete, "0" = conversion in progress.

THF = Temperature High Flag. This bit will normally be "0", but will be set to "1" when the tempera-

ture exceeds the value of TH. It will remain "1" until reset by writing 0 into this location. This feature provides a method of determining if the DS1821 has ever been subjected to temperatures above TH. This bit is nonvolatile, and is stored in E^2 memory.

TLF = Temperature Low Flag. This bit will normally be "0", but will be set to "1" when the temperature is lower than the value of TL. It will remain "1" until reset by writing 0 into this location. This feature provides a method of determining if the DS1821 has ever been subjected to temperatures below TL. This bit is nonvolatile, and is stored in E^2 memory.

NVB= Nonvolatile memory busy flag. "1" = Write to an E^2 memory cell in progress, "0" = nonvolatile memory is not busy. A write to E^2 may take up to 10 ms.

T/R* = Power–up mode bit. If set to a "1", the DS1821 will power up in a thermostat mode. If set to a "0", the device will power up in one–wire "read" mode. This bit is nonvolatile.

POL = Output Polarity Bit. "1" = active high, "0" = active low. This bit is nonvolatile.

1SHOT= One Shot Mode. If 1SHOT is "1", the DS1821 will perform one temperature conversion upon reception of the Start Convert T protocol. If 1SHOT is "0", the DS1821 will continuously perform temperature conversions. Note that the one–shot mode is available only when the device is in one–wire mode. In thermostat mode, the device continuously performs temperature conversions. This bit is nonvolatile.

PROGRAMMING COMMAND FUNCTIONS

The command set for the DS1821 as shown in Table 2 is as follows:

Read Temperature [AAh]

This command reads the contents of the register which contains the last temperature conversion result.

Write TH [01h]

This command writes to the TH (HIGH TEMPERATURE) register. After issuing this command, the user writes eight bits of data to the TH register.

Write TL [02h]

This command writes to the TL (LOW TEMPERATURE) register. After issuing this command, the user writes eight bits of data to the TL register.

Read TH [A1h]

This command reads the value of the TH (HIGH TEMPERATURE) register. After issuing this command, the user reads the eight bits of data present in the TH register.

Read TL [A2h]

This command reads the value of the TL (LOW TEMPERATURE) register. After issuing this command, the user reads the eight bits of data present in the TL register.

Write Status [0Ch]

This command writes to the status register. This would be used for clearing the values of the THF and TLF flags, and setting the T/$\overline{R}$, POL and 1SHOT bits. After issuing this command, the user writes the eight bit data into the register.

Read Status [ACh]

This command reads the value in the status register. After issuing this command, the user reads the eight bits present in the status register.

Start Convert T [EEh]

This command begins a temperature conversion. No further data is required. In one–shot mode, the temperature conversion will be performed and then the DS1821 will remain idle. In continuous mode, this command will initiate continuous conversions.

Stop Convert T [22h]

This command stops temperature conversion. No further data is required. This command may be used to halt a DS1821 in continuous conversion mode. After issuing this command, the current temperature measurement will be completed, and then the DS1821 will remain idle until a Start Convert T is issued to resume continuous operation.

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RETURNING TO ONE–WIRE MODE FROM THERMOSTAT MODE

The operating mode of the DS1821 is determined at power–up, depending upon the setting of the T/$\overline{R}$ bit. If the T/$\overline{R}$ bit is set to a "1", the DS1821 will power up in thermostat mode. In this mode, the device cannot be written to or read from over the DQ line. However, it is possible to return to the one–wire "read" mode temporarily, in cases where thermostat limits may need to be changed after insertion and use in a system.

To return to the one–wire "read" mode, the V_{DD} pin of the DS1821 is brought to 0V, while the DQ line is held high. The DQ line must then be clocked low 16 times. After this is accomplished, V_{DD} may be brought high again, and the DS1821 will then be in one–wire "read" mode. If V_{DD} is brought low again and then high, the part will return to thermostat operation, unless during the "read" mode the user wrote the T/$\overline{R}$ bit to "0", in which case the part will now power up in one–wire mode.

DS1821 COMMAND SET Table 2

INSTRUCTION	DESCRIPTION	PROTOCOL	1–WIRE BUS DATA AFTER ISSUING PROTOCOL
TEMPERATURE CONVERSION COMMANDS			
Start Convert T	Initiates temperature conversion.	EEh	idle
Stop Convert T	Halts temperature conversion.	22h	idle
Read Temperature	Reads last converted temperature value from temperature register.	AAh	<read data>
THERMOSTAT COMMANDS			
Write TH	Writes high temperature limit value into TH register.	01h	<write data>
Write TL	Writes low temperature limit value into TL register.	02h	<write data>
Read TH	Reads stored value of high temperature limit from TH register.	A1h	<read data>
Read TL	Reads stored value of low temperature limit from TL register.	A2h	<read data>
Write Status	Writes configuration data to configuration register.	0Ch	<write data>
Read Status	Reads configuration data from configuration register.	ACh	<read data>

Example: CPU sets up DS1821 for low temp limit of +10°C and high temp limit of +40°C, output active high (i.e. DQ pin is off), then instructs the DS1821 to become a thermostat.

DQ PORT PIN	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480–960 µs).
RX	Presence	Presence pulse.
TX	01h	CPU issues Write TH command.
TX	28h	CPU sends data for TH limit of +40°C.
TX	Reset	Reset pulse (480–960 µs).
RX	Presence	Presence pulse.
TX	02h	CPU issues Write TL command.
TX	0Ah	CPU sends data for TL limit of +10°C.
TX	Reset	Reset pulse (480–960 µs).
RX	Presence	Presence pulse.
TX	A1h	CPU issues Read TH command.
RX	28h	DS1821 sends back stored value of TH for CPU to verify.
TX	Reset	Reset pulse (480–960 µs).
RX	Presence	Presence pulse.
TX	A2h	CPU issues Read TL command.
RX	0Ah	DS1821 sends back stored value of TL for CPU to verify.
TX	Reset	Reset pulse (480–960 µs).
RX	Presence	Presence pulse.
TX	0Ch	CPU issues Write Config command.
TX	06h	CPU sets DS1821 up for active high output, sets T/$\overline{R}$ bit to instruct device to become thermostat.
<high impedance>		Power cycles; DS1821 now comes up in thermostat mode.

1–WIRE BUS SYSTEM

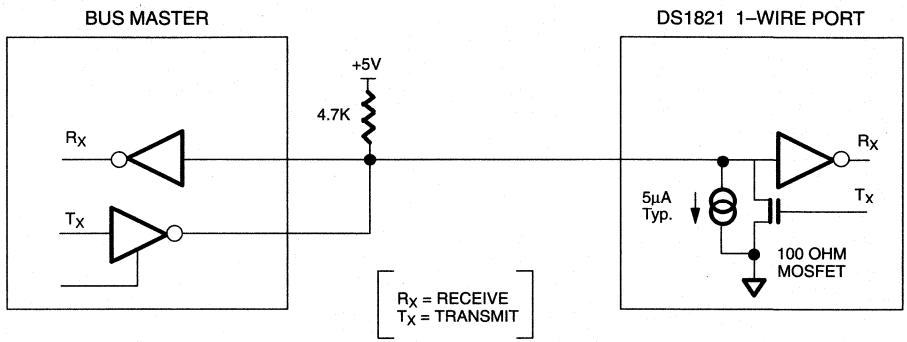
The DS1821 1–wire bus is a system which has a single bus master and one slave. The DS1821 behaves as a slave. The DS1821 is not able to be multidropped, unlike other 1–wire devices from Dallas Semiconductor.

The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1–wire signaling (signal types and timing).

HARDWARE CONFIGURATION

The 1–wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1–wire bus must have open drain or 3–state outputs. The 1–wire port of the DS1821 (DQ pin) is open drain with an internal circuit equivalent to that shown in Figure 4. The 1–wire bus requires a pull–up resistor of approximately 5K.

HARDWARE CONFIGURATION Figure 4



The idle state for the 1–wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 480 µs, all components on the bus will be reset.

TRANSACTION SEQUENCE

The protocol for accessing the DS1821 via the 1–wire port is as follows:

- Initialization
- Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1–wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s).

The presence pulse lets the bus master know that the DS1821 is on the bus and is ready to operate. For more details, see the "1–Wire Signaling" section.

1–WIRE SIGNALING

The DS1821 requires strict protocols to insure data integrity. The protocol consists of several types of signaling on one line: reset pulse, presence pulse, write 0, write 1, read 0, and read 1. All of these signals, with the exception of the presence pulse, are initiated by the bus master.

The initialization sequence required to begin any communication with the DS1821 is shown in Figure 5. A reset pulse followed by a presence pulse indicates the DS1821 is ready to send or receive data given the correct function command.

The bus master transmits (TX) a reset pulse (a low signal for a minimum of 480 µs). The bus master then releases the line and goes into a receive mode (RX). The 1–wire bus is pulled to a high state via the 5K pull–up resistor . After detecting the rising edge on the DQ pin, the DS1821 waits 15–60 µs and then transmits the presence pulse (a low signal for 60–240 µs).

READ/WRITE TIME SLOTS

DS1821 data is read and written through the use of time slots to manipulate bits and a command word to specify the transaction.

Write Time Slots

A write time slot is initiated when the host pulls the data line from a high logic level to a low logic level. There are two types of write time slots: Write One time slots and Write Zero time slots. All write time slots must be a minimum of 60 microseconds in duration with a minimum of a one microsecond recovery time between individual write cycles.

The DS1821 samples the DQ line in a window of 15 µs to 60 µs after the DQ line falls. If the line is high, a Write One occurs. If the line is low, a Write Zero occurs (see Figure 6).

For the host to generate a Write One time slot, the data line must be pulled to a logic low level and then released, allowing the data line to pull up to a high level within 15 microseconds after the start of the write time slot.

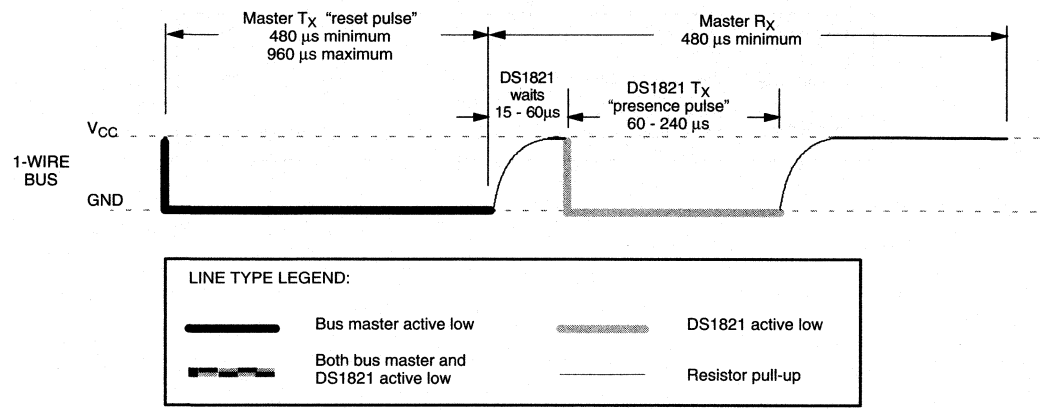
For the host to generate a Write Zero time slot, the data line must be pulled to a logic low level and remain low for the duration of the write time slot.

Read Time Slots

The host generates read time slots when data is to be read from the DS1821. A read time slot is initiated when the host pulls the data line from a logic high level to logic low level. The data line must remain at a low logic level for a minimum of one microsecond; output data from the DS1821 is then valid for the next 14 microseconds maximum. The host therefore must stop driving the DQ pin low in order to read its state 15 microseconds from the start of the read slot (see Figure 6). By the end of the read time slot, the DQ pin will pull back high via the external pull–up resistor. All read time slots must be a minimum of 60 microseconds in duration with a minimum of a one microsecond recovery time between individual read slots.

Figure 7 shows that the sum of T_{INIT}, T_{RC}, and T_{SAMPLE} must be less than 15 µs. Figure 8 shows that system timing margin is maximized by keeping T_{INIT} and T_{RC} as small as possible and by locating the master sample time towards the end of the 15 µs period.

INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 5



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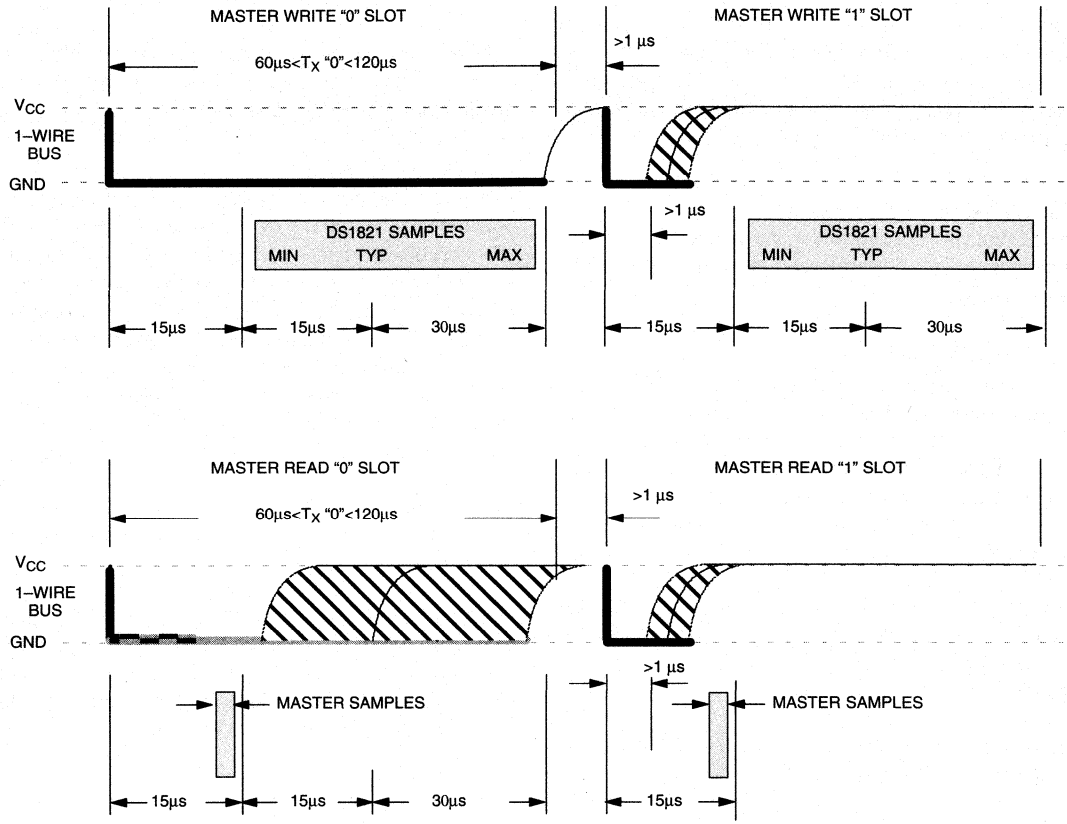
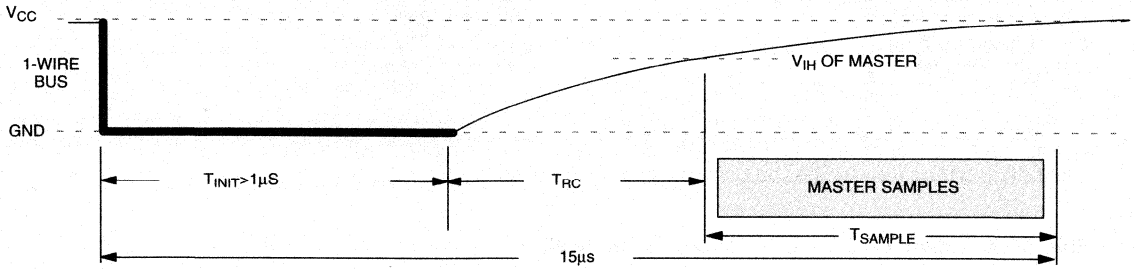
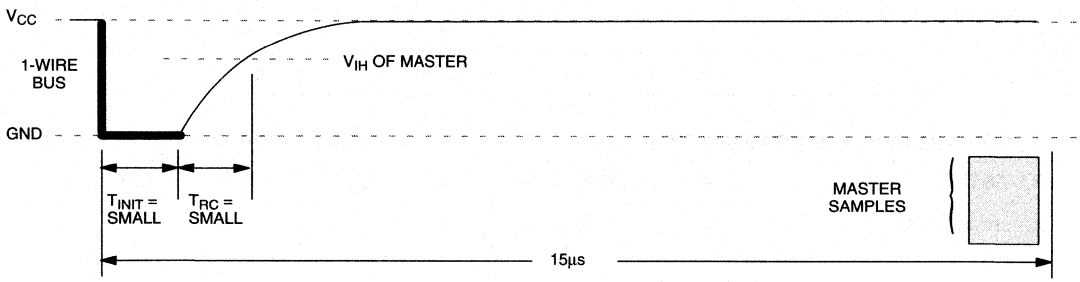
READ/WRITE TIMING DIAGRAM Figure 6

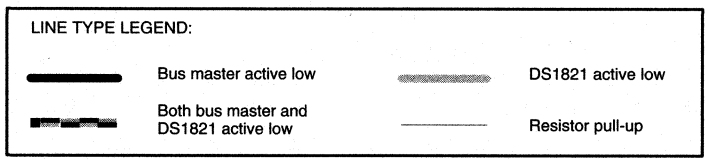


DETAILED MASTER READ "1" TIMING Figure 7



RECOMMENDED MASTER READ "1" TIMING Figure 8





10

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	–55°C to +125°C
Storage Temperature	–55°C to 125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD}	Operation	4.3	5.0	5.5	V	1
Data Pin	DQ		–0.5		5.5	V	1
Logic 1	V_{IH}		2.0		V_{CC}+0.3	V	1, 2
Logic 0	V_{IL}		–0.3		+0.8	V	1, 3

DC ELECTRICAL CHARACTERISTICS

(–55°C to +125°C; V_{DD}=4.3V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Thermometer Error	T_{ERR}	–40°C to +85°C			±1	°C	
		–55°C to –40°C and +85°C to +125°C			±2	°C	
Open Drain Output Logic Low (DQ pin)	V_{IL}		–0.3		+0.8	V	1, 3
Sink Current	I_L	V_{DQ}=0.4V	–4.0			mA	1
Standby Current	I_Q			100	150	nA	7
Active Current	I_{DD}	Temperature Conversions, Programming		500	1000	µA	4
Input Resistance	R_I			500		KΩ	5

AC ELECTRICAL CHARACTERISTICS: 1–WIRE INTERFACE

(–55°C to +125°C; V_{DD}=4.3V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Temperature Conversion Time	t_{CONV}		1.2	2	s	
Time Slot	t_{SLOT}	60		120	µs	
Recovery Time	t_{REC}	1			µs	
Write 0 Low Time	t_{LOW0}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Read Data Valid	t_{RDV}			15	µs	
Reset Time High	t_{RSTH}	480			µs	
Reset Time Low	t_{RSTL}	480		4800	µs	
Presence Detect High	t_{PDHIGH}	15		60	µs	
Presence Detect Low	t_{PDLOW}	60		240	µs	
EEPROM Write Time	t_{WR}		10	50	µs	
V_{DD} Low to Mode Toggle Clock Low	t_{PC}	100			ns	6
Mode Toggle Clock 16 High to V_{DD} High	t_{CP}	100			ns	
Mode Toggle Clock Pulse Low Time	t_{CL}	0.1		10	µs	
Mode Toggle Clock Pulse High Time	t_{CH}	0.1		10	µs	
Mode Toggle Clock High–to–Low or Low–to–High Transition Time	t_T			100	ns	
Capacitance	$C_{IN/OUT}$			25	pF	

NOTES:

1. All voltages are referenced to ground.
2. Logic one voltages are specified at a source current of 1 mA.
3. Logic zero voltages are specified at a sink current of 4 mA.
4. I_{DD} specified with V_{CC} at 5.0V
5. DQ line in "hi–Z" state and Idq=0.
6. Time for part to disable thermostat output.
7. Standby current specified up to 70°C. Standby current may be up to 5 µA at 125°C.

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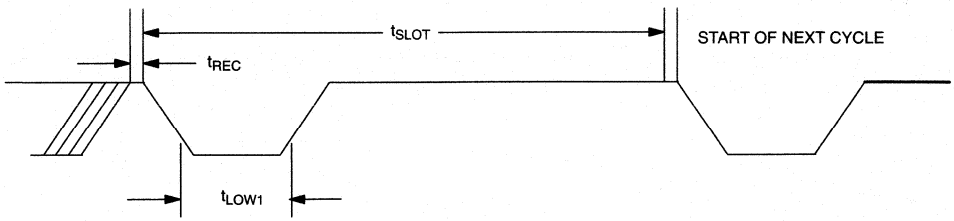
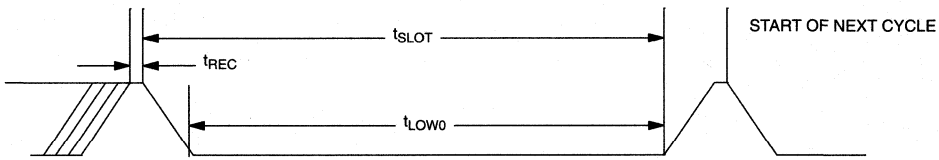
TIMING DIAGRAMS

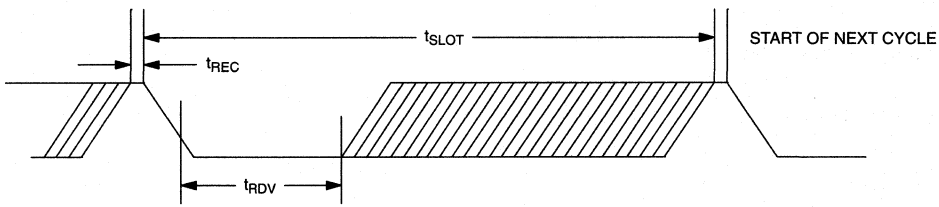
1–WIRE WRITE ONE TIME SLOT



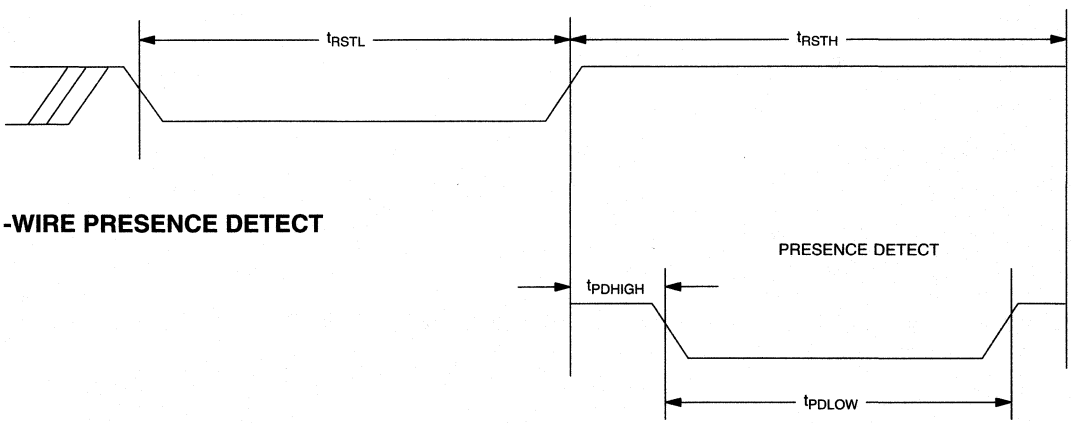
1–WIRE WRITE ZERO TIME SLOT



1-WIRE READ ZERO TIME SLOT

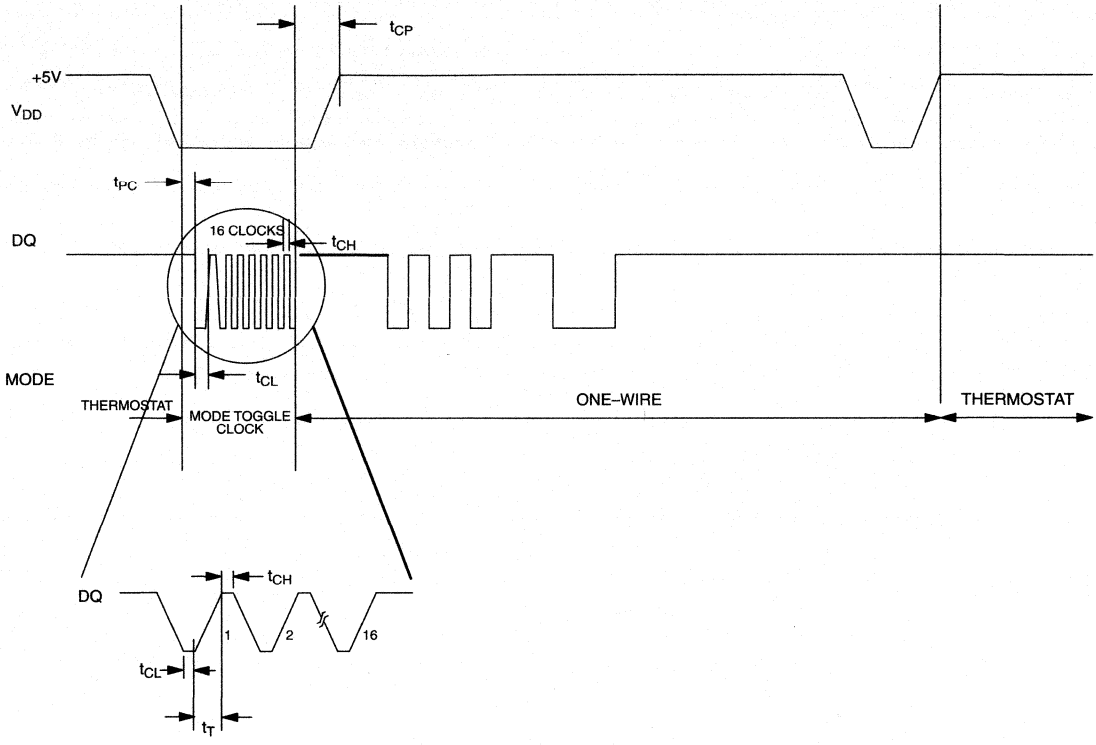


1-WIRE RESET PULSE



1-WIRE PRESENCE DETECT

MODE TOGGLE TIMING (Return to 1–wire mode after setting T/$\overline{R}$ bit)



MECHANICAL DRAWINGS

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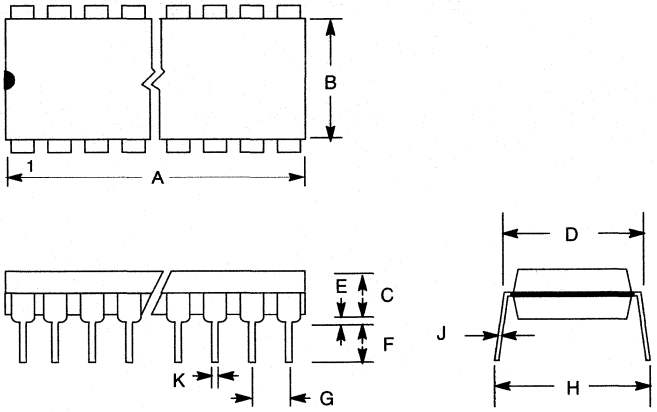
8– TO 28–PIN DIP (300 MIL)



Includes:

DS1000	DS1228	DS1640
DS1000M	DS1229	DS1651
DS1000–IND	DS1231	DS1652
DS1000M–IND	DS1232	DS1652B
DS1003	DS1232LP	DS1653
DS1003M	DS1234	DS1666
DS1004M	DS1236	DS1667
DS1005	DS1236A	DS1669
DS1005M	DS1237	DS1705
DS1007	DS1238	DS1706
DS1010	DS1238A	DS1707
DS1012M	DS1239	DS1708
DS1013	DS1267	DS1800
DS1013M	DS1275	DS1802
DS1020	DS1291	DS1803
DS1033M	DS1293	DS1804
DS1035M	DS1336	DS1806
DS1040M	DS1620	DS1832
DS1044	DS1621	DS1834
DS1045	DS1623	DS1866
DS1210	DS1624	DS1867
DS1211	DS1625	DS1868
DS1221	DS1632	DS1869

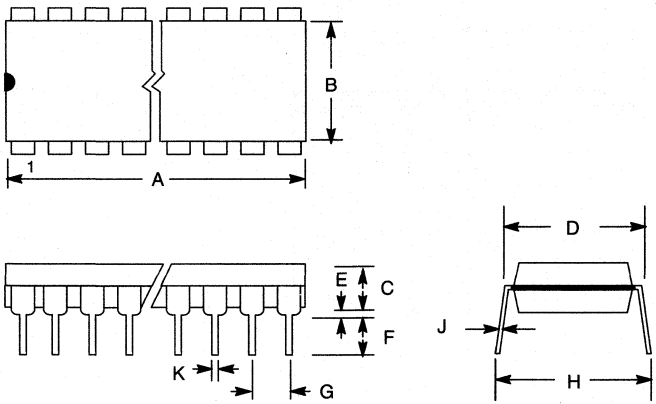
PKG	8-PIN		10-PIN		14-PIN		16-PIN	
DIM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A IN.	0.360	0.400	0.480	0.520	0.740	0.780	0.740	0.780
MM	9.14	10.16	12.19	13.21	18.80	19.81	18.80	19.81
B IN.	0.240	0.260	0.240	0.260	0.240	0.260	0.240	0.260
MM	6.10	6.60	6.10	6.60	6.10	6.60	6.10	6.60
C IN.	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140
MM	3.05	3.56	3.05	3.56	3.05	3.56	3.05	3.56
D IN.	0.300	0.325	0.300	0.325	0.300	0.325	0.300	0.325
MM	7.62	8.26	7.62	8.26	7.62	8.26	7.62	8.26
E IN.	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.040
MM	0.38	1.02	0.38	1.02	0.38	1.02	0.38	1.02
F IN.	0.120	0.140	0.110	0.130	0.120	0.140	0.120	0.140
MM	3.04	3.56	2.79	3.30	3.O4	3.56	3.04	3.56
G IN.	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110
MM	2.29	2.79	2.29	2.79	2.29	2.79	2.29	2.79
H IN	0.320	0.370	0.320	0.370	0.320	0.370	0.320	0.370
MM	8.13	9.40	8.13	9.40	8.13	9.40	8.13	9.40
J IN	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012
MM	0.20	0.30	0.20	0.30	0.20	0.30	0.20	0.30
K IN.	0.015	0.021	0.015	0.021	0.015	0.021	0.015	0.021
MM	0.38	0.53	0.38	0.53	0.38	0.53	0.38	0.53

Continued on following page.

PKG	18-PIN		20-PIN		24-PIN		28-PIN	
DIM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A IN.	0.890	0.920	0.970	1.040	1.150	1.260	1.345	1.370
MM	22.61	23.36	24.63	26.42	29.21	32.00	34.16	34.80
B IN.	0.240	0.260	0.240	0.270	0.250	0.270	0.270	0.295
MM	6.10	6.60	6.09	6.86	6.35	6.86	6.85	7.49
C IN.	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140
MM	3.05	3.56	3.05	3.56	3.05	3.56	3.05	3.56
D IN.	0.300	0.325	0.295	0.325	0.300	0.325	0.300	0.325
MM	7.62	8.26	7.49	8.26	7.62	8.26	7.62	8.26
E IN.	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.050
MM	0.38	1.02	0.38	1.02	0.38	1.02	0.38	1.27
F IN.	0.120	0.140	0.120	0.140	0.125	0.135	0.125	0.135
MM	3.04	3.56	3.04	3.56	3.18	3.48	3.18	3.48
G IN.	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110
MM	2.23	2.79	2.23	2.79	2.23	2.79	2.23	2.79
H IN	0.320	0.370	0.310	0.390	0.320	0.370	0.320	0.370
MM	8.13	9.40	7.87	9.91	8.13	9.40	8.13	9.40
J IN	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012
MM	0.20	0.30	0.20	0.30	0.20	0.30	0.20	0.30
K IN.	0.015	0.021	0.015	0.021	0.015	0.022	0.015	0.022
MM	0.38	0.53	0.38	0.53	0.38	0.56	0.38	0.56

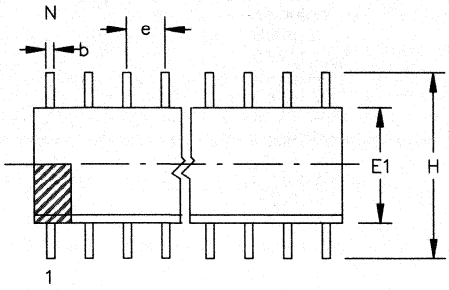
24– TO 40–PIN DIP (600 MIL)

Includes:
DS1212



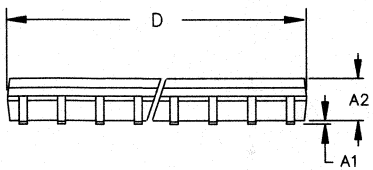
PKG	24-PIN		28-PIN		40-PIN	
DIM	MIN	MAX	MIN	MAX	MIN	MAX
A IN.	1.245	1.270	1.445	1.470	2.050	2.075
MM	31.62	32.25	36.70	37.34	52.07	52.71
B IN.	0.530	0.550	0.530	0.550	0.530	0.550
MM	13.46	13.97	13.46	13.97	13.46	13.97
C IN.	0.140	0.160	0.140	0.160	0.140	0.160
MM	3.56	4.06	3.56	4.06	3.56	4.06
D IN.	0.600	0.625	0.600	0.625	0.600	0.625
MM	15.24	15.88	15.24	15.88	15.24	15.88
E IN.	0.015	0.050	0.015	0.040	0.015	0.040
MM	0.380	1.27	0.380	1.02	0.380	1.02
F IN.	0.120	0.145	0.120	0.145	0.120	0.145
MM	3.05	3.68	3.05	3.68	3.05	3.68
G IN.	0.090	0.110	0.090	0.110	0.090	0.110
MM	2.29	2.79	2.29	2.79	2.29	2.79
H IN	0.625	0.675	0.625	0.675	0.625	0.675
MM	15.88	17.15	15.88	17.15	15.88	17.15
J IN	0.008	0.012	0.008	0.012	0.008	0.012
MM	0.20	0.30	0.20	0.30	0.20	0.30
K IN.	0.015	0.022	0.015	0.022	0.015	0.022
MM	0.38	0.56	0.38	0.56	0.38	.56

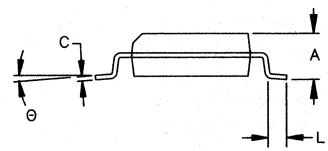
8–, 14–, AND 16–PIN SOIC (.150" BODY WIDTH)



Includes:

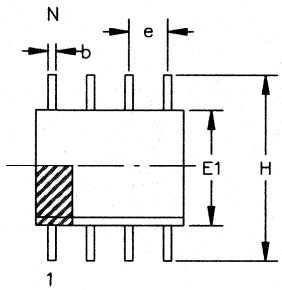
DS1000Z	DS1621S
DS1000Z–IND	DS1705
DS1004Z	DS1706
DS1021Z	DS1707
DS1033Z	DS1708
DS1035Z	DS1803
DS1040Z	DS1804
DS1044R	DS1832
DS1232LPS	DS1834
DS1233M	DS1866



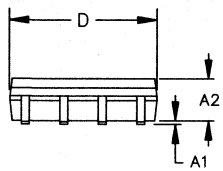


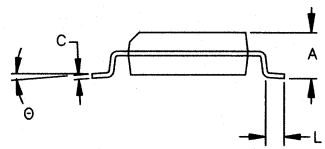
PKG	8-PIN		14-PIN		16-PIN	
DIM	MIN	MAX	MIN	MAX	MIN	MAX
A IN. MM	0.053 1.35	0.069 1.75	0.053 1.35	0.069 1.75	0.053 1.35	0.069 1.75
A1 IN. MM	0.004 0.10	0.010 0.25	0.004 0.10	0.010 0.25	0.004 0.10	0.010 0.25
A2 IN. MM	0.048 1.24	0.062 1.57	0.048 1.24	0.062 1.57	0.048 1.24	0.062 1.57
b IN. MM	0.012 0.030	0.020 0.50	0.012 0.30	0.020 0.50	0.012 0.30	0.020 0.50
C IN MM	0.007 0.17	0.011 0.28	0.007 0.17	0.011 0.28	0.007 0.17	0.011 0.28
D IN. MM	0.188 4.78	0.196 4.98	0.337 8.55	0.344 8.74	0.386 9.80	0.393 9.98
e IN. MM	0.050 BSC 1.27 BSC		0.050 BSC 1.27 BSC		0.050 BSC 1.27 BSC	
E1 IN. MM	0.150 3.81	0.158 4.01	0.150 3.81	0.158 4.01	0.150 3.81	0.158 4.01
H IN. MM	0.230 5.84	0.244 6.20	0.230 5.84	0.244 6.20	0.230 5.84	0.244 6.20
L IN. MM	0.016 0.40	0.050 0.89	0.016 0.40	0.050 0.89	0.016 0.40	0.050 0.89
Θ	0°	8°	0°	8°	0°	8°

8–PIN SOIC (208 MIL)



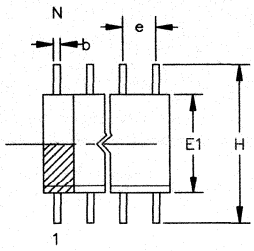
Includes:
DS1620S
DS1623S
DS1624S
DS1625S
DS1651S
DS1652S
DS1669S
DS1821S
DS1869
DS2404

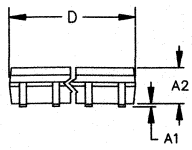


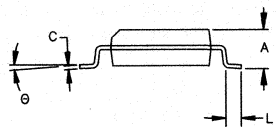


PKG	8-PIN	
DIM	MIN	MAX
A IN. MM	0.072 1.83	0.084 2.13
A1 IN. MM	0.004 0.102	0.010 0.25
A2 IN. MM	0.070 1.78	0.080 2.03
b IN. MM	0.013 0.33	0.020 0.51
C IN. MM	0.006 0.15	0.010 0.25
D IN. MM	0.203 5.16	0.215 5.46
e IN MM	0.050 BSC 1.27 BSC	
E1 IN MM	0.203 5.16	0.213 5.41
H IN. MM	0.302 7.67	0.318 8.07
L IN. MM	0.019 0.48	0.030 0.76
Θ	0°	8°

16–, 20–, 24–, 28–PIN SOIC (300 MIL)







Includes:

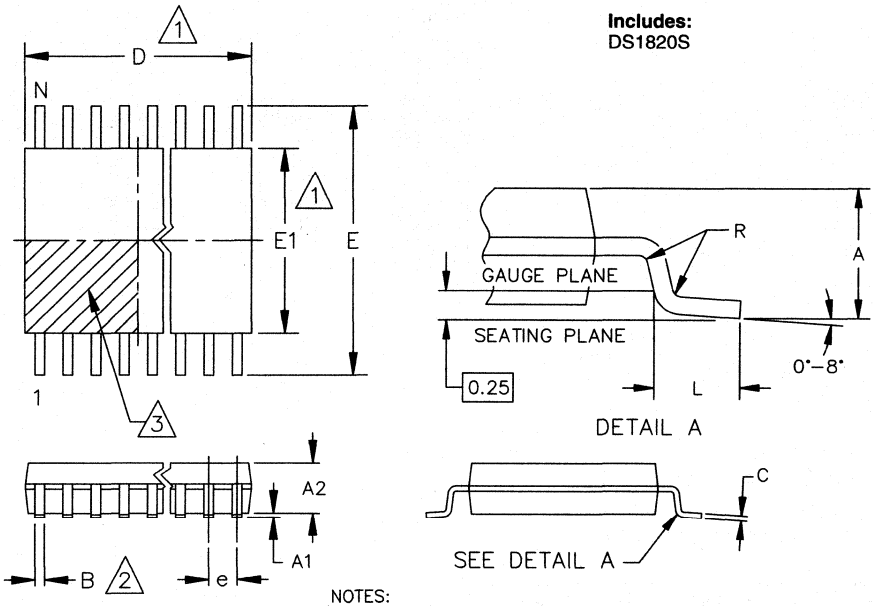
DS1005S	DS1229S	DS1640S
DS1007S	DS1232S	DS1653S
DS1010S	DS1232LPS	DS1666S
DS1013S	DS1234S	DS1667
DS1020S	DS1236S	DS1800
DS1021S	DS1237S	DS1801
DS1045S	DS1238S	DS1802
DS1210S	DS1239S	DS1806S
DS1211S	DS1267S	DS1807S
DS1221S	DS1336S	DS1867
DS1231S	DS1632S	DS1868
DS1228S		

The chamfer on the body is optional. If it is not present, a terminal 1 identifier must be positioned so that 1/2 or more of its area is contained in the hatched zone.

PKG	16-PIN		20-PIN		24-PIN		28-PIN	
DIM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A IN. MM	0.094 2.38	0.105 2.68	0.094 2.38	0.105 2.68	0.094 2.38	0.105 2.68	0.094 2.39	0.105 2.67
A1 IN. MM	0.004 0.102	0.012 0.30	0.004 0.102	0.012 0.30	0.004 0.102	0.012 0.30	0.004 0.102	0.012 0.30
A2 IN. MM	0.089 2.26	0.095 2.41	0.089 2.26	0.095 2.41	0.089 2.26	0.095 2.41	0.089 2.26	0.095 2.41
b IN. MM	0.013 0.33	0.020 0.51	0.013 0.33	0.020 0.51	0.013 0.33	0.020 0.51	0.013 0.33	0.020 0.51
C IN MM	0.009 0.229	0.013 0.33	0.009 0.229	0.013 0.33	0.009 0.229	0.013 0.33	0.009 0.229	0.013 0.33
D IN. MM	0.398 10.11	0.412 10.46	0.498 12.65	0.511 12.99	0.598 15.19	0.612 15.54	0.698 17.73	0.712 18.08
e IN. MM	0.050 BSC 1.27 BSC						0.050 BSC 1.27 BSC	
E1 IN. MM	0.290 7.37	0.300 7.62	0.290 7.37	0.300 7.62	0.290 7.37	0.300 7.62	0.290 7.37	0.300 7.62
H IN MM	0.398 10.11	0.416 10.57	0.398 10.11	0.416 10.57	0.398 10.11	0.416 10.57	0.398 10.11	0.416 10.57
L IN MM	0.016 0.40	0.040 1.02	0.016 0.406	0.040 1.20	0.016 0.40	0.040 1.02	0.016 0.40	0.040 1.02
Θ	0°	8°	0°	8°	0°	8°	0°	8°

14–, 16–, 20–, 24–, 28–PIN SSOP PACKAGE

Includes:
DS1820S

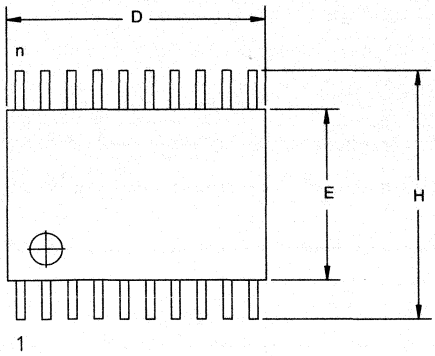


NOTES:

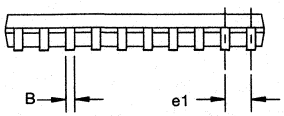
1. DIMENSIONS D & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE PARTING LINE; MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 0.20 MM PER SIDE.
2. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSION TO BE 0.13 MM TOTAL IN EXCESS OF B AT MAXIMUM MATERIAL CONDITION.
3. VISUAL INDEX FEATURE WITHIN CROSSHATCHED AREA.

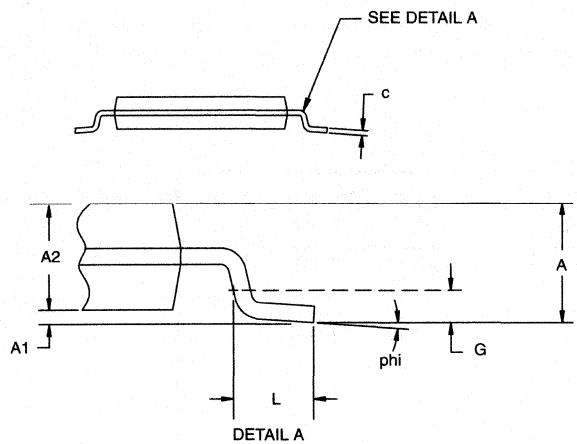
PKG	14/16-PIN		20–PIN		24–PIN		28–PIN	
DIM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	–	2.00	–	2.00	–	2.00	–	2.00
A1	0.05	0.25	0.05	0.25	0.05	0.25	0.05	0.25
A2	1.65	1.85	1.65	1.85	1.65	1.85	1.65	1.85
B	0.22	0.38	0.22	0.38	0.22	0.38	0.22	0.38
C	0.09	0.21	0.09	0.21	0.09	0.21	0.09	0.21
D	5.90	6.50	6.90	7.50	7.90	8.50	9.90	10.50
E	7.40	8.20	7.40	8.20	7.40	8.20	7.40	8.20
E1	5.00	5.60	5.00	5.60	5.00	5.60	5.00	5.60
e	0.65 BSC		0.65 BSC		0.65 BSC		0.65 BSC	
L	0.55	0.95	0.55	0.95	0.55	0.95	0.55	0.95
R	0.09	–	0.09	–	0.09	–	0.09	–

20-PIN TSSOP



Includes:
DS1033E
DS1035E
DS1800
DS1802
DS1806E
DS1867

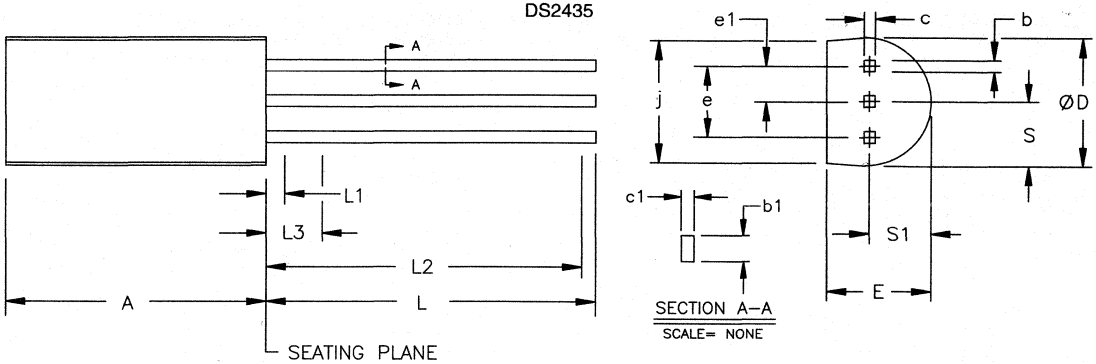




DIM	MIN	MAX
A MM	–	1.10
A1 MM	0.05	–
A2 MM	0.75	1.05
C MM	0.09	0.18
L MM	0.50	0.70
e1 MM	0.65 BSC	
B MM	0.18	0.30
D MM	6.40	6.90
E MM	4.40 NOM	
G MM	0.25 REF	
H MM	6.25	6.55
phi	0°	8°

PR35 PACKAGE

Includes:
DS1820
DS1821
DS2434
DS2435

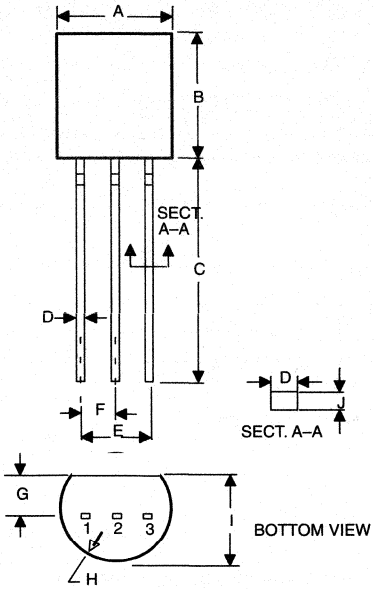


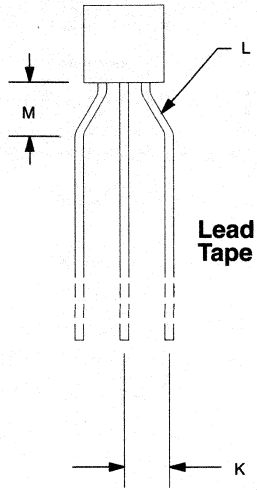
PKG	PR35			
DIM	**MIN**	**TYP**	**MAX**	**NOTE**
A in. **mm**	0.348 8.84	0.350 8.89	0.353 8.97	
b IN. **MM**	0.015 0.38	–	0.022 0.56	
b1 IN. **MM**	0.015 0.38	–	0.018 0.46	2
c IN. **MM**	0.014 0.36	–	0.020 0.51	
c1 IN. **MM**	0.014 0.36	–	0.016 0.41	2
D IN. **MM**	0.178 4.52	0.180 4.57	0.183 4.65	
E IN. **MM**	0.135 3.43	0.140 3.56	0.145 3.68	
e IN. **MM**	0.095 2.41	0.100 2.54	0.105 2.67	
e1 IN. **MM**	0.045 1.14	0.050 1.27	0.055 1.40	
j IN. **MM**	0.160 4.06	–	–	4
L IN. **MM**	0.420 10.67	–	–	
L1 IN. **MM**	–	–	0.050 1.27	1
L2 IN **MM**	0.250 6.35	–	–	2
L3 IN. **MM**	–	–	0.100 2.54	2
S IN. **MM**	0.083 2.11	0.090 2.29	0.099 2.51	3
S1 IN. **MM**	0.080 2.03	0.0825 2.10	0.090 2.29	3

NOTES:

1. TERMINAL DIMENSIONS ARE UNCONTROLLED WITHIN L1.
2. b1 AND c1 APPLY BETWEEN L3 AND L2.
3. S DIMENSION IS DISTANCE FROM TRUE POSITION CENTERLINE OF THE MIDDLE LEAD POSITION TO THE EXTREMITY OF THE BODY.
4. FLAT INDEX SURFACE FOR MARKING.

TO-92 PACKAGE





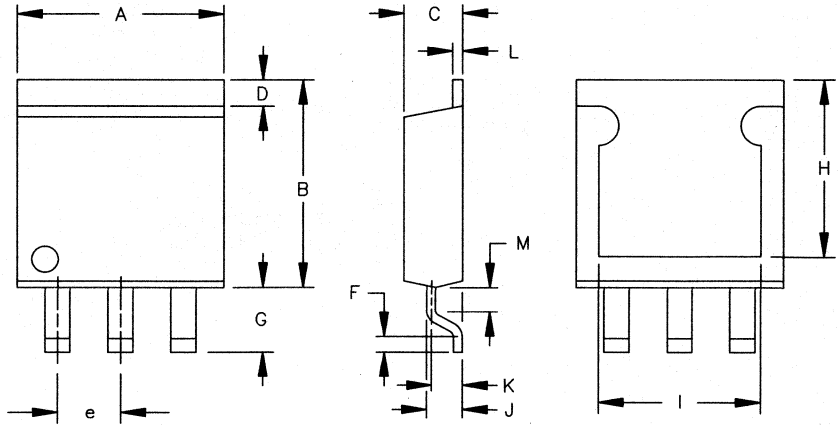
Lead binding for Tape & Reel Order

Includes:

DS1233	DS1813
DS1233A	DS1815
DS1233D	DS1816
DS1233M	DS1818
DS1810	DS1833
DS1811	

PKG	TO-92	
DIM	MIN	MAX
A IN.	0.175	0.195
MM	4.45	4.96
B IN.	0.170	0.195
MM	4.32	4.96
C IN.	0.500	0.610
MM	12.70	15.49
D IN.	0.016	0.022
MM	0.406	0.559
E IN.	0.095	0.105
MM	2.41	2.67
F IN.	0.045	0.060
MM	1.14	1.52
G IN.	0.45	0.060
MM	1.14	1.52
H IN	0.085	0.095
MM	2.16	2.41
I IN	0.130	0.155
MM	3.30	3.94
J IN	0.014	0.020
MM	0.35	0.51
K IN	0.093	0.115
MM	2.36	2.92
L IN	45°	60°
MM		
M IN	0.118 TYPICAL	
MM	3.00	

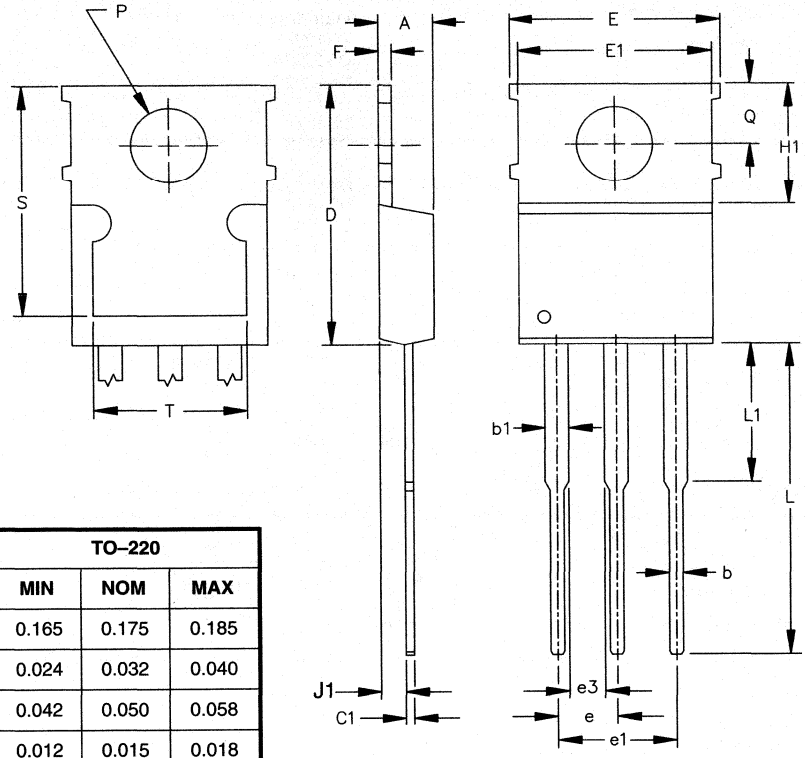
3L D2PAK (TO–220 TABLESS)



NOTES:
1. Dimensions F and M are measured to the center of radius.
2. All dimensions are shown in inches.

PKG	TO–220		
DIM	MIN	NOM	MAX
A	0.386	0.396	0.406
B	0.410	0.420	0.430
C	0.160	0.170	0.180
D	0.035	0.045	0.055
e	0.095	0.105	0.115
F	0.025	0.035	0.045
G	0.125	0.135	0.145
H	0.265	0.275	0.285
I	0.195	0.205	0.215
J	0.088	0.098	0.108
K	0.080	0.090	0.100
L	0.040	0.050	0.060
M	0.070	0.080	0.090

3L TO–220

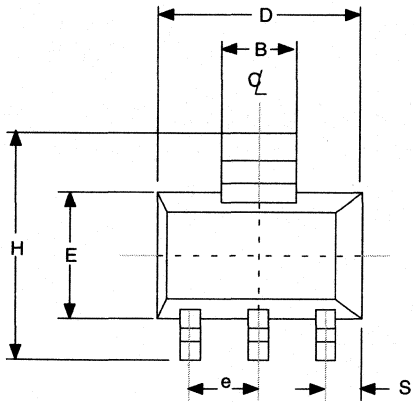


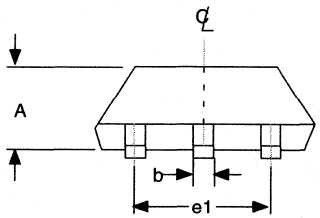
Includes:
DS1633
DS1633x
DS1821T

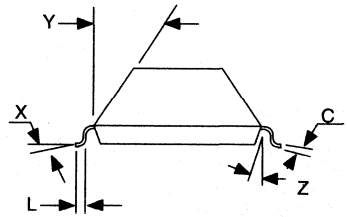
PKG	TO–220		
DIM	MIN	NOM	MAX
A	0.165	0.175	0.185
b	0.024	0.032	0.040
b1	0.042	0.050	0.058
C1	0.012	0.015	0.018
D	0.573	0.588	0.603
E	0.394	0.404	0.414
E1	0.390	0.400	0.410
e	0.090	0.100	0.110
e1	0.190	0.200	0.210
e3	0.045	0.050	0.055
F	0.045	0.050	0.055
H1	0.236	0.248	0.260
J1	0.095	0.105	0.115
L	0.535	0.545	0.555
L1	0.220	0.230	0.240
P	0.146	0.151	0.156
Q	0.100	0.108	0.116
S	0.465	0.475	0.485
T	0.195	0.205	0.215

All dimensions are shown in inches.

SOT–223 PACKAGE





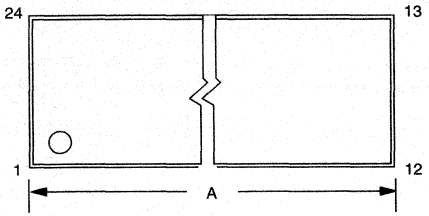


Includes:
DS1233
DS1233A
DS1233D
DS1810
DS1811
DS1813
DS1815
DS1816
DS1818
DS1833

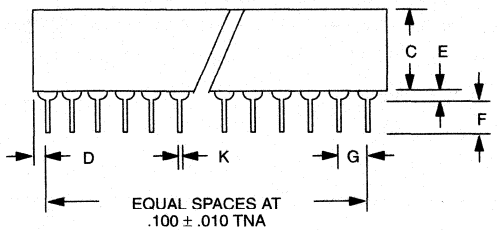
PKG	SOT–223	
DIM	MIN	MAX
A IN. MM	–	0.067 1.70
b IN. MM	0.025 0.64	0.033 0.84
B IN MM	0.116 2.95	0.124 3.15
C IN. MM	0.009 0.23	0.013 0.33
D IN. MM	0.248 6.30	0.263 6.68
e IN MM	0.0905 TYP 2.30 TYP	
e1 IN. MM	0.181 TYP 4.60 TYP	
E IN. MM	0.130 3.30	0.145 3.68
H IN MM	0.264 6.71	0.287 7.29
L IN. MM	0.016 0.41	0.036 0.91
S IN. MM	0.033 0.84	0.041 1.04
X	10° MAX	
Y	10°	20°
Z	10°	20°

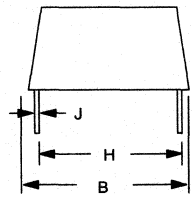
16- AND 24- PIN ENCAPSULATED PACKAGE (FLUSH BOTTOM – 450 MIL.)

Includes:
DS1290
DS1292



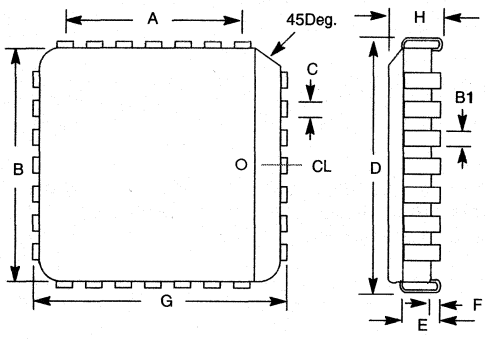
NOTE: On 16–pin package, pins 1 and 16 are missing by design. On 24–pin package, pins 1 and 24 are missing by design.



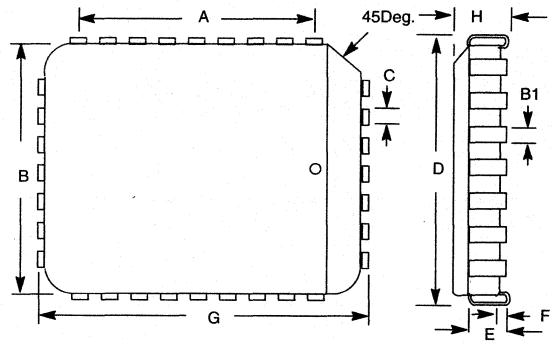


PKG	16-PIN		24-PIN	
DIM	MIN	MAX	MIN	MAX
A IN.	0.820	0.840	1.310	1.330
MM	20.83	21.34	33.27	33.78
B IN.	0.440	0.460	0.440	0.460
MM	11.18	11.68	11.18	11.68
C IN.	0.330	0.370	0.330	0.370
MM	8.38	9.40	8.38	9.40
D IN.	0.180	0.210	0.215	0.245
MM	4.57	5.33	5.46	6.22
E IN.	0.020	0.040	0.020	0.040
MM	0.51	1.02	0.51	1.02
F IN.	0.110	0.140	0.110	0.140
MM	2.79	3.56	2.79	3.56
G IN.	0.090	0.110	0.090	0.110
MM	2.29	2.79	2.29	2.79
H IN	0.330	0.380	0.330	0.380
MM	8.38	9.65	8.38	9.65
J IN	0.008	0.012	0.008	0.012
MM	0.20	0.31	0.20	0.31
K IN.	0.015	0.021	0.015	0.021
MM	0.38	0.53	0.38	0.53

28- AND 32- PIN PLASTIC LEADED CHIP CARRIERS (PLCC)



28- Pin Includes:
DS1212Q



32-Pin Includes:

PKG	28-PIN		32-PIN	
DIM	MIN	MAX	MIN	MAX
A IN. MM	0.300 BSC 7.62		0.400 BSC 10.16	
B IN. MM	0.445 11.30	0.460 11.68	0.442 11.30	0.460 11.68
B1 IN MM	0.013 0.33	0.021 0.53	0.013 0.33	0.021 0.53
C IN MM	0.027 0.68	0.33 0.84	0.027 0.68	0.33 0.84
D IN. MM	0.480 12.19	0.500 12.70	0.480 12.19	0.500 12.70
D2 IN. MM	0.390 9.91	0.430 10.92	0.390 9.91	0.430 10.92
E IN. MM	0.090 2.29	0.120 3.05	0.060 1.52	0.095 2.41
E2 IN. MM	0.390 9.91	0.430 10.92	0.490 12.45	0.530 13.46
F IN. MM	0.020 0.51		0.015 0.38	
G IN MM	0.480 12.19	0.500 12.70	0.580 14.7	0.600 15.24
H IN MM	0.165 4.19	0.180 4.57	0.100 2.54	0.140 3.56